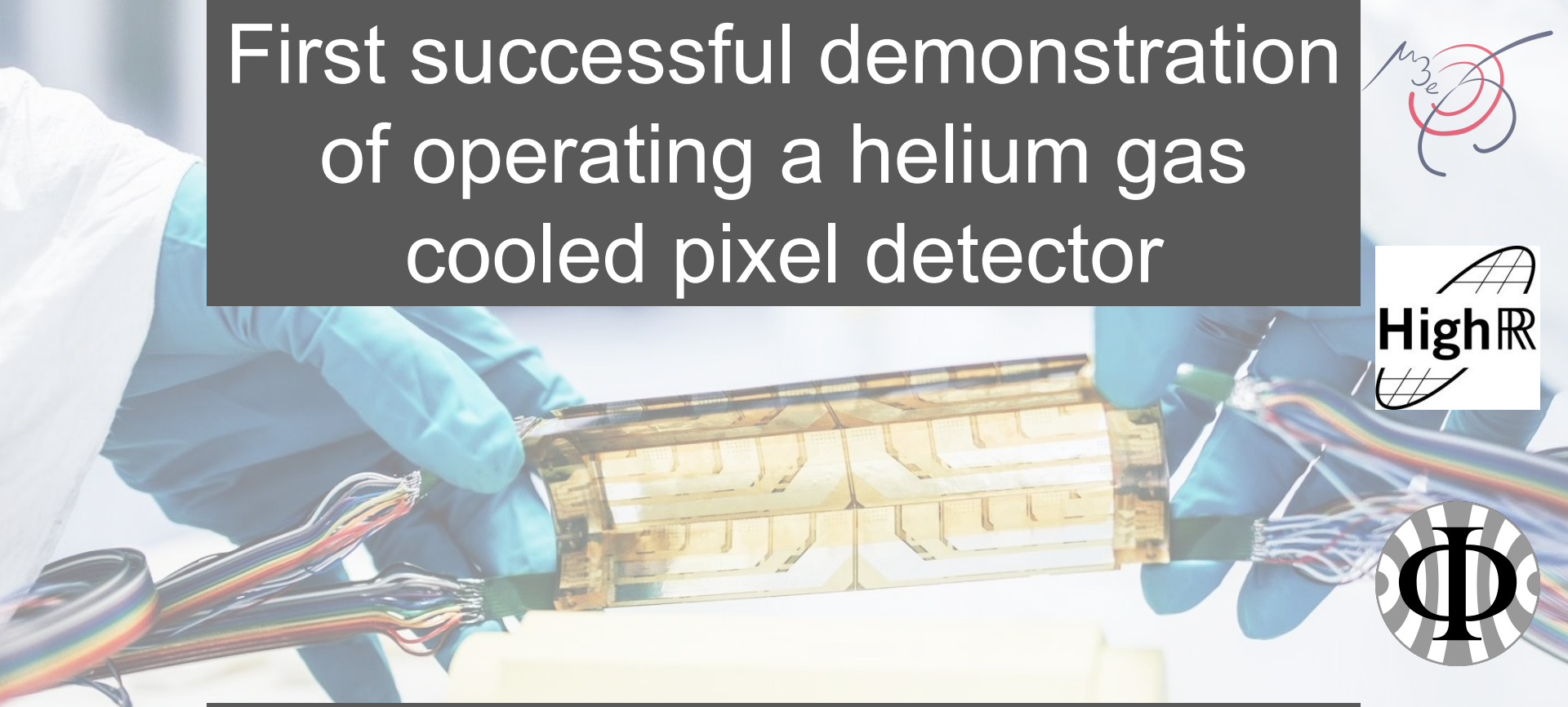
First successful demonstration of operating a helium gas cooled pixel detector



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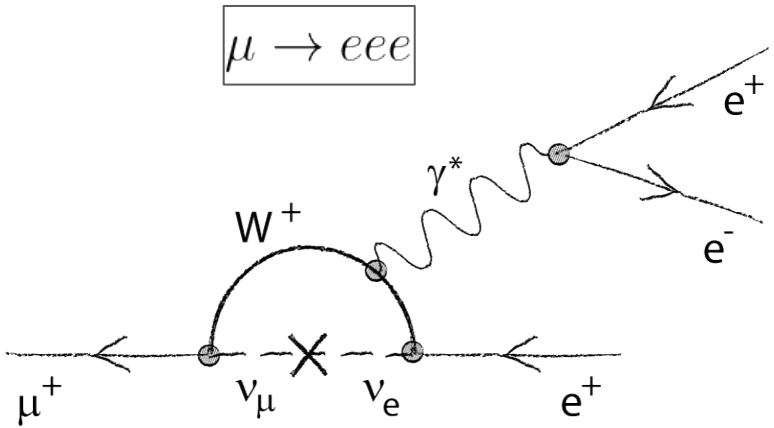
Frank Meier Aeschbacher - Paul Scherrer Institut
FTDM 2022 - 08.06.2022

Probing the Standard Model with Mu3e

- Mu3e is a high-precision experiment at PSI, Switzerland
- μ→eee in SM including neutrino mixing
  ➡ BR (μ→eee) < 10^{-54}
  ➡ beyond observable levels
- New physics might enhance BR by several orders
- Current limit:
  BR (μ→eee) < 10^{-12} (SINDRUM, 1988)
- Aimed single-event sensitivity:
  BR (μ→eee) < $2 \cdot 10^{-15}$ (Phase 1)
  BR (μ→eee) < 10^{-16} (Phase 2)

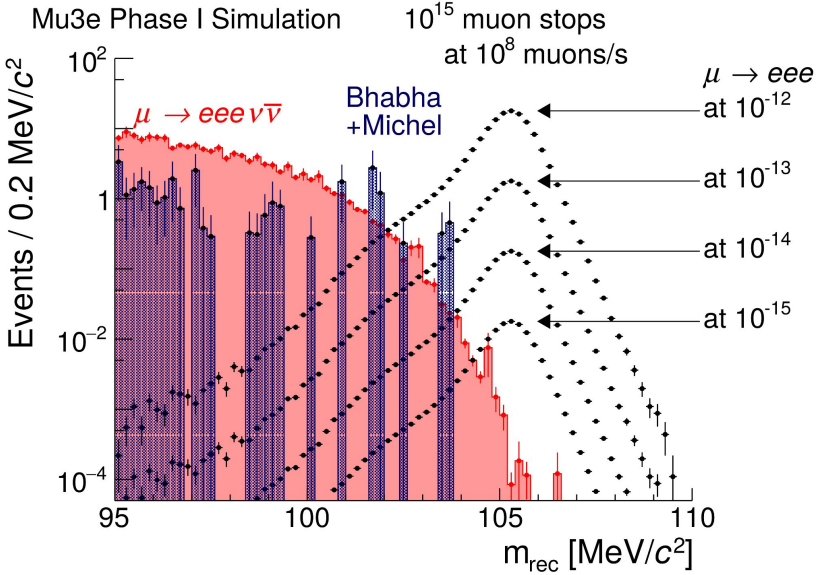


Standard Model decay via neutrino mixing

Experimental challenges

- High rates (≥ 10^8 μ^+ decays per second)
- Low-momentum particles
  - Muons decay at rest
  - Electron/Positron momenta < 53 MeV/c
- Signal-to-background discrimination
  - μ⟶eeevv (main background channel)
  - Limited by multiple-Coulomb scattering
  - Accidental background

➡ **low material budget**
➡ **fast detectors**
➡ **high granularity**

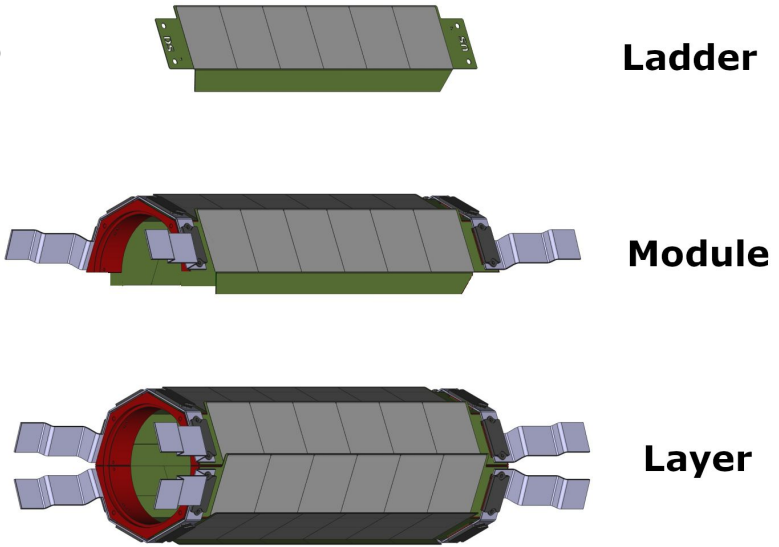


Invariant mass of signal decay, radiative decay and accidental background (Bhaba+Michel) [Mu3e TDR]

Low material budget

Detector ladders:

- High-density interconnect (HDI) + HV-MAPS
- $X/X_0 \approx 1.15$ ‰ per tracking layer
- ≈ 80 µm laminates (HDI)
- 50 µm thin pixel chips (2 x 2.3 cm² area)

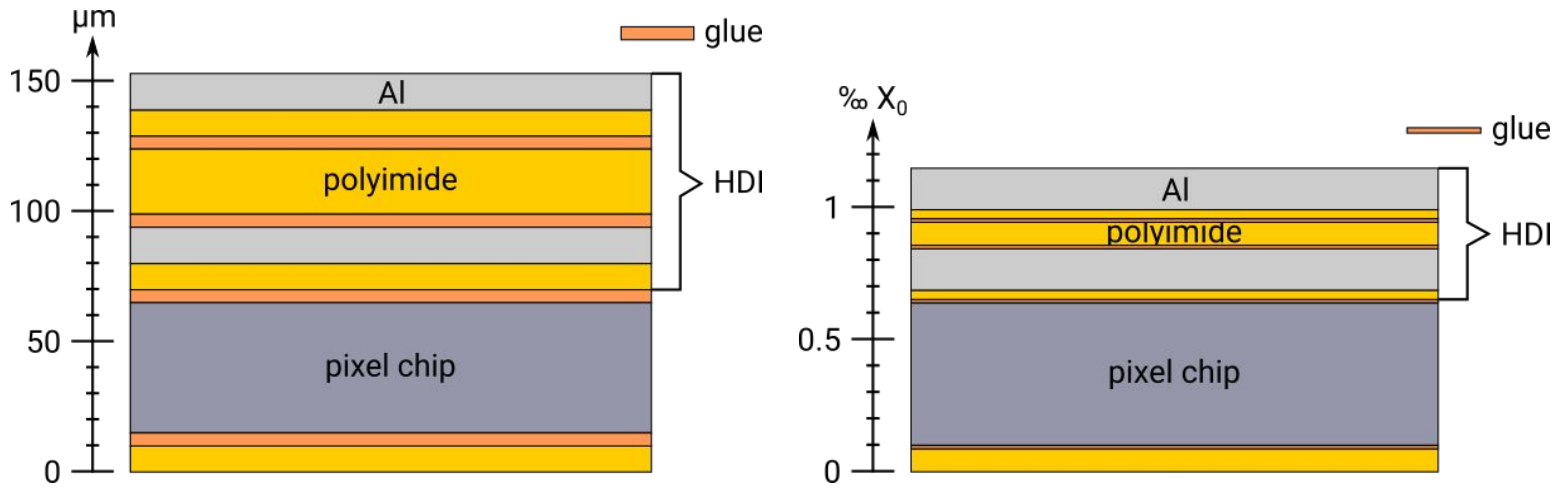


Composition of a Mu3e vertex detector layer

Low material budget

Detector ladders:

- High-density interconnect (HDI) + HV-MAPS
- $X/X_0 \approx 1.15$ ‰ per tracking layer



Low material budget

Cooling:

- HDIs:
  - serve as support
  - host lines for LV, HV, chip configuration and signals
- only missing: infrastructure for cooling

Low material budget

Cooling:

- HDIs:
  - serve as support
  - host lines for LV, HV, chip configuration and signals
- only missing: infrastructure for cooling

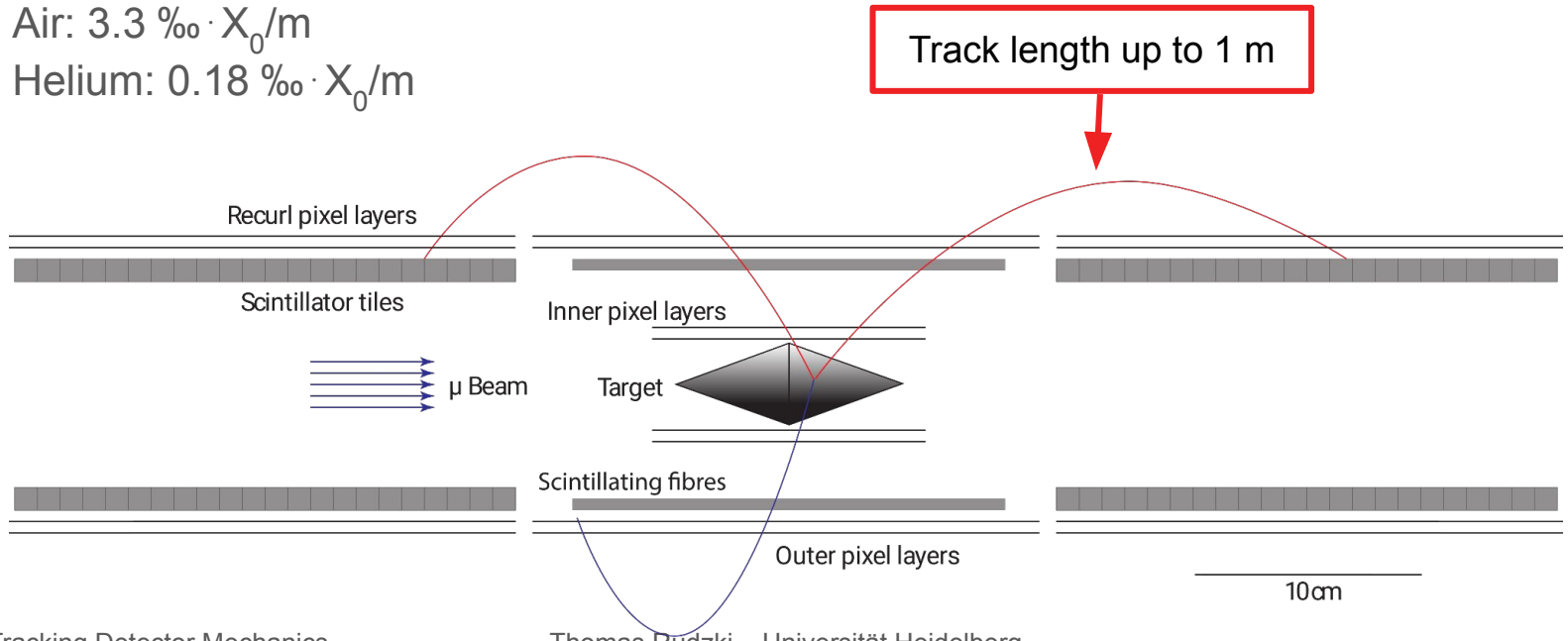
Concept:

- gaseous cooling ➡ little material
- flow channels confined by tracking layers themselves ➡ no additional material

Low material budget

Cooling gas:

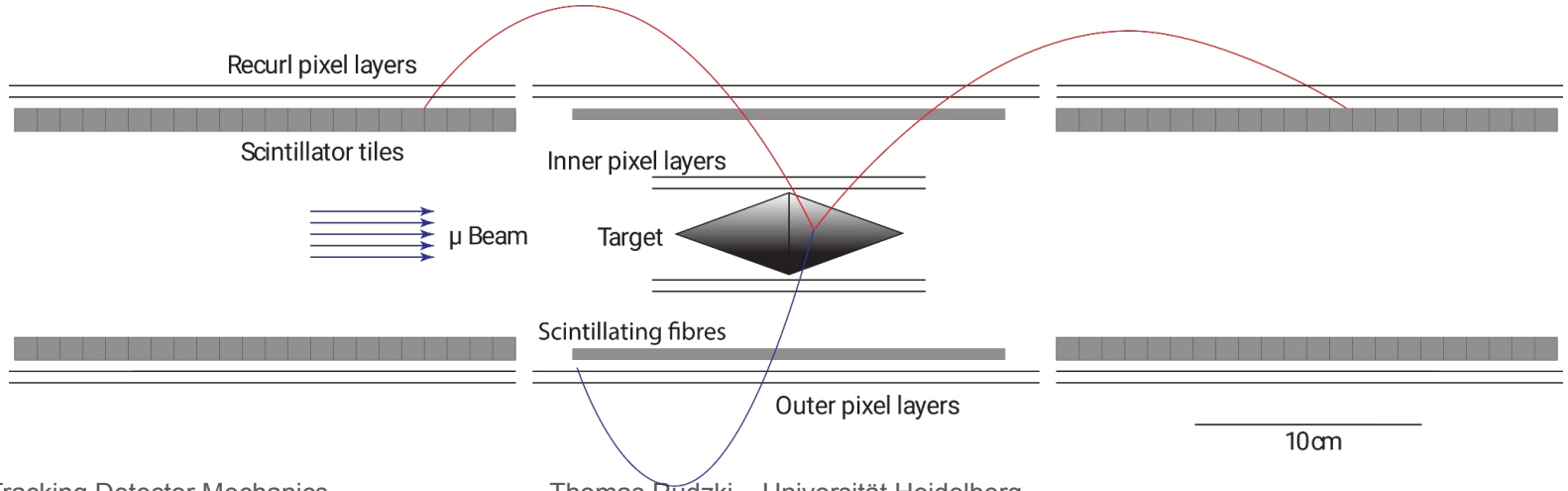
- Air: 3.3 ‰ · X_0/m
- Helium: 0.18 ‰ · X_0/m



Low material budget

Cooling gas:

- ~~Air: 0.33 % · X_0/m~~ ⬅️ corresponds to around 3 tracking layers
- **Helium: 0.018 % · X_0/m**



Gaseous helium cooling

	Air	N_2	Ne	He	H_2	unit
density: ρ	1.29	1.25	0.90	0.18	0.09	kg/m^3
X_0	3.0×10^4	3.3×10^4	3.5×10^4	5.7×10^5	7.5×10^5	cm
X/X_0	0.33	0.30	0.29	0.018	0.013	% (for X = 1 m)
Thermal conductivity: λ	0.241	0.24	0.46	1.43	1.71	$mW/(cm \cdot K)$
C_p	1.01	1.04	1.03	5.23	14.32	$kJ/(kg \cdot K)$
volumetric heat capacity: s	1.30	1.30	0.93	0.94	1.29	$kJ/(m^3 \cdot K)$

Gaseous helium cooling

- high thermal conductivity
- average heat capacity
- despite low density

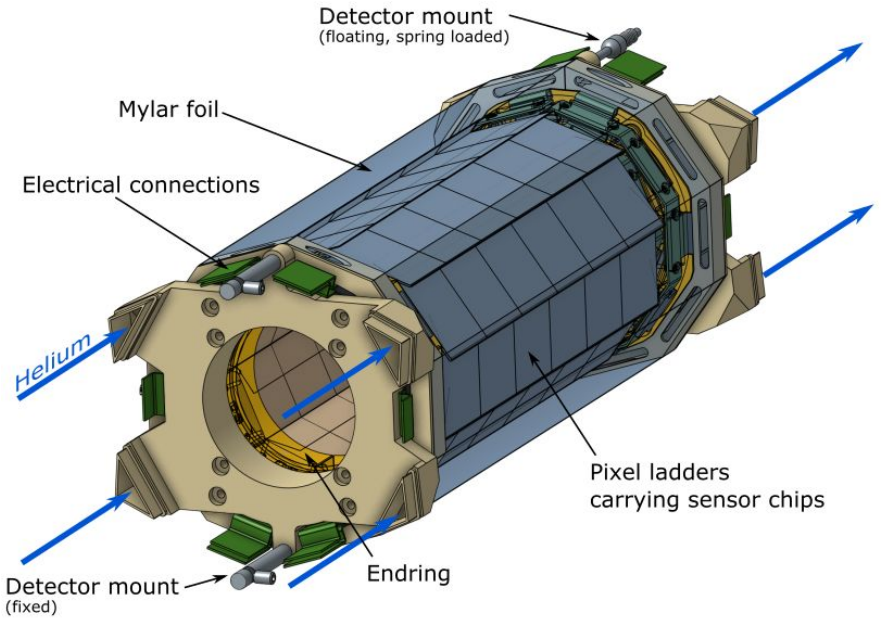
➡ **Gaseous helium offers not only a high radiation length but also acts as an good coolant!**

Specs:

- $T_{chip} < 70°C$ for an inlet temperature of ~ 0°C
- glass transition temperature of adhesives used

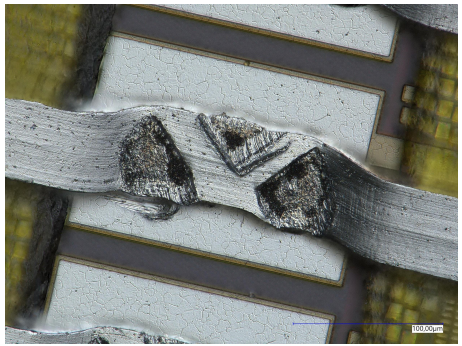
Mu3e vertex detector

- inner two tracking layers
- Layer 0
  - 8 ladders (48 MuPix chips)
  - r = 23.3 mm
- Layer 1
  - 10 ladders (60 MuPix chips)
  - r = 29.8 mm
- 2 helium flow channels
  - between L0/L1
  - around L1, confined by Mylar foil
- estimated heat dissipation 215 mW/cm²
- system designed to cool up to 350 mW/cm²

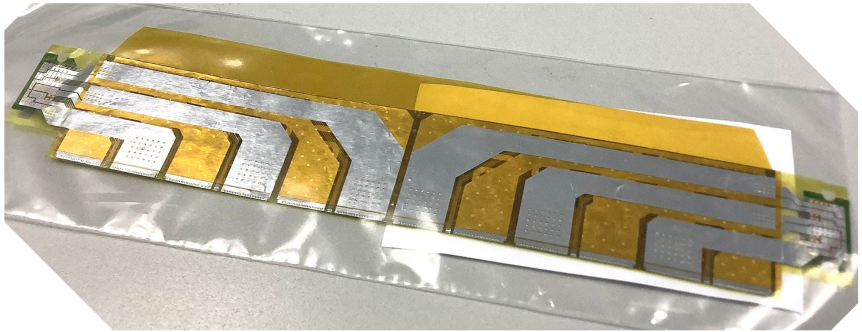


Cooling tests

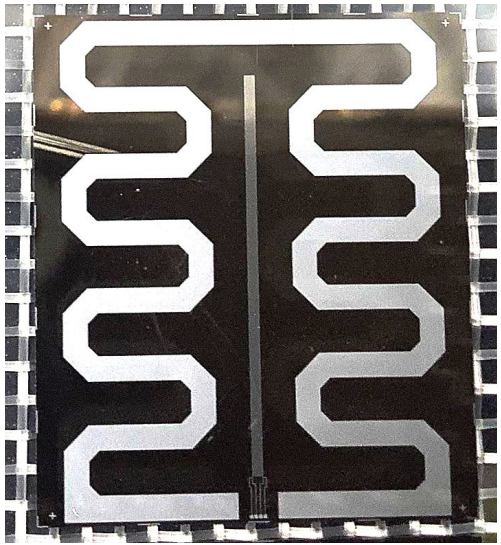
- thermal-mechanical mock-up (mechanical copy of final detector)
- silicon heater chips of final dimensions
  - 3 Ω heating loop
  - ~ 1.2 kΩ resistive thermometer
- spTAB connection to HDI



spTAB connection



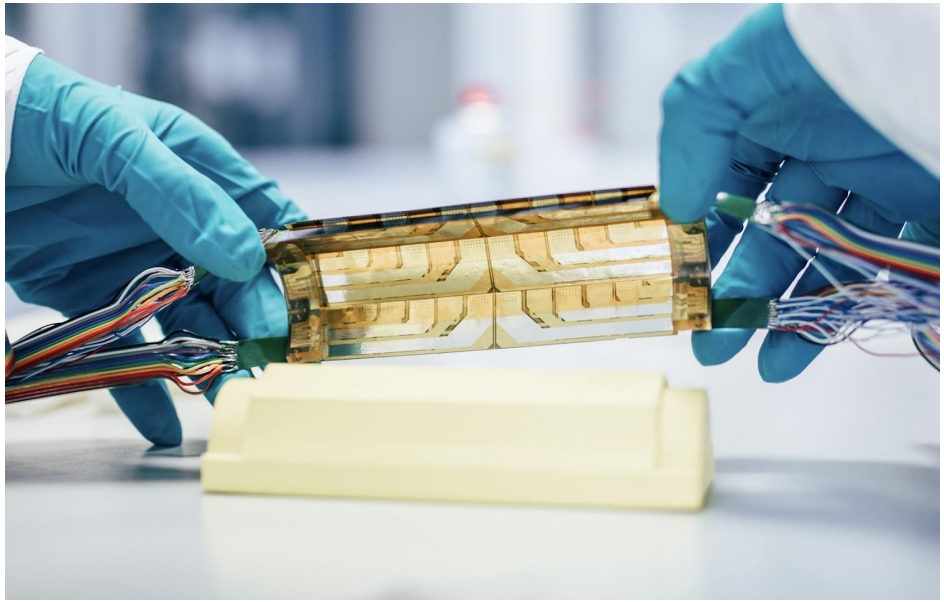
HDI for heater chips



Silicon heater chip

Cooling tests

- thermal-mechanical mock-up
- silicon heater chips of final dimensions
  - 3 Ω heating loop
  - ~ 1.2 kΩ resistive thermometer
- spTAB connection to HDI
- mock-up modules:
  - perfect matching of geometry and material
  - mounted in mini-cage with gaseous helium supply
- simulate heat loads:
  - 215 mW/cm² (expected)
  - 350 mW/cm² (conservative limit)

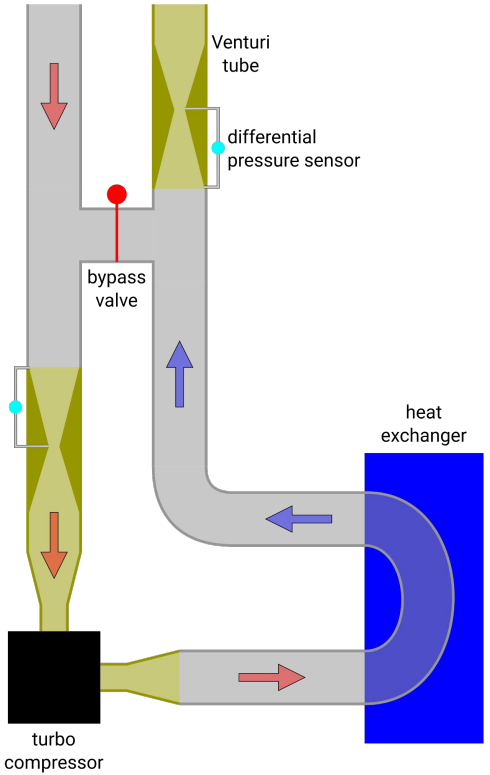


Cooling setup

- Total helium flow of 2 g/s
- Power silicon heaters with constant[1] heat load
- Readout of on-chip thermometers

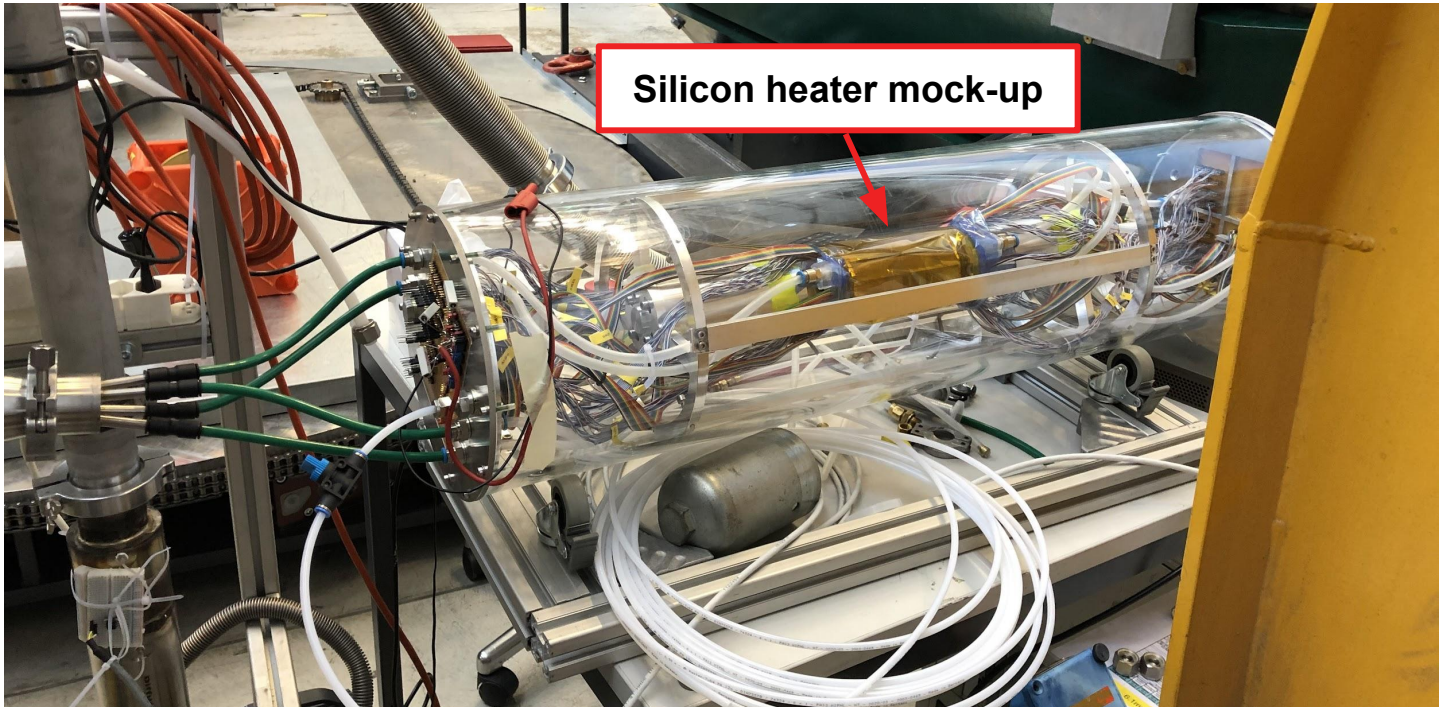
Measurements:

- transient behaviour
- temperature maps
- temperature-to-power relation

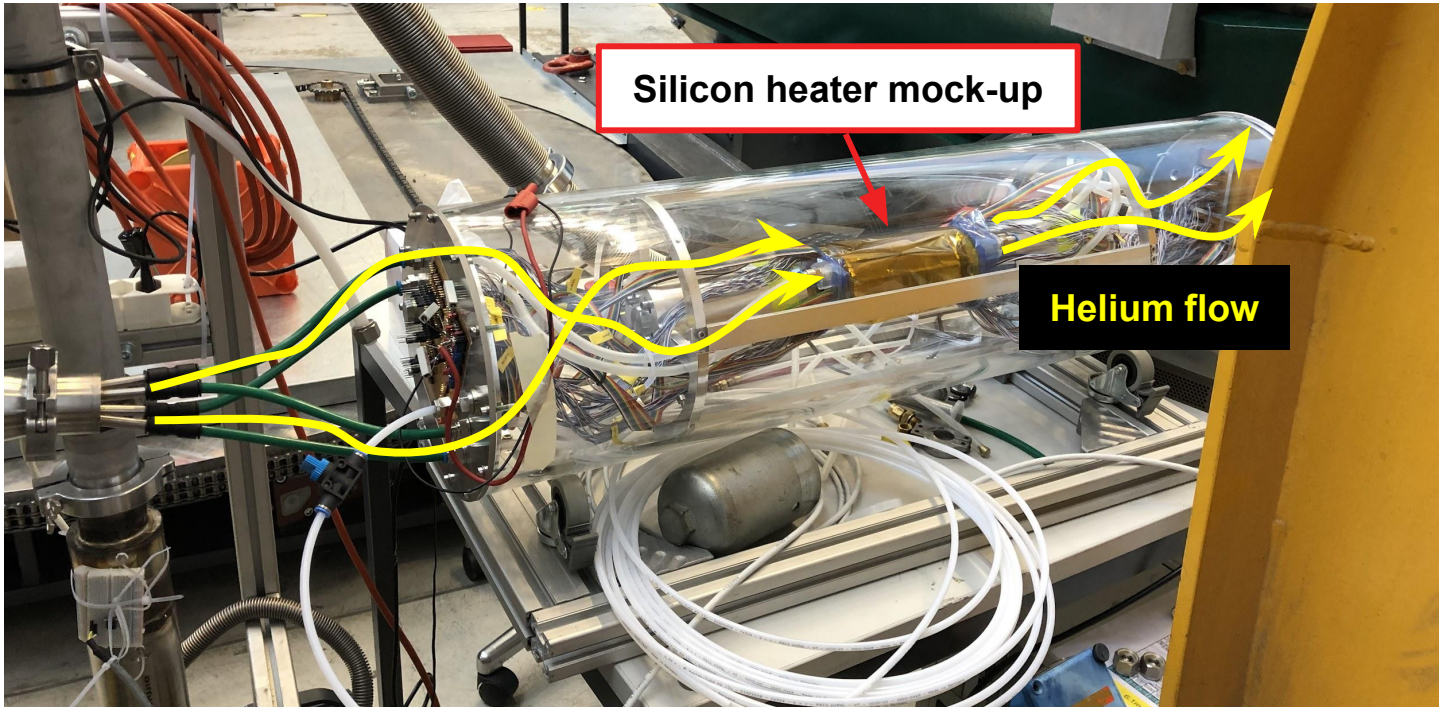


[1] heat dissipation depends on chip temperature, corrections to study uniform heating applied

Cooling setup



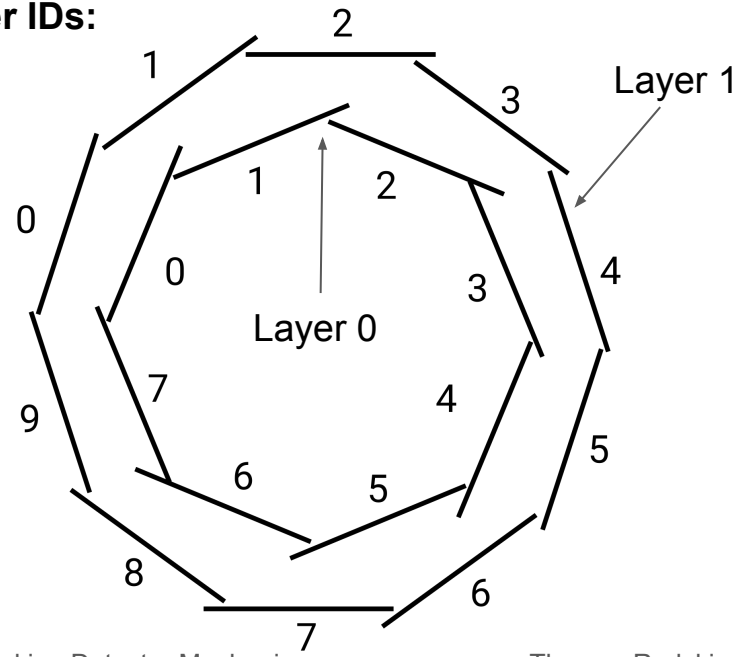
Cooling setup



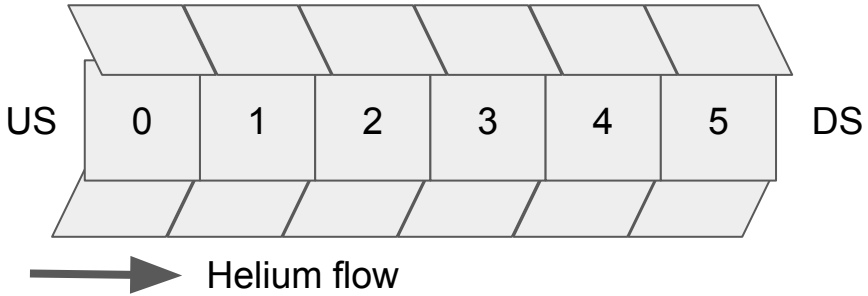
Measurement results

Numbering scheme for temperature maps (next slide)

Ladder IDs:



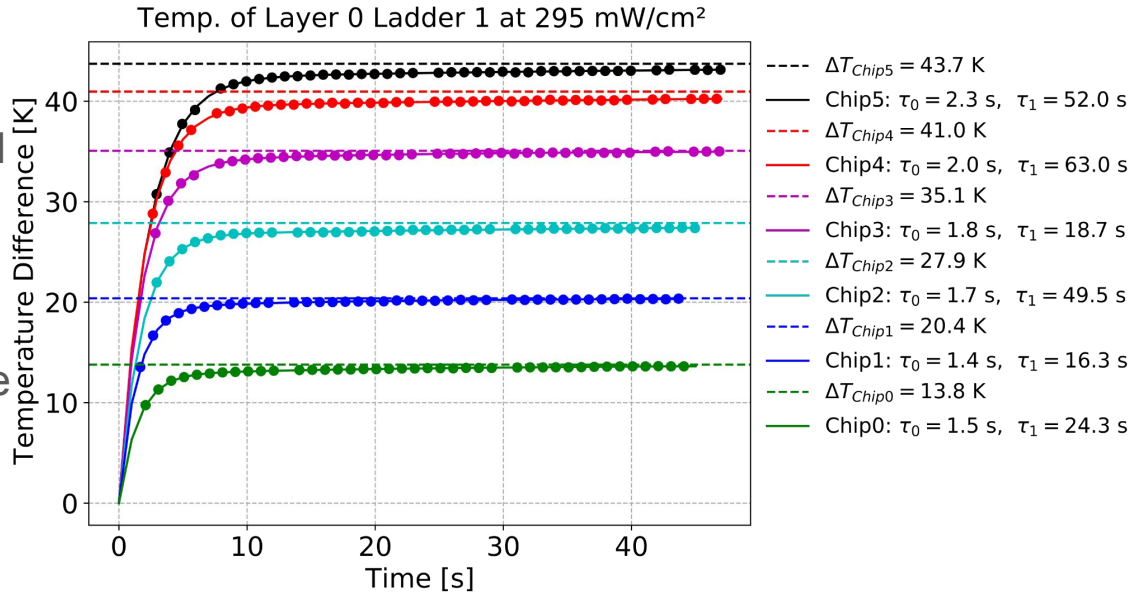
Chip IDs:



Measurement results

Transient behaviour (start-up):

- temperature increase described by 2 time constants τ_0 and τ_1
- τ_0 of 1 to 3 s
- τ_1 of 20 to 60 s
- 90 % of equilibrium temperature reached in less than 5 s
- Cooling needs to run at full speed when powering detector

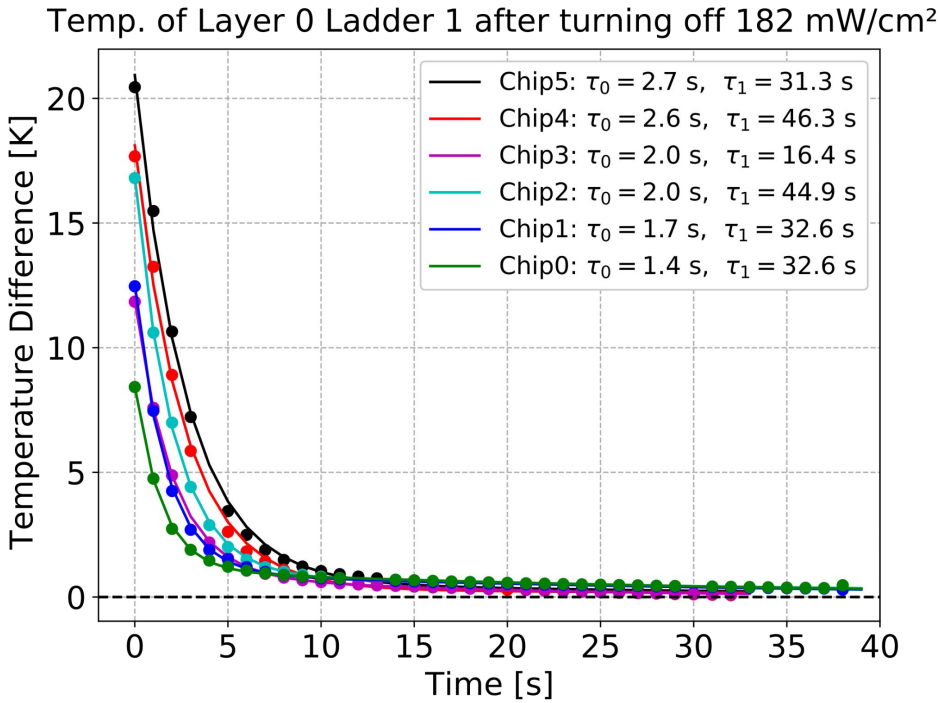


Chip temperature of 1 ladder in Layer 0.
Coldest chip at gas inlet, hottest chip at outlet

Measurement results

Transient behaviour (turning off):

- Simulated emergency shutdown of pixel power
- Similar time constants as for start-up
- T < 5°C in less than 5 s

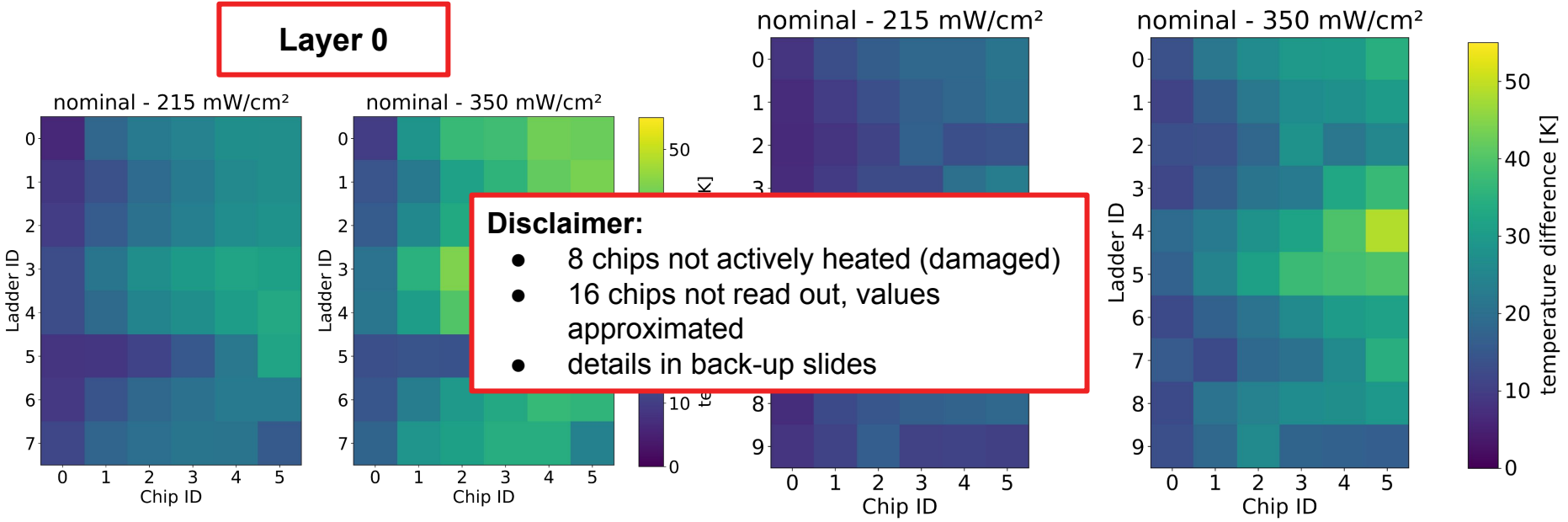


Measurement results

Temperature maps

Layer 0

Layer 1



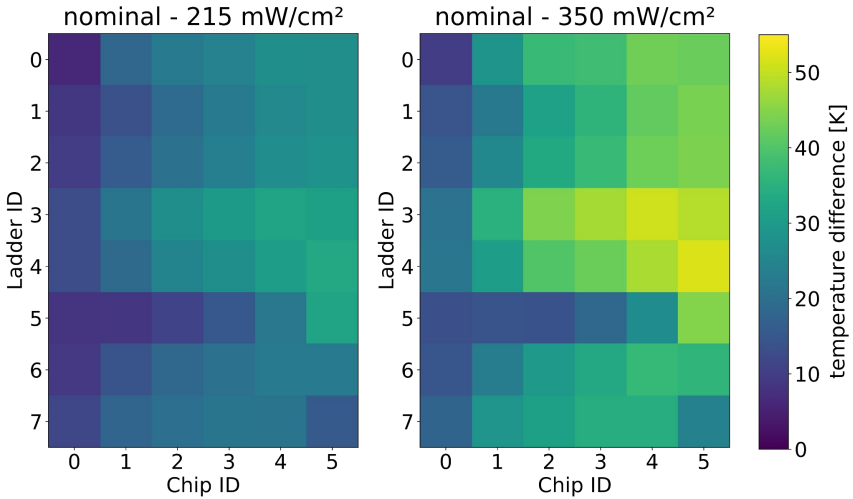
Disclaimer:

- 8 chips not actively heated (damaged)
- 16 chips not read out, values approximated
- details in back-up slides

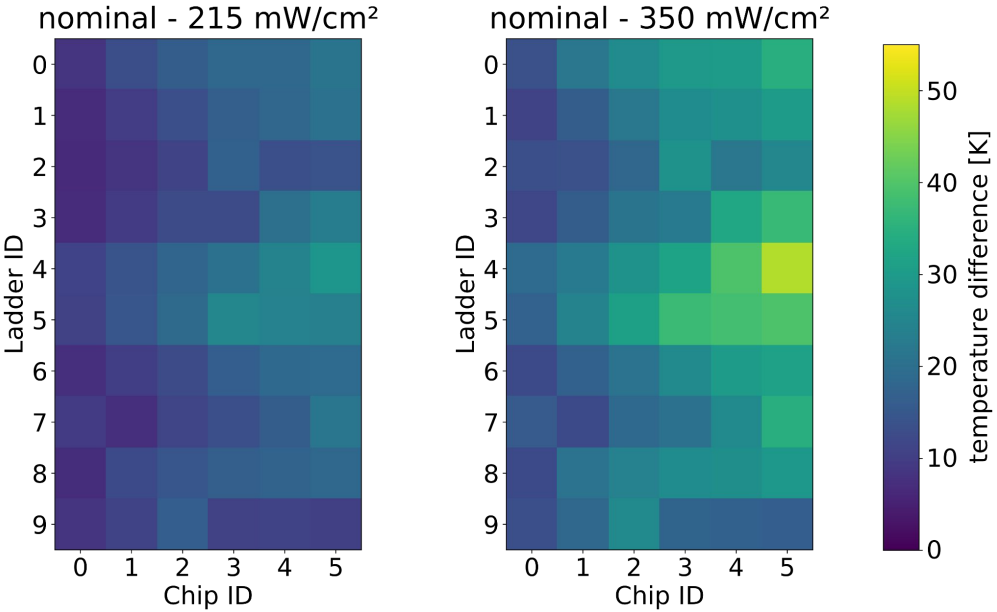
Measurement results

Temperature maps

Layer 0

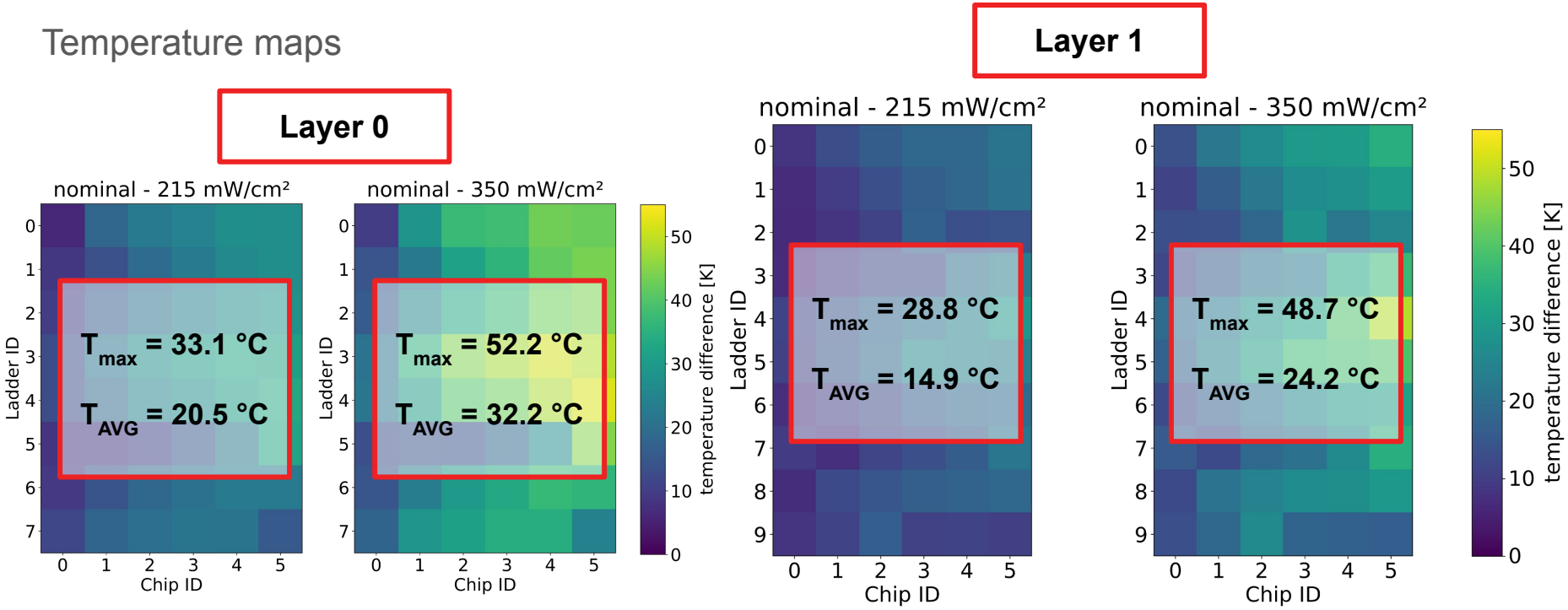


Layer 1



Measurement results

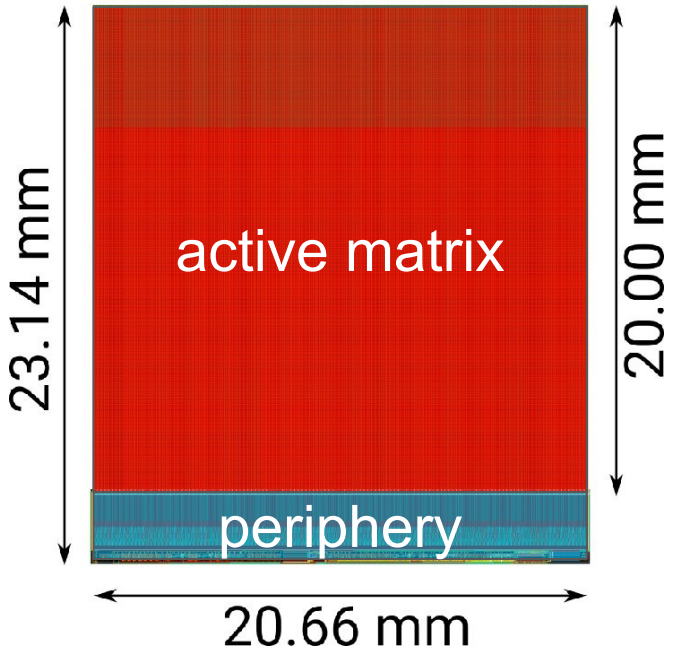
Temperature maps



Measurement results

Temperature maps

- all temperatures < 70°C
- hot area due to flow non-uniformities
- studied uniform heating
  - chip periphery of MuPix sensors will dissipate more heat than active matrix
  - 20°C higher temperatures locally expected
  - just at limit of 70°C
- 2 g/s helium cooling sufficient for Mu3e vertex detector
- at 350 mW/cm² at the edge of specifications



Operation of helium-cooled demonstrator

- Mu3e DAQ tests (“integration run”)
- Simplified PCB-based demonstrator
  - PCB ladders instead of HDIs
  - Full-scale MuPix10 chips
  - wire bonded chips

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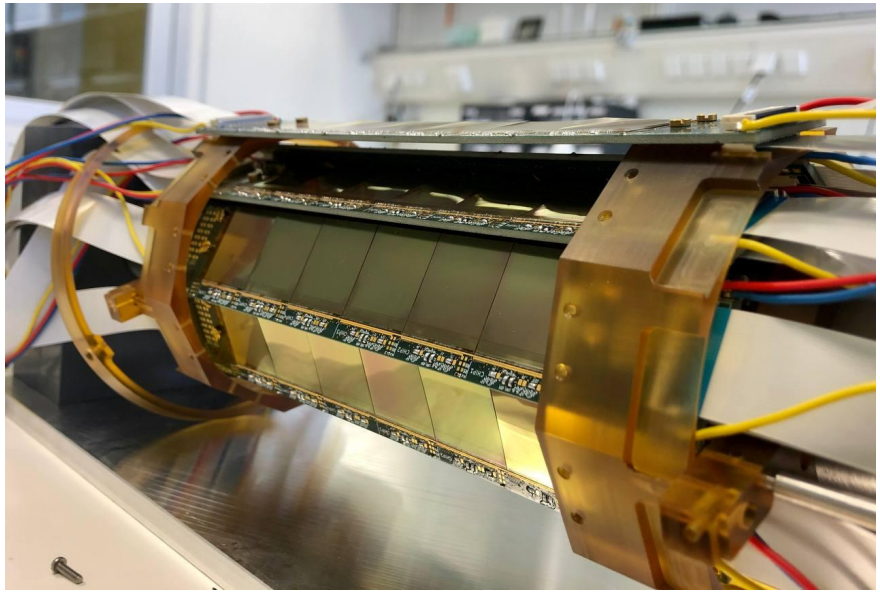
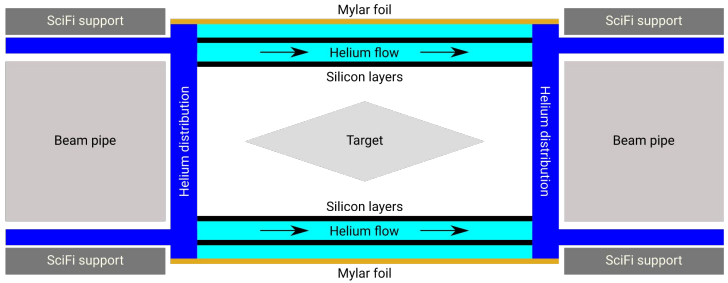


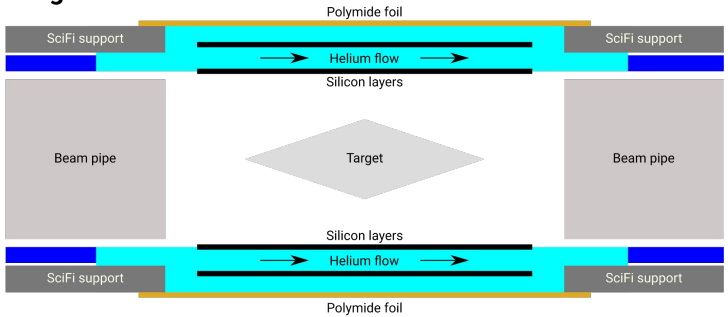
Operation of helium-cooled demonstrator

- Mu3e DAQ tests (“integration run”)
- Simplified PCB-based demonstrator
  - PCB ladders instead of HDIs
  - Full-scale MuPix10 chips
  - wire bonded chips
- Simplified helium distribution

Phase I:

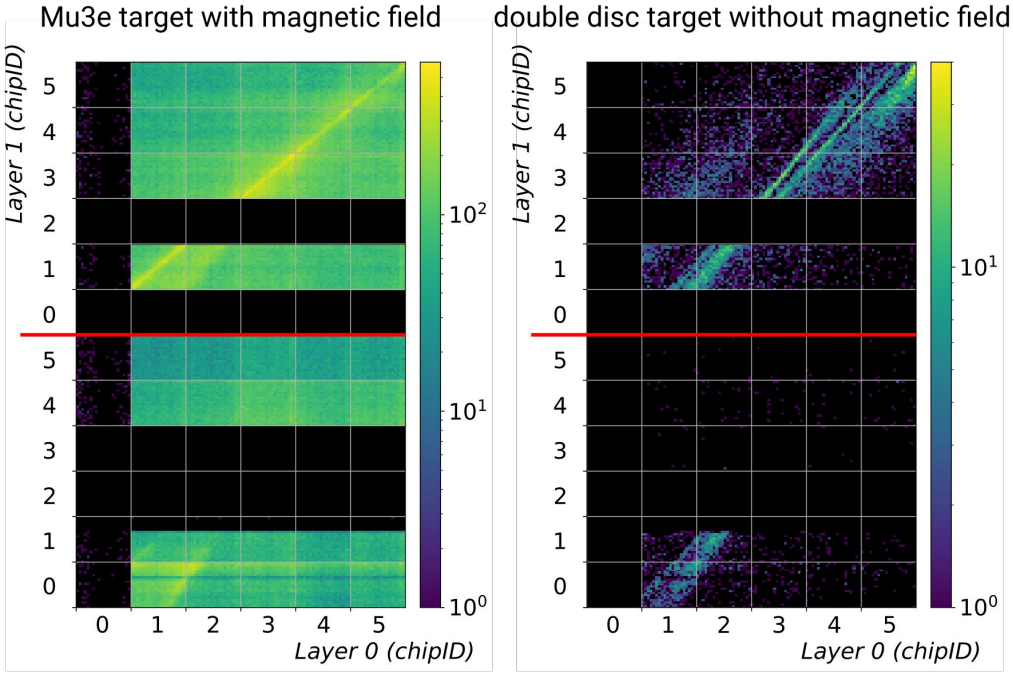


Integration Run:



Operation of helium-cooled demonstrator

- full detector operated
- ~ 100 W heat load cooled away with gaseous helium cooling (2 g/s)
- successful correlation analysis between Layer 0 and Layer 1
- Figures on the right:
  - correlating pixel hits (column address) in L0 and L1 within the same time frame (128 ns)
  - recognize geometrical features of different target configurations



Summary & Outlook

- Cooling concept verified using a detailed thermal-mechanical mock-up ✅
- Successful long-term operation with prototype helium plant (2 g/s) ✅
- First successful demonstration of operating a helium gas cooled pixel detector ✅

- Thermal tests of Mu3e outer pixel layers scheduled for late 2022
- 3x 16 g/s helium systems in production

Gaseous helium as coolant for tracking detectors aiming to minimize material:

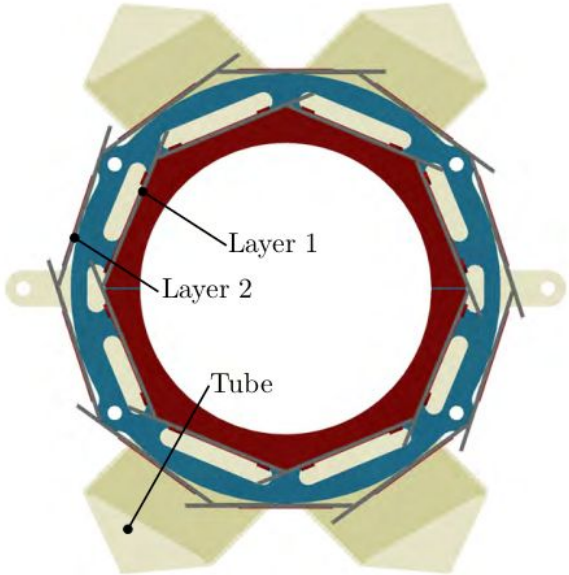
- Material budget of ~ 0.1% per tracking layer possible when using monolithic chips and no additional support for flow channels
- Good thermal properties of helium open the possibility to use fast detectors without integrated liquid cooling systems

Backup

Helium distribution

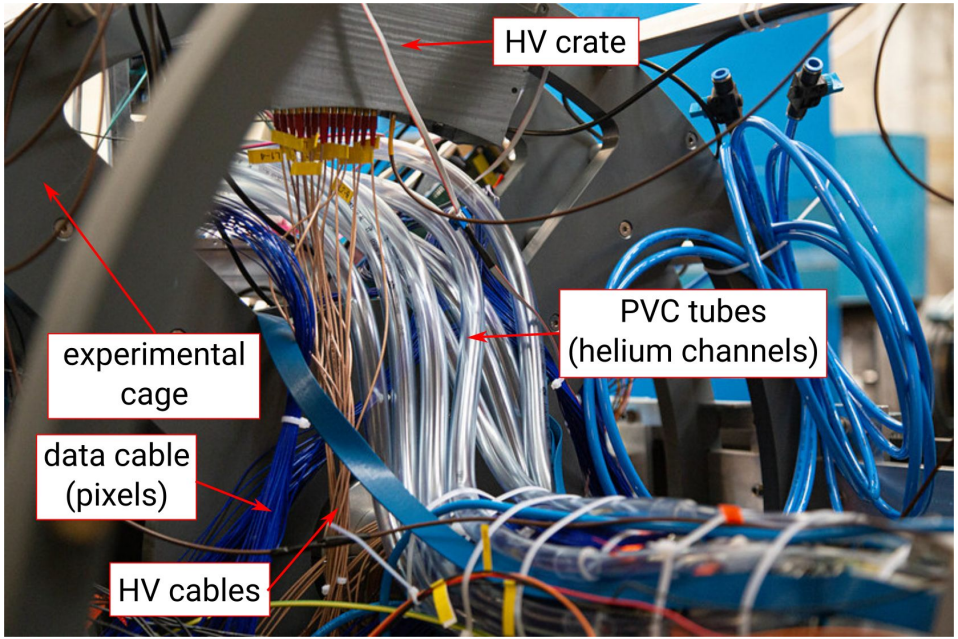
Layer 1 = Layer 0; Layer 2 = Layer 1, distribution for final detector

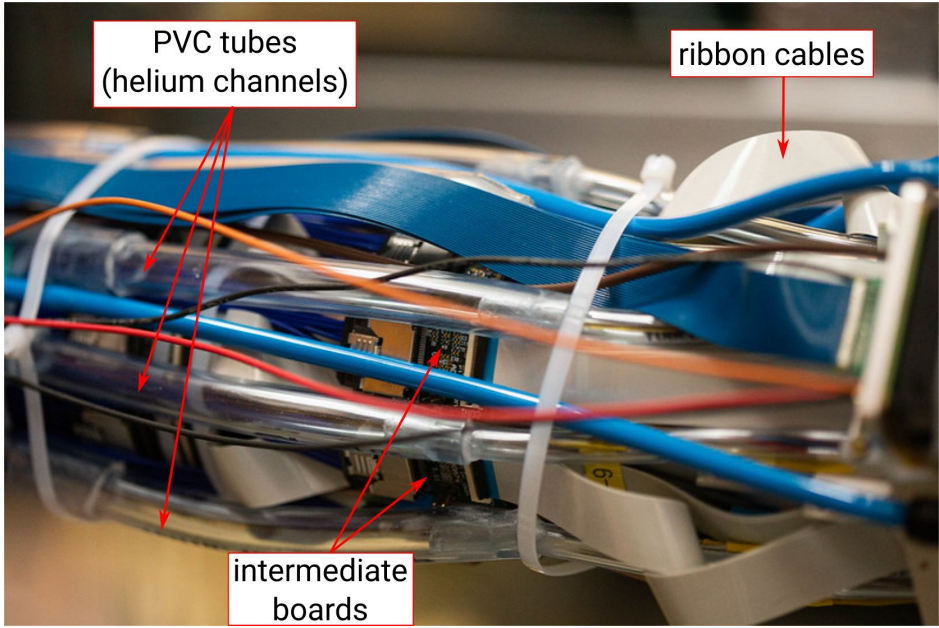
Ducts on beam pipes



Helium distribution

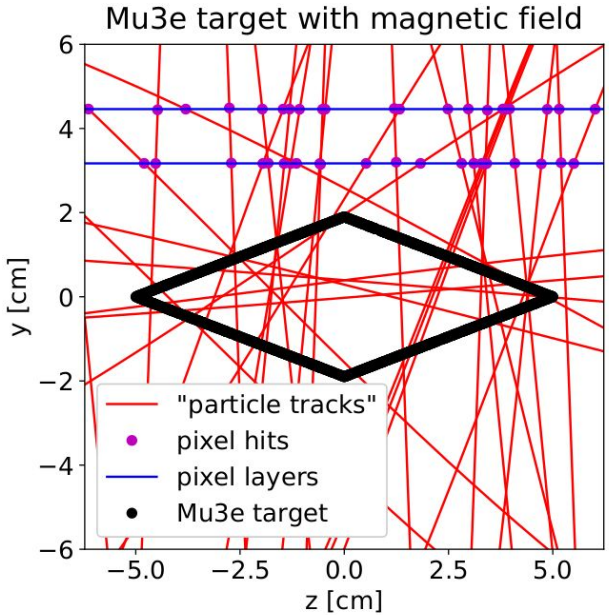
simplified helium channels for demonstrator

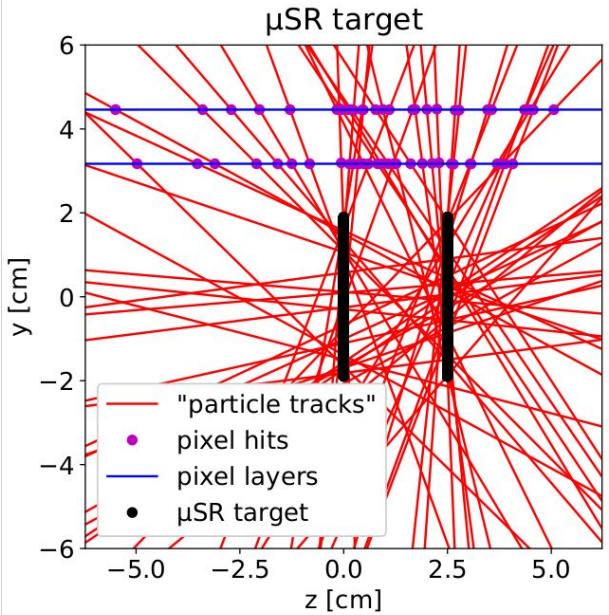




Target configurations - demonstrator

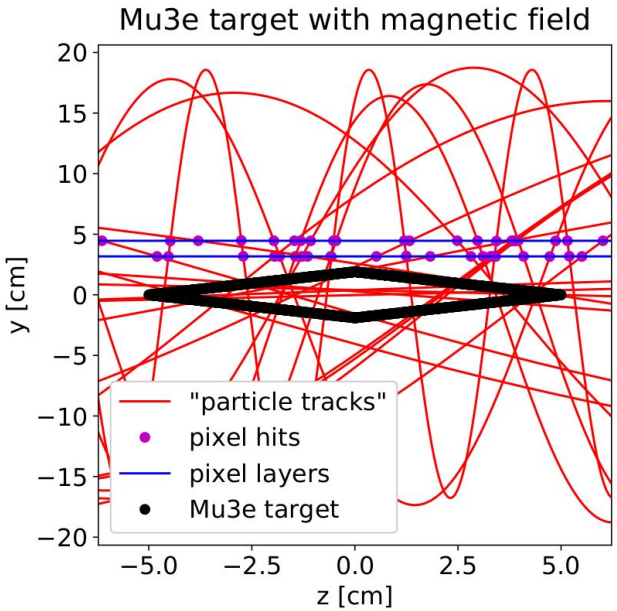
target configurations for the obtained correlation diagrams

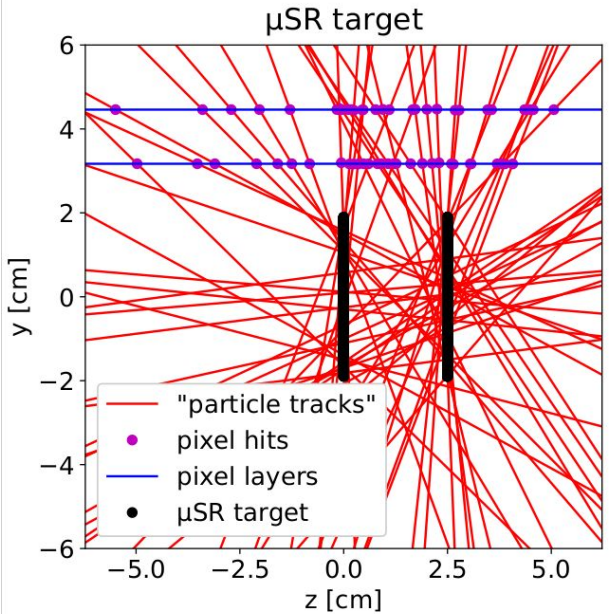




Target configurations - demonstrator

target configurations for the obtained correlation diagrams (Mu3e target zoomed-in)



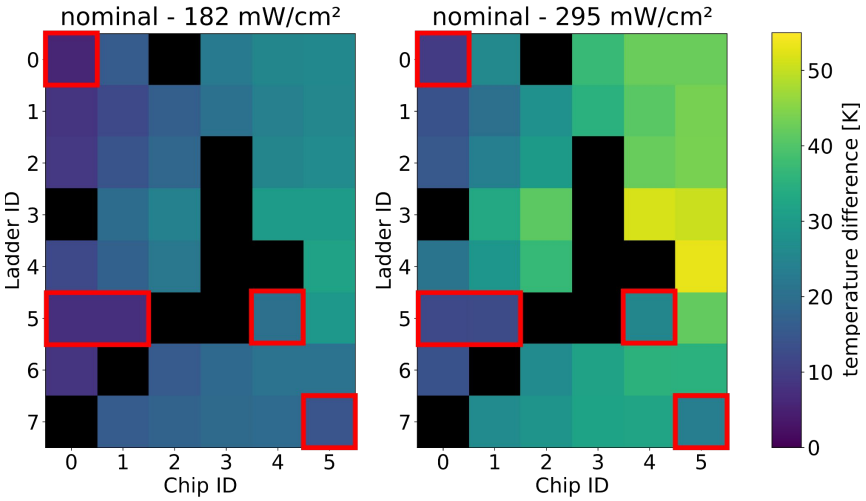


Measurement results

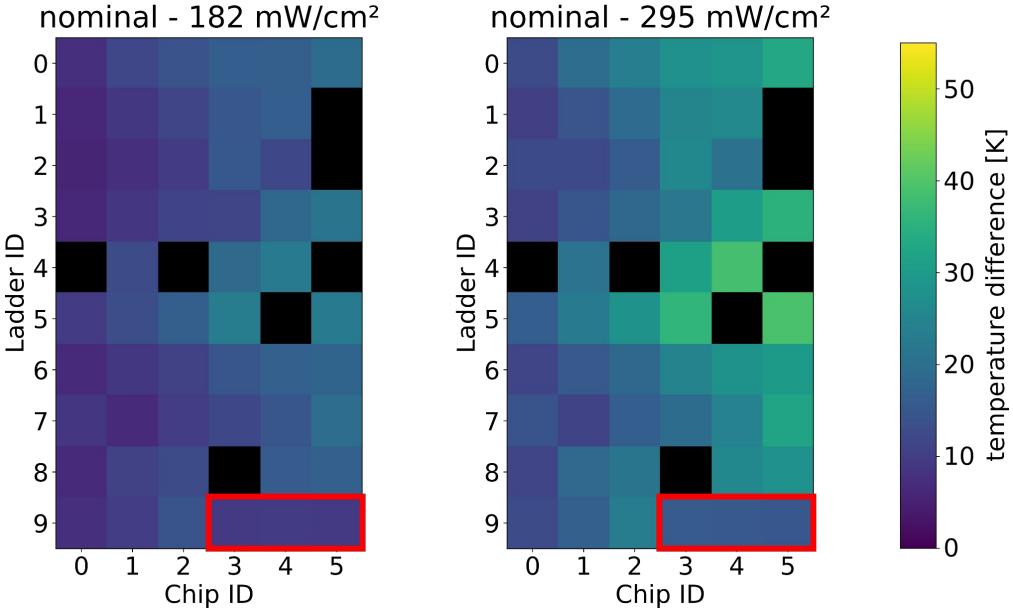
not heated
no readout

Temperature maps (raw data)

Layer 0



Layer 1

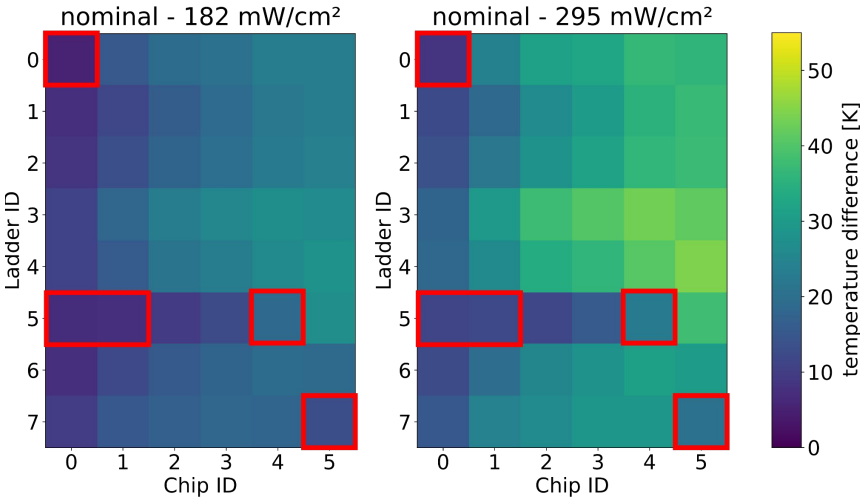


not heated

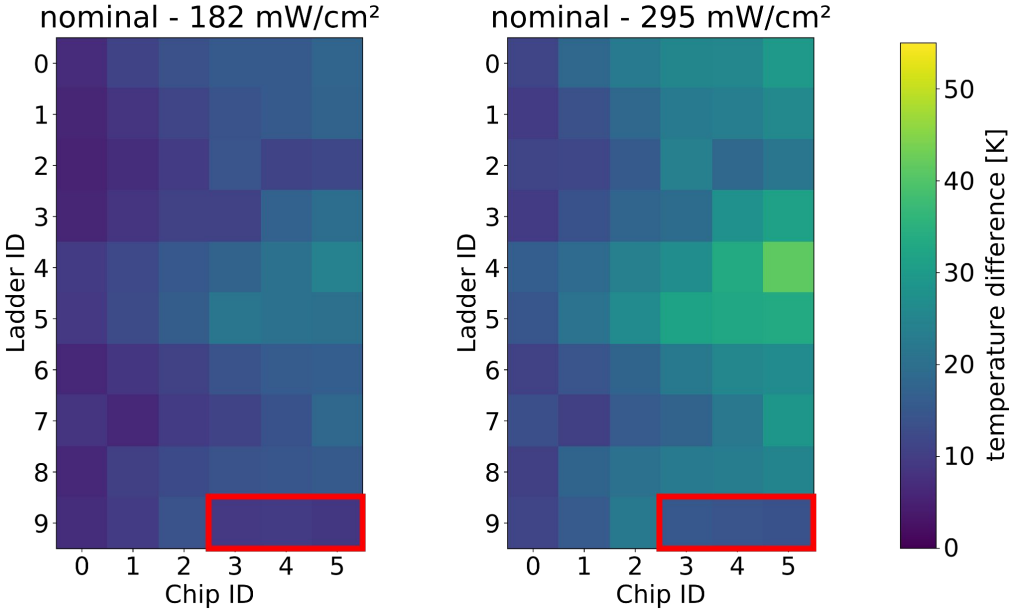
Measurement results

Temperature maps (raw data)

Layer 0

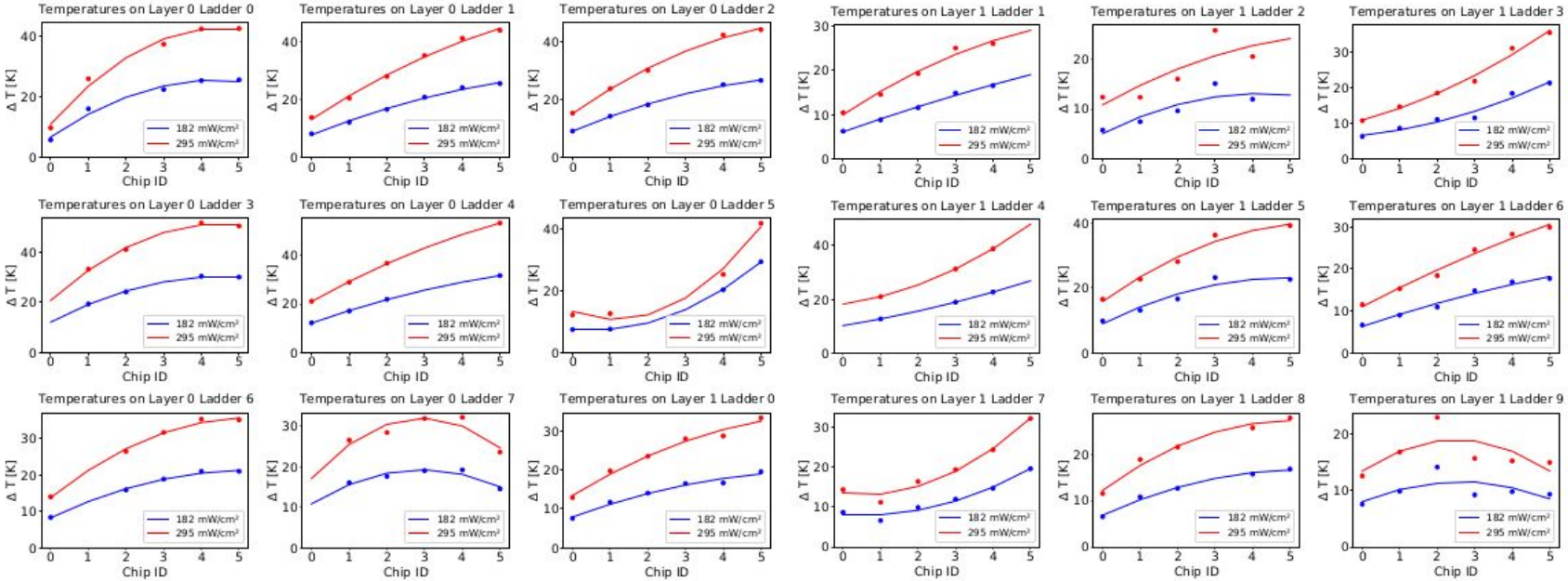


Layer 1



Measurement results

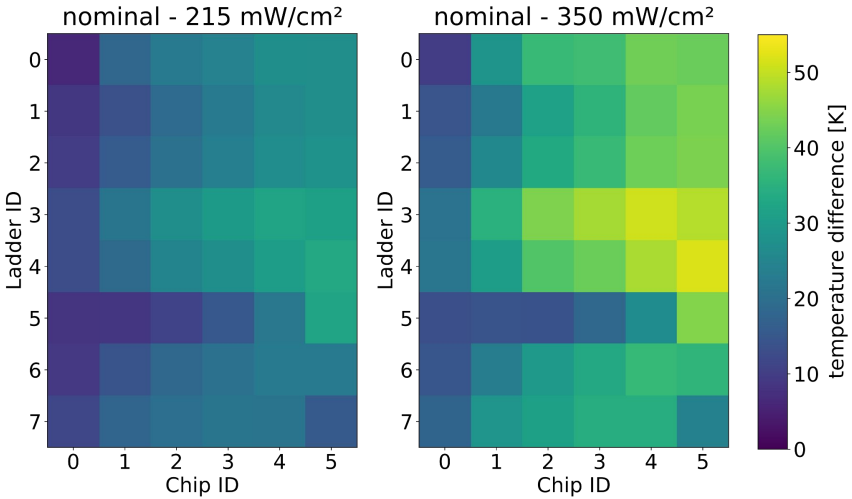
2nd order polynomial approximation of missing temperature readings:



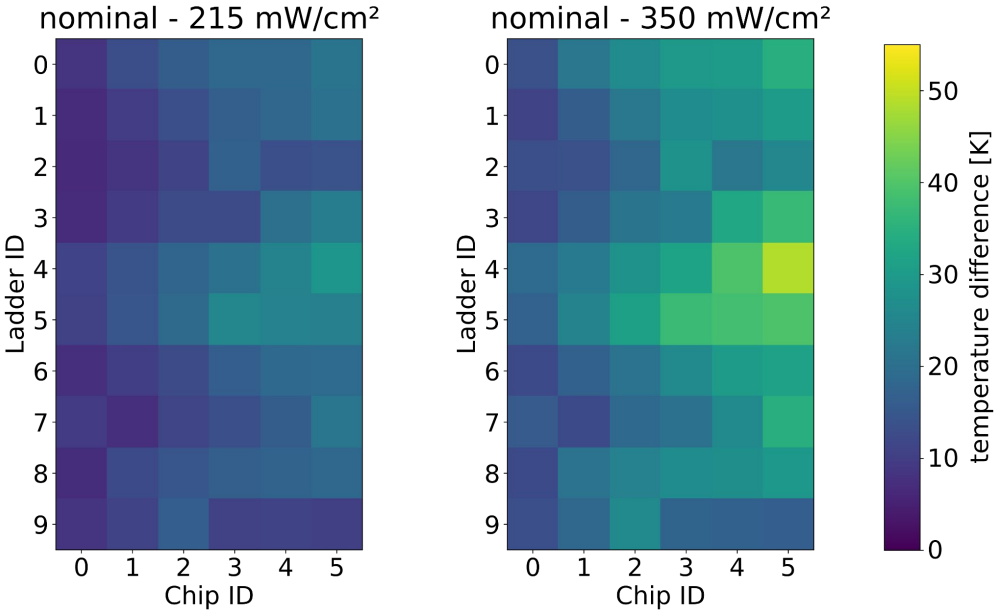
Measurement results

Temperature maps (translated to nominal heat dissipation)

Layer 0



Layer 1



Measurement results

- Translation to different heat dissipation
- Linearity of temperature-to-power relation