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Development of a Quality Control Procedure for MuPix11 Pixel Sensors for the Mu3e Vertex Detector

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Abstract

The Mu3e experiment will search for the charged lepton flavour violating $\mu^+ \to e^+e^-e^+$ decay with an unprecedented single event sensitivity of 10^{-15}. The observation of this decay would be a clear indication of physics beyond the Standard Model. The experiment requires particle detection systems with precise spatial and timing resolutions, which will employ 2844 MuPix11 HV-MAPS. A quality control procedure is necessary to reliably evaluate sensor functionality before their installation into the detector.

The aim of this thesis is to improve the MuPix11 quality control procedure, and investigate common failures. Multiple tests were carried out in the context of the Mu3e vertex detector pre-production, on sensors of both 50 µm and 70 µm thickness, as both are candidates for the final detector. The information gained is used to amend the quality control tests, in order to improve the yield by reducing testing errors, and the procedure is extended to investigate failure causes in detail. The improved quality control procedure shows a more effective evaluation and a reduction in errors during testing. The final quality control yield for 70 µm sensors is 66%. The 50 µm yield was systematically limited by external effects on the testing setup.

Zusammenfassung

Das Mu3e Experiment wird den geladene leptonfamilienzahl-verletzenden $\mu^+ \to e^+e^-e^+$ Zerfall mit einer beispiellosen Einzelereignisempfindlichkeit von 10^{-15} suchen. Die Beobachtung dieses Zerfalls wäre ein klarer Hinweis auf eine Physik jenseits des Standardmodells. Das Experiment erfordert Detektorsysteme mit präzisen Orts- und Zeitauflösungen, welche 2844 MuPix11 HV-MAPS einsetzen werden. Eine Qualitätskontrolle ist notwendig, um die Funktionalität der Sensoren vor dem Einbau im Detektor zu verifizieren.

Ziel dieser Arbeit ist es, das MuPix11 Qualitätskontrollverfahren zu verbessern, und häufige Fehlerquellen zu untersuchen. Mehrere Tests wurden im Rahmen der Vorproduktion des Mu3e-Vertexdetektors durchgeführt, für Sensoren mit einer Dicke von 50 µm und 70 µm, da beide für die Installation im Detektor in Frage kommen. Die gewonnenen Informationen werden genutzt um die Qualitätskontrolle zu verbessern und Bewertungsfehler zu reduzieren, sowie die Tests zur Untersuchung häufiger Fehlerursachen zu erweitern. Mit Hilfe der verbesserten Qualitätskontrolle lassen sich die Sensoren effektiv bewerten und Fehler während den Tests reduzieren. Die Ausbeute der Qualitätskontrolle für 70 µm Sensoren betrug 66%. Die Ausbeute for 50 µm Sensoren wurde durch externe Effekte systematisch verringert.

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Chapter 1

Introduction

Particle physics describes matter at the most elementary level. Understanding of fundamental structures started showing progress towards the turn of the 20th century [1]. The last hundred years have seen the field progress from two known fundamental particles to seventeen [2], along with their categorisation, observation, and precise mathematical descriptions. The Standard Model is a summary of our knowledge of elementary particles and their interactions. It explains, quantifies and predicts the behaviour of matter and processes at the most elementary level. However, while remarkably comprehensive and successful in many predictions, it remains incomplete.

The Mu3e experiment is currently under construction at the Paul Scherrer Institute in Switzerland. It will search for the charged lepton flavour violating decay $\mu^+ \to e^+e^-e^+$ with an unprecedented single event sensitivity of 10^{-15} in Phase I [3][4]. The aim is to either confirm the decay, or set the upper limit for the branching ratio to 10^{-15} with a confidence level of 90%. The information on the branching ratio for this decay will improve our understanding of the Standard Model. The challenges of searching for such a decay require particle detection systems with precise spatial and timing resolutions, which are made possible by the MuPix11 HV-MAPS. The innovative technology introduces new possibilities for a low material pixel tracker. The monolithic design is essential for improving the momentum resolution to a level at which the single event sensitivity target of 10^{-15} can be achieved. Successful particle detection at Mu3e depends on the functionality of these sensors, so each must pass a Quality Control (QC) procedure before its installation.

The object of this thesis is the improvement of the quality control concept for MuPix11 sensors, and the investigation of frequent failure modes. The aim is to define a testing scheme which accurately evaluates the functionality of the sensors, and their ability to fulfil the operational demands of the experiment. The tests are carried out in the context of vertex detector pre-production, which allows the expansion of the testing procedures to gain more information on failure modes. This can help identify systematic testing errors, and guide the improvement of the testing scheme.

This thesis presents quality control results for sensors of 50 µm and 70 µm thickness. It will show that the sensor thickness has an affect on some sensor functions, such as the depletion process. The improved quality control procedure demonstrates an improved yield for 70 µm sensors, as errors in the testing procedure were reduced. The total quality control yield for 50 µm sensors is lower than for 70 µm, which should be considered in the planning of the production phase quality control. However, 50 µm yield is systematically limited by external factors, and is expected to increase significantly when this is corrected.

Chapter 2
Physics Motivation

The Standard Model summarises our knowledge of elementary particles and their interactions. Despite its success, the model presents limitations. The search for charged lepton flavour violation is an avenue of research with the potential to expand the standard model towards new physics.

2.1 The Standard Model of Particle Physics

The Standard Model of particle physics is a quantum field theory [5] that was developed in the second half of the twentieth century. The Standard Model categorises the elementary particles, as is visualised in Figure 1. Particles are categorised into bosons and fermions according to their spins [6]. Bosons, with integer spins, carry interactions between particles, so their characteristics define particle behaviour. The Higgs boson gives particles the property of mass, while the four gauge bosons carry the fundamental forces.

Fermions have half- integer spins. They are grouped into three generations, as is shown in Figure 1. The first generation is stable, and are the constituents of ordinary matter. Particles of later generations increase in mass. Due to their instability, later generations can only be observed in high energy collisions, or in the form of cosmic rays.

Fermions are divided into quarks and leptons. Quarks have charges of $+\frac{2}{3}\mathrm{e}$ or $-\frac{1}{3}\,\mathrm{e}$ and carry colour charge, allowing them to interact with the strong force. Each generation of leptons consists of a pair of the same flavour. Each pair contains a particle carrying an electric charge of - e, and its corresponding neutrino, which is neutral.

For every fermion in the Standard Model, we observe a corresponding anti-particle, which carries the opposite charge, but otherwise shows the same properties.

While all fermions interact with the weak force, only quarks and charged leptons interact electromagnetically, and only quarks experience the strong force. The strong force is carried by gluons, the electromagnetic force by photons, and the weak force by the W^+, W^- and Z bosons.

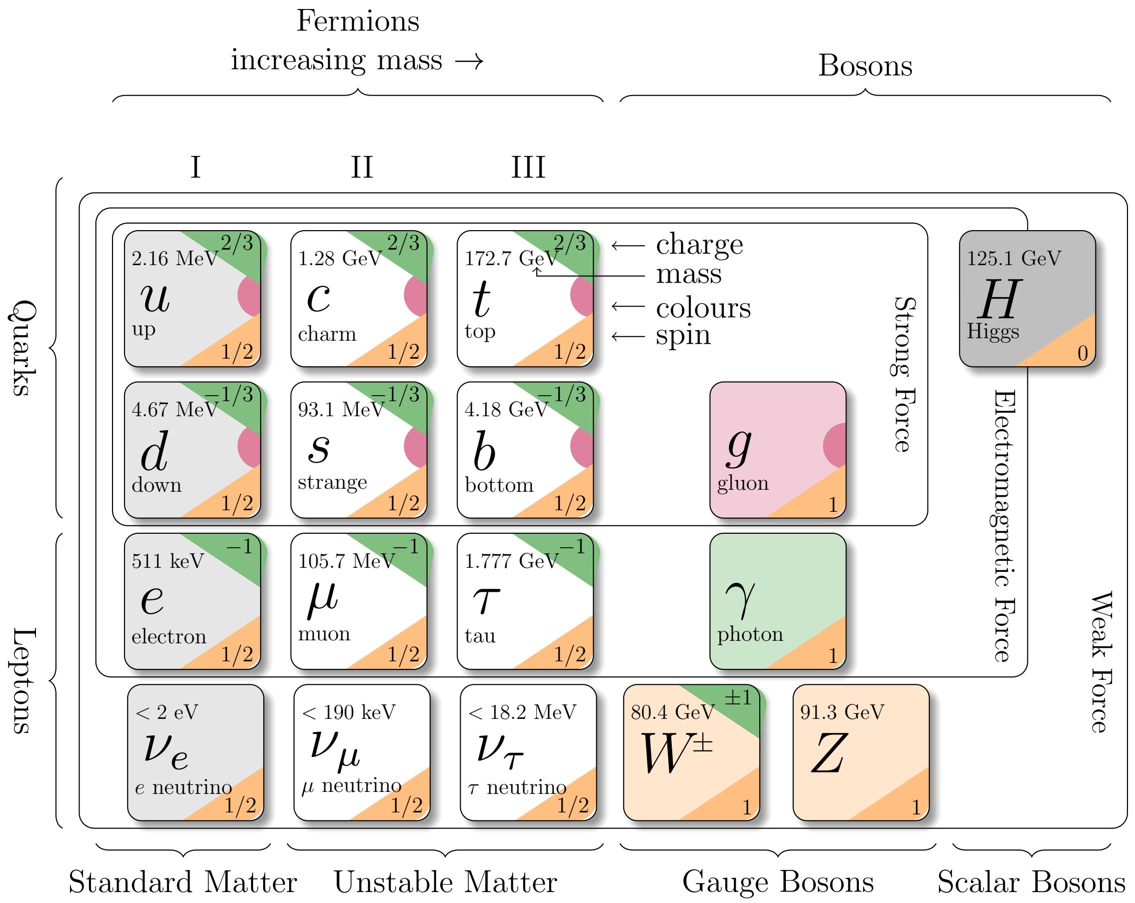
Fermions
increasing mass →
Bosons
I
II
III
Quarks
Leptons
2.16 MeV
2/3
u
up
1/2
1.28 GeV
2/3
c
charm
1/2
172.7 GeV
2/3
t
top
1/2
← charge
mass
← colours
← spin
Strong Force
125.1 GeV
H
Higgs
0
4.67 MeV
−1/3
d
down
1/2
93.1 MeV
−1/3
s
strange
1/2
4.18 GeV
−1/3
b
bottom
1/2
g
gluon
1
Electromagnetic Force
511 keV
−1
e
electron
1/2
105.7 MeV
−1
μ
muon
1/2
1.777 GeV
−1
τ
tau
1/2
γ
photon
1
Weak Force
< 2 eV
ν_e
e neutrino
1/2
< 190 keV
ν_μ
μ neutrino
1/2
< 18.2 MeV
ν_τ
τ neutrino
1/2
80.4 GeV
±1
W±
1
91.3 GeV
Z
1
Standard Matter
Unstable Matter
Gauge Bosons
Scalar Bosons

Figure 1: Visualisation of the Standard Model. Modified from [7], with values taken from [8].

The ability to predict particles and their qualities with remarkable accuracy is one of the great successes of the Standard Model. With the discovery of the Higgs boson in 2012 [9][10], every particle prediction made by the Standard Model has now been confirmed [5].

In addition, the predictions made by the Standard Model are remarkably precise. The predicted magnetic moment of the electron, for example, was experimentally confirmed to a precision of 10^{-12} [11][8].

2.2 Limitations of the Standard Model

The Standard Model has proven successful, but there are certain limitations.

For instance, it only incorporates three out of the four fundamental forces. The modern description of gravity, general relativity, cannot be reconciled with the quantum mechanical description of matter at the fundamental level. The attempt to combine the two theories leads to unsolved contradictions [6].

Furthermore, the model requires at least 19[1] fundamental constants, which are well defined, but arbitrary. Key qualities, such as particle masses and interaction parameters cannot be explained theoretically, which indicates that there could be more to these systems than the Standard Model describes.

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[1] This number increases if we consider neutrino oscillations and masses [12].

In addition, the Standard Model fails to provide an answer for the nature of dark matter. Due to the gravitational force, the amount and distribution of matter present in our universe influences the dynamics of surrounding systems. The matter required to provide sufficient gravitational attraction to balance the velocity of systems on stellar and galactic scales is much larger than the amount of matter we actually observe [13][14]. The continued stability of such systems is evidence for the presence of matter which interacts with gravity but not the electromagnetic force, and is therefore not directly observable. The explanation for the unprecedented interactive behaviour of this dark matter should lie in its particle nature, and therefore a complete model of particle physics would explain this observation.

Finding possible amendments and extensions of the Standard Model is a key interest of modern particle physics. One promising avenue of research is the search for Lepton Flavour Violation (LFV).

2.3 Searching for Lepton Flavour Violation

Every symmetry in a physical system of conservative forces naturally leads to the conservation of a physical quantity [15]. In the Standard Model, most of the conserved quantities are derived from a symmetry. However, Lepton flavour conservation is an accidental conservation law. It is based only on experimental observations. Without the foundation of a fundamental symmetry, lepton flavour conservation can be broken without the violation of physical laws. Lepton Flavour Violation (LFV) therefore presents a unique opportunity for observing new physics. LFV has already been confirmed for neutral particles, through the observation of neutrino oscillations [16][17][18]. The search for charged Lepton Flavour Violation (cLFV) is seen as one of the most promising investigations into the formulation of the Standard Model.

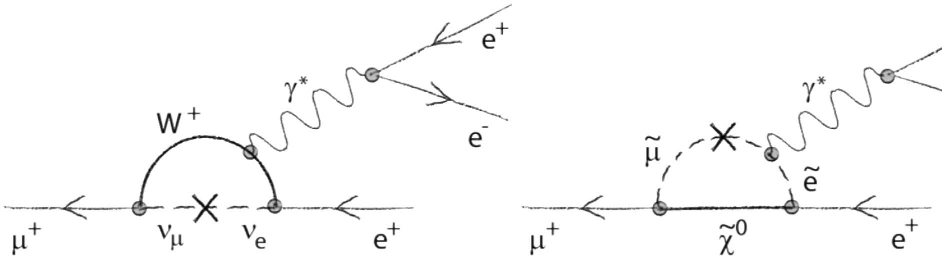
Chapter 3

The Mu3e Experiment

The Mu3e experiment is currently under construction at the Paul Scherrer Institute in Switzerland. It will search for cLFV in the form of the $\mu^+ \rightarrow e^+e^-e^+$ decay., with the aim of either observing it, or setting the upper limit for the branching ratio to 10^{-15} with a confidence level of 90%.

3.1 The $\mu^+ \rightarrow e^+e^-e^+$ Decay

The $\mu^+ \rightarrow e^+e^-e^+$ decay presents a possibility for observation of charged lepton flavour violation [4]. This decay is permitted by Beyond the Standard Model (BSM) theories which include neutrino oscillations, as shown in Figure 2a. However, the large difference in mass between the heavy W^+ Boson and the two neutrinos in the loop, and the loop-internal neutrino oscillation, lower the branching fraction of this decay avenue to $<<$ 10^{-50} [4]. This branching fraction is not observable. Therefore, the decay is effectively suppressed under the Standard Model.



(a) Decay under BSM theories

(b) Decay under SUSY

Figure 2: Feynman diagrams of a muon decay to three electrons via (a) The Standard Model with neutrino oscillation and (b) Slepton mixing according to SUSY [19].

Many models beyond the Standard Model naturally allow cLFV, such as supersymmetry, as shown in Figure 2b. The observation of the $\mu^+ \rightarrow e^+e^-e^+$ decay would be direct evidence of such mechanisms taking place. The Standard Model could then be extended to include these behaviours, improving its description of the universe at the particle level.

3.2 The Experimental Concept

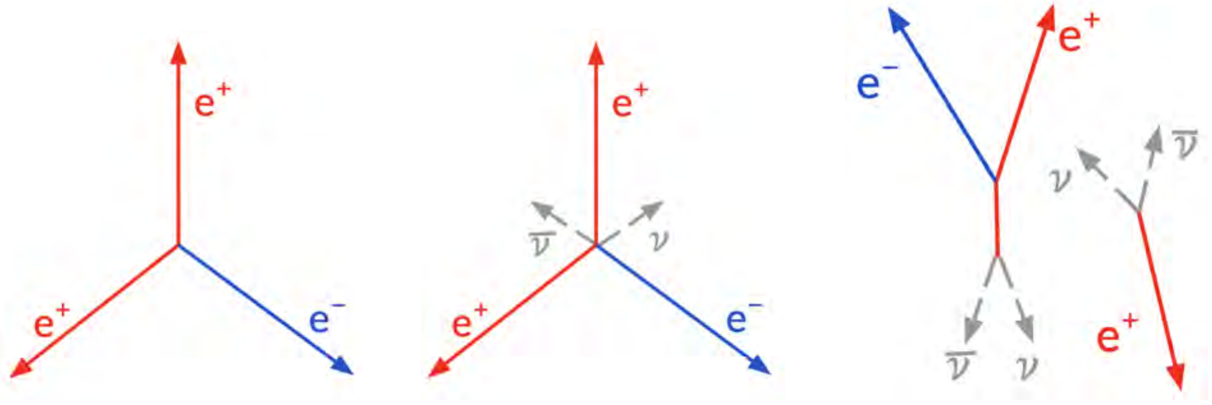
The Mu3e experiment consists of a low energy beam of muons, which are stopped by a target inside the Mu3e detector [20]. The stationary muons then decay, and the charged decay products are observed. The low branching fraction of the $\mu^+ \rightarrow e^+e^-e^+$ decay introduces specific challenges for its detection. A very large number of events must be observed and processed. The first challenge is gaining the needed statistics to observe the decay. This includes generation of a sufficient decay rate, as well as the creation of a suitably fast and efficient detection system.

If the $\mu^+ \rightarrow e^+e^-e^+$ decay occurs at the smallest branching fraction that is experimentally observable with the Mu3e design, 10^{-15}, it would require the observation of 10^{16} muons to either confirm the decay, or set the upper limit for the branching ratio to 10^{-15} with a confidence level of 90%. The observation of this large number of decays is to be achieved through high intensity muon beams, and sensors with an efficiency target of $\geq 99\%$. The experiment will operate in two phases [20]. Phase I will operate with the μE5 beamline, with a rate of 10^8 muons per second. Phase II is intended to improve on this decay rate with a new High Intensity Muon Beam (HIMB), currently in planning at PSI.

This large rate of observed decays leads to new challenges, as it creates a background many orders of magnitude larger than the decay signal itself. To remove the background, each observed decay must be analysed and assigned to the responsible process. The two main background processes are background from radiative muon decay, and from accidental coincidences.

3.2.1 Background from Accidental Coincidences

Background from accidental coincidences will be the most frequently observed signal in the Mu3e experiment [20].



(a) The $\mu^+ \rightarrow e^+e^-e^+$ decay

(b) The radiative muon decay

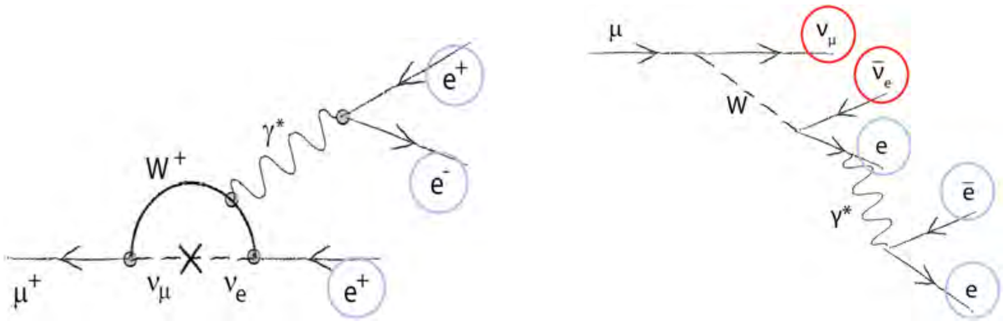
(c) An example of accidental coincidence

Figure 3: Topologies of a) $\mu^+ \rightarrow e^+e^-e^+$ decay, and b) and c), the most common backgrounds [20].

Accidental coincidences consist of two Michel decays ($\mu^- \to \bar{\nu}_e + \nu_\mu + e^-$) and an external electron, from a radiative decay or Bhabha scattering within the detector. These coincide to look like the $\mu^+ \to e^+e^-e^+$ signal. With a branching fraction close to 1, the Michel decay is 10^{16} times as frequent than the best case scenario for $\mu^+ \to e^+e^-e^+$. The accidental coincides will not be as frequent, but are still expected to be several orders of magnitude more frequent than the $\mu^+ \to e^+e^-e^+$ decay.
The topologies of the $\mu^+ \to e^+e^-e^+$ decay and the two main backgrounds are shown in Figure 3. The Mu3e detector detects only the electrons and positrons. Accidentally coinciding particles will not share a common vertex, as shown in Figure 3c, as they did not originate from the same process. The tracks generated by the $\mu^+ \to e^+e^-e^+$ decay, however, do have a common origin, see Figure 3a. The accurate resolution of this common origin relies on good timing and vertex resolutions, as listed in Table 3.1. The vertex resolution requires track reconstruction, which assigns hits to an event.

3.2.2 Background from Radiative Decay

Radiative decay is the leading order muon decay, $\mu^- \to \bar{\nu}_e + \nu_\mu + e^- + \gamma$ [20]. This can be mistaken for the $\mu^+ \to e^+e^-e^+$ decay if internal conversion takes place ($\mu \to \bar{\nu}_e + \nu_\mu + e^- + e^+ + e^-$), as the two processes have the same number of electron-type decay products. It will be the second most common process observed by the Mu3e detector. With a branching fraction of 10^{-5}, it is still 10^{11} times more frequent than the smallest observable branching fraction for $\mu^+ \to e^+e^-e^+$. The radiative decay cannot be differentiated from the $\mu^+ \to e^+e^-e^+$ decay by track reconstruction because the tracks for both decays converge to a common origin, see Figure 3. Instead, they can be differentiated by the momenta of the observed decay products. The Feynman diagrams of the $\mu^+ \to e^+e^-e^+$ decay and radiative background are shown in Figure 4.



(a) A muon decay to three electrons (b) A radiative muon decay

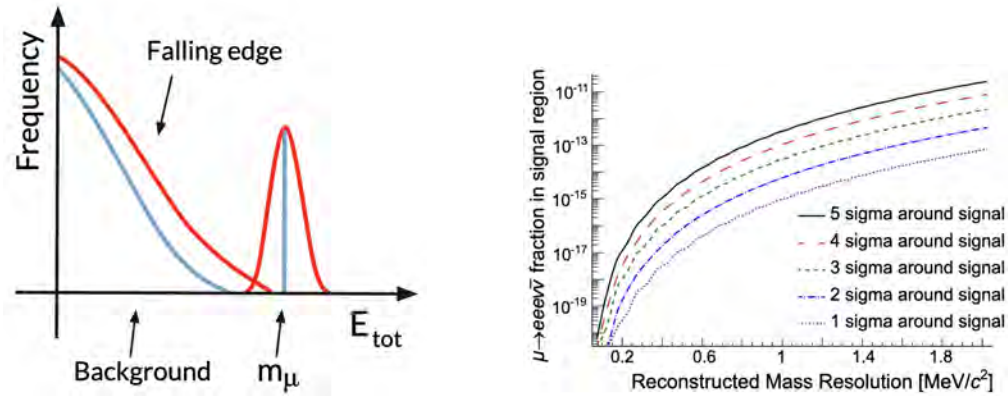
Figure 4: Feynman diagrams of (a) a muon decay to three electrons, and (b), the radiative background [19].

$$E_{tot} = \sum_{i=0}^{3} E_i = m_\mu \qquad |\rho_{tot}| = \sum_{i=0}^{3} \rho_i = 0 \tag{3.1}$$

$$E_{tot} = \sum_{i=0}^{3} E_i = m_\mu - E_{missing} \qquad |\rho_{tot}| = \sum_{i=0}^{3} \rho_i \neq 0 \tag{3.2}$$

For the muon decay to three electrons, Figure 4a, the total energy of the observed decay products is the muon mass, see Equation (3.1). This is because of energy conservation: the muons decay at rest, and all three decay products are electrons or positrons, and therefore observed by the detector. It must therefore be ensured that the muons decay at rest in the detector for a successful background identification. If the muons did not decay at rest, the kinetic energy before the decay would have to be very well defined, which would require a pre-decay detection concept.

The radiative background also has a total energy of the muon mass for all decay products, but the two neutrinos generated along with the three electrons are not observed. This means that the total energy of all observed particles is less than the muon mass by the energy carried by the neutrinos. This decay is visualised in Figure 4b, and the energy and momentum relations are given in Equation (3.2). Both the background and $\mu^+ \rightarrow e^+e^-e^+$ signals have uncertainties which must be reduced to limit the overlap of the signals and allow the signal to be separated from the background. The curves shown in Figure 5b show how a higher mass resolution reduces the branching fraction of radiative decay in the signal region.



(a) Distribution of total energies of decay products measured in the Mu3e detector, not to scale.

(b) Branching fraction of radiative background in signal region against mass resolution [20].

Figure 5: The dependence of signal identification on the momentum resolution.

To observe the $\mu^+ \rightarrow e^+e^-e^+$ decay at a branching fraction of 10^{-15}, the branching fraction for radiative decay should be reduced to an order of magnitude of $\leq 10^{-16}$ in the signal region. The momentum resolution required for this is derived from the 1σ curve in Figure 5b and shown in Table 3.1:

Background	Requirement	Target
Accidental Coincidences	Vertex Resolution	$\leq 200\,\mu$m
	Time Resolution	≤ 100 ps
Radiative Decay	Momentum Resolution	≤ 0.5 MeV
	Initial Momentum	0

Table 3.1: Detector requirements for background identification [20]

3.3 The Mu3e Detector

The Mu3e detector consists of two double layers of silicon pixel sensors, of which the outer pixel layers are extended at both sides of the detector to observe particle recurls [20]. Additional scintillator layers provide timing information, but are not further discussed in this thesis. The muons are stopped by a hollow, double-cone target inside the detector. The detector is located inside a superconducting solenoid magnet which provides an external magnetic field of 1 T.

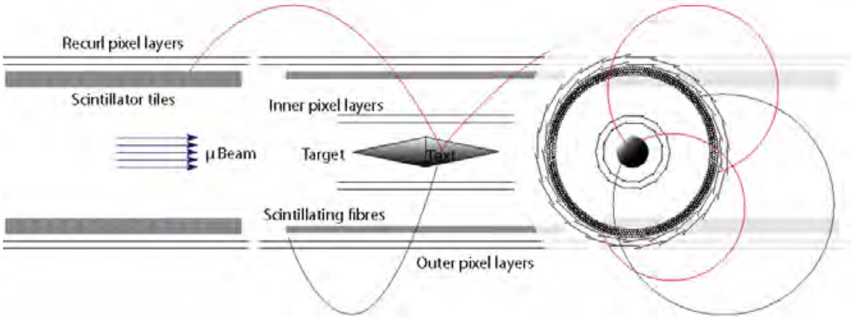


Figure 6: Visualisation of the Mu3e detector [21]

The detector is designed to achieve the momentum and vertexing resolutions shown in Table 3.1. The sensors and scintillators provide the necessary time resolution for hit identification and removing the combinatorial background.

The inner pixel detector provides a good vertex resolution due to the small radii of the sensor modules. The radius is defined as the distance of the detector layer from the beam line, the symmetry axis of the Mu3e detector. The proximity of the inner pixel detector to the beam line means that there is little material, and therefore little scattering between the target and the detector.

The momentum resolution is achieved by the sensors in the outer pixel layers and the recurl stations. The momentum resolution can be improved by increasing the magnetic field strength or reducing multiple scattering.

The magnetic field strength is set by the external magnet. Additional reduction of multiple scattering is dependent on the detector design. The curvature of the particle trajectories due to the magnetic field allows additional measurements at their re-entry to the detector at the recurl stations. This means the particles are observed at two points, with the angle between them approximately equal to π, which cancels out much of the multiple scattering effect. To reduce the remaining multiple scattering, the material in the active detector volume must be kept to a minimum.

The specialisation of the sensors to meet the requirements of the Mu3e experiment is further discussed in Chapter 5.

Chapter 4

Particle Detection

Particles have characteristic interactions with the medium they pass through based on their mass, charge, velocity, external magnetic or electric fields, and the medium itself. A particle can be observed through its interaction with a detector medium. This chapter will discuss one aspect of particle detection in the Mu3e detector: observation of charged particles with pixel sensors[1].

4.1 Interactions of Charged Particles with Matter

The description of particle interactions with matter presented in this chapter is based on [5] and [22]. Charged particles lose energy when they pass through matter. They transfer energy to the electrons in the material, causing excitation or ionisation. The nature of this energy loss differs between electrons and heavy charged particles, because the low mass of electrons implies that they always travel at relativistic speeds.

4.1.1 Heavy Charged Particles

Heavy charged particles lose energy in a medium according to the Bethe-Bloch formula (from [22], slightly amended). The Bethe- Bloch formula describes the energy loss per unit distance of heavy charged particles passing through a medium, due to excitation and ionisation of electrons in the medium.

$$-\left\langle \frac{dE}{dx} \right\rangle = K \frac{Z}{A} \rho \frac{z^2}{\beta^2} \left[\frac{1}{2} ln \left(\frac{2 m_e c^2 \beta^2 \gamma^2 T_{max}}{I^2} \right) - \beta^2 - \frac{\delta(\beta\gamma)}{2} - \frac{C(\beta\gamma, I)}{Z} \right] \tag{4.1}$$

The energy loss with distance is therefore dependent on following variables:

- z and β, the charge and velocity ($\beta = \frac{v}{c}$) of the charged particle.
- Z and A, the atomic number and atomic mass number of the medium.
- ρ, the density of the material
- I, the mean energy required to ionise the medium.

---

[1] The Mu3e detector will also contain scintillating fibres for precise time measurements. As the fibres are not relevant to this thesis, their structure and operation is not further discussed.

- γ, the Lorentz factor of the traversing particle $\left(\gamma = \frac{1}{\sqrt{1-\beta^2}}\right)$
- T_{max}, the mean energy transfer to a bound electron through a head-on collision.
- δ, a density correction, which is particularly relevant for high energy particles.
- C/Z, a correction for number of energy levels, which is important for low velocities.
- $K = 4\pi N_A r_e^2 m_e c^2$, a constant dependent on the electron radius.

Particles with low velocities lose more energy per unit distance. In this case, the energy loss is proportional to $\frac{1}{\beta^2}$. Another special case are particles in the momentum region of $\beta\gamma \approx 3-3.5$. These are minimally ionising particles (mips) and show a density-normalised energy loss of $\leq 2\,\text{MeV g}^{-1}\text{cm}^2$ [23]. For higher energies, the energy loss per unit distance for heavy charged particles increases logarithmically until it reaches the Fermi-plateau. The logarithmic increase is due to the relativistic increase of the electric field experienced by the traversing particles at high energies. The energy loss plateaus because at high energies the density correction δ cancels out the relativistic rise. This changing behaviour of the energy loss per unit distance is shown in for some examples of heavy charged particles.

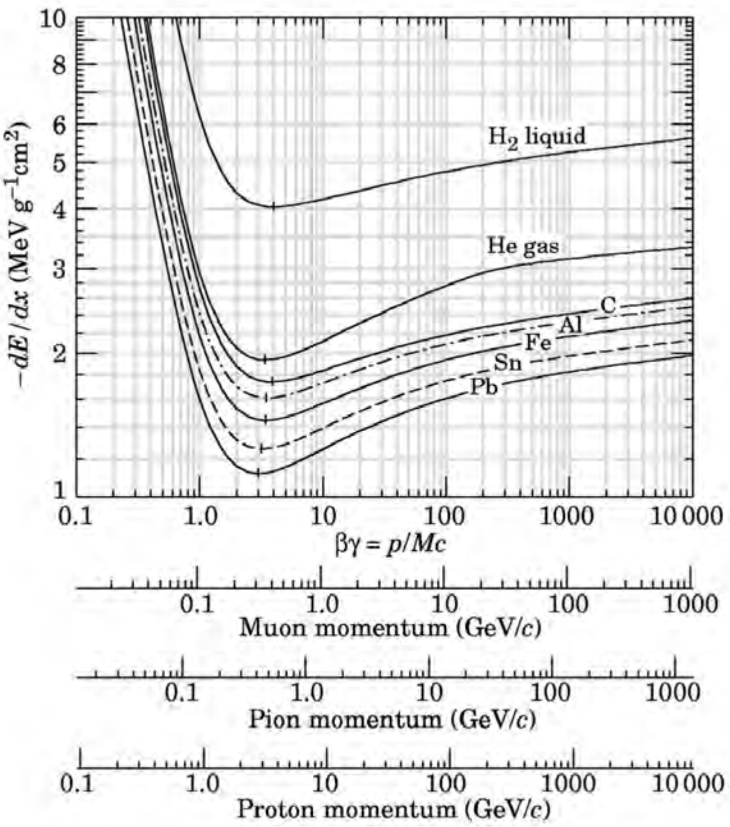


Figure 7: Energy loss per unit distance as a function of $\beta\gamma$ for pions, muons and protons in a selection of materials [24].

4.1.2 Electrons and Positrons

The Mu3e detector will observe electrons and positrons from muon decays and scattering, and, perhaps, the $\mu^+ \rightarrow e^+e^-e^+$ decay.

The interaction of electrons with matter is characterised by effects not described by the Bethe-Bloch formula. The electrons lose a high amount of energy through bremsstrahlung due to their low mass. Bremsstrahlung is the emission of a high energy photon in response to the electromagnetic deflection of a high energy electron by an atomic nucleus. Positrons can annihilate electrons in the material, while incident electrons are not distinguishable from those already in the material. The total energy loss per unit distance with respect to all these effects, according to [25], is given by Equation 4.2, the Berger-Seltzer formula, and shown in Figure 8.

$$-\left\langle \frac{dE}{dx} \right\rangle = \rho \frac{Z}{A} \frac{0.153526}{\beta^2} \left(B_0(T) - 2ln\left(\frac{I}{m_e c^2}\right) - \delta \right) \tag{4.2}$$

The same variable definitions apply in Equation 4.2 as for Equation 4.1. B_0(T) is the stopping power of the material, which depends on the kinetic energy of the particle, and is different for electrons and positrons to accommodate the possibility of annihilation.

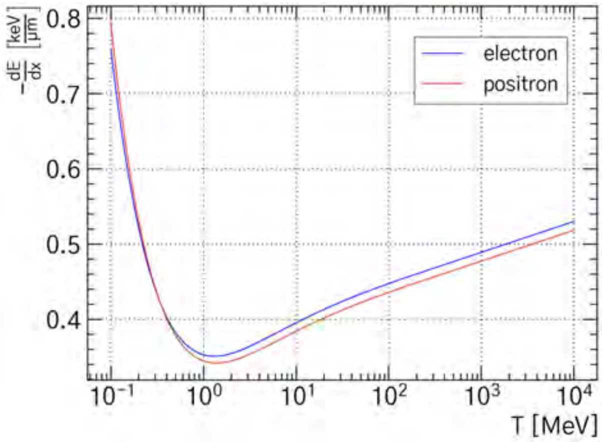


Figure 8: Energy loss per unit distance for electrons and positrons in silicon, from [26].

The difference in energy loss between the electrons and positrons are due to the inability to distinguish electrons which are incident, and those inherent to the material, which is not a problem for positrons.

The energy loss of electrons due to bremsstrahlung is given by Equation 4.3 (adapted from [22]).

$$\frac{dE}{dx} = -\frac{E_0}{X_0} \tag{4.3}$$

With X_0 the radiation length, which is given empirically in [8] in the form of Equation 4.4.

$$X_0 = \frac{716.408\, g\, cm^{-2} A}{\rho Z(Z+1)\ln(\frac{287}{\sqrt{Z}})} \tag{4.4}$$

Most of the energy lost to bremsstrahlung is not deposited in the detector. The bremsstrahlung photons have high energies and mostly leave the detector without interacting with the material.

4.1.3 Multiple Scattering

The electrons and positrons created in the Mu3e detector will pass through multiple detector layers, and experience energy loss and electromagnetic deflection at each one. The multiple coulomb scattering angle is the angle between initial and final path after multiple scattering events. The probability distribution of the multiple scattering angle θ takes a Gaussian shape, centred around the initial direction of the particle. The variance is given by the Highland formula shown in Equation 4.5 [22] [27].

$$\sigma_\theta = \frac{13.6\,\mathrm{MeV/c}}{p\beta} z \sqrt{\frac{x}{X_0}} \left(1 + 0.038 \ln\left(\frac{x}{X_0}\right)\right) \tag{4.5}$$

With x, the thickness of the detector layer, z, the charge of the particle, X_0, the radiation length, and p the momentum of the particle. Minimising multiple scattering can increase the accuracy of tracking and therefore the momentum resolution for detected particles. The reduction of multiple scattering is therefore a key consideration for the design of the Mu3e detector, as was discussed in Chapter 3.

4.2 Semiconductor Physics

The conductive properties of semiconductors make them well suited for the detection of charged particles. A semiconductor is a material with a conductivity below that of a metal, but above that of an insulator. The valence band has a small band gap to the conduction band. This is shown in Figure 9.

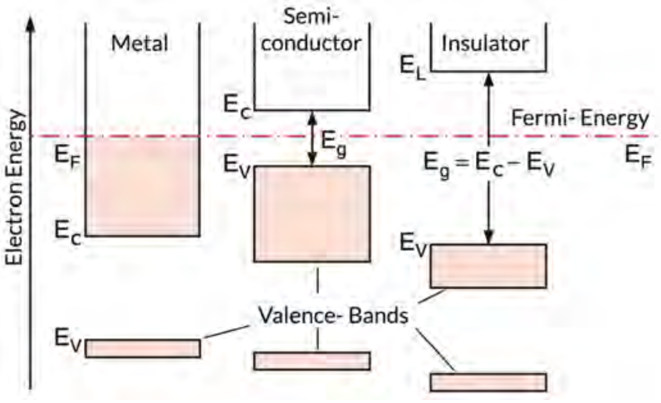


Figure 9: The energy band configuration for metals, semiconductors and insulators, translated from [28].

The conductivity of a semiconductor can be increased through doping. Doping is the introduction of another element with a different number of outer shell electrons than the semiconductor material. This is visualised in Figure 10. Dopants with more outer shell electrons than an atom of the semiconductor introduce excess electrons to the material, which cannot be bound into the material lattice. This produces an n-doped semiconductor. Dopants with fewer outer shell electrons will introduce excess holes to the material, which produces a p-doped semiconductor. In both cases, the semiconductor contains more free charge carriers than before the doping, and is therefore more conductive. The overall charge of the material remains zero, as the charge of the free electrons or holes is compensated by the charge of nucleus of the doping material bound in the crystal lattice.

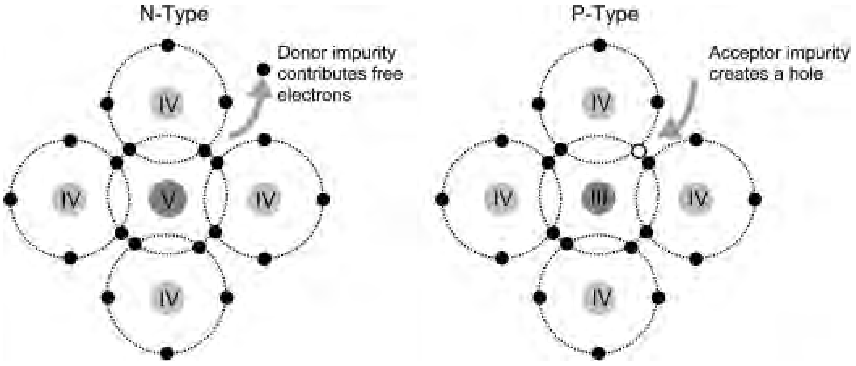

N-Type
Donor impurity contributes free electrons
IV
IV
V
IV
IV
P-Type
Acceptor impurity creates a hole
IV
IV
III
IV
IV

Figure 10: Visualisation of n- and p- doping of semiconductors, taken from [29].

4.2.1 The P-N Junction

When n- and p-doped semiconductors are brought into contact, the electrons and holes diffuse from their respective areas of high concentration to areas of low concentration and recombine in the boundary region. Every hole that leaves an atom in the p-doped semiconductor leaves behind a negative ion. Similarly, every electron that leaves an atom in the n-doped semiconductor leaves behind a positive ion. The n-doped semiconductor becomes positively charged at the boundary, and the p-doped semiconductor becomes negatively charged at the boundary. The boundary region has no more free charge carriers and is called the depletion region.

An electric field develops across the depletion region, from the positively charged region to the negatively charged region. This field opposes the further expansion of the depletion region. The diffusion process stops when the electric field of the positive and negative ions at the boundary balances the diffusion. The semiconductor material far from the boundary remains neutral and undepleted. In this state of equilibrium, there is negligible current flow.

A p-n junction is also known as a p-n diode. Current can pass through the junction in the direction of the electric field (from the n-doped semiconductor to the p-doped semiconductor) but not against it, as the oppositely charged sides of the depletion region form a voltage barrier. The development of the depletion region at a p-n junction is visualised in Figure 11.

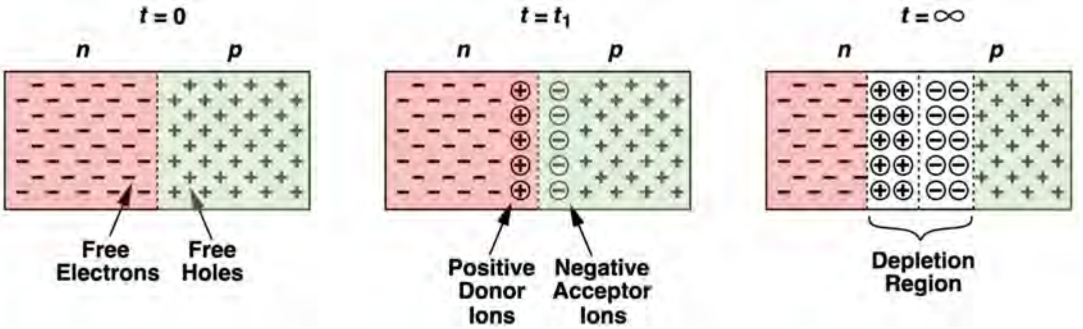


Figure 11: Visualisation of the development of a depletion region at a p-n junction, adapted from [30][31].

Particle detection by pixel sensors relies on a p-n diode under reverse bias. A voltage is applied with the positive terminal at the n-doped semiconductor, and the negative terminal at the p-doped semiconductor. Since the E-field of a p-n junction in equilibrium points from the n-doped semiconductor to the p-doped semiconductor, the reverse bias voltage enhances it, increasing the width of the depletion region. The voltage barrier across the depletion region is increased, so the current flow through the diode, the leakage current, is very small. The diode therefore acts as a capacitor, with the two charged areas in the depletion zone acting as the two capacitor plates.

The capacitance depends on the supplied bias voltage. A higher reverse bias voltage expands the depletion region, reducing the capacitance of the pixel. Equation 4.6 was adapted from [22]. It describes width of the depletion zone w, it terms of the applied reverse bias voltage U, the vacuum permittivity ϵ_0, the relative permittivity[2] of silicon ϵ, the (p-) doping concentration N_D, and the elementary charge e.

$$w = \sqrt{2\epsilon\epsilon_0 \mathrm{U} \cdot \frac{1}{\mathrm{N_D} e}} \tag{4.6}$$

The doping concentration for silicon substrates is often given in terms of the resistivity ρ, as shown in Equation 4.7 [32].

$$\rho = \frac{1}{e \mathrm{N_D} \mu} \tag{4.7}$$

With μ the mobility, which describes how quickly a charge carrier can be transported through a material by an electric field. The depletion depth in terms of ρ is therefore given by Equation 4.8.

$$w = \sqrt{2\epsilon\epsilon_0 \mathrm{U} \rho\mu} \tag{4.8}$$

---

[2] The relative permittivity of silicon is 11.9 [22]

The electric field strength for a given HV bias voltage U, and resistivity ρ, is given by Equation 4.9 adapted from [32].

$$E = \sqrt{\frac{2}{\epsilon\epsilon_0\rho\mu}U} \tag{4.9}$$

At very high electric field strengths, the leakage current will show a very large, rapid increase [31]. This is due to the electron-hole pairs created by ionisation being accelerated to high drift velocities by the electric field. The kinetic energy of the charge carriers surpasses the ionisation energy of the silicon atoms, and can therefore generate new electron-hole pairs through impact ionisation. These electron-hole pairs are themselves accelerated and will cause further ionisation, creating an avalanche of free charge carriers and a rapid current increase. This is known as an avalanche breakdown.

The electric field strength at which avalanche breakdown occurs depends on the ionisation energy of the substrate, and lies at $\approx 3 \times 10^5\,\mathrm{V/cm}$ for silicon [32]. The reverse bias voltage that generates this electric field in the diode is referred to as the breakdown voltage, and is the largest reverse bias voltage that can be applied without the leakage current entering an exponential increase.

4.3 Pixel Sensors

The Mu3e experiment aims to detect charged electrons and positrons using pixel sensors. The neutrinos are not observable by pixel sensors because they only interact weakly, and the pixel sensors rely on ionisation via the electromagnetic interaction.

Pixel sensors use p-n diodes under reverse bias to observe charged particles. When a charged particle passes through the sensor, it causes ionisation in the material, see Section 4.1. Within the depleted region the resulting electron-hole pairs are accelerated by the E-field. The electrons are transported towards the positive electrode, while the holes are accelerated towards the negative electrode. Outside of the depleted region the electron-hole pairs will diffuse randomly until they reach the depletion region or are reabsorbed.

According to the Shockley Ramo theorem [22], this current flow in the p-n diode, the leakage current, causes a a temporary decrease in diode capacitance, which induces a voltage signal at the collection diodes, the height and duration of which depend on the energy lost by the charged particle which passed through the sensor.

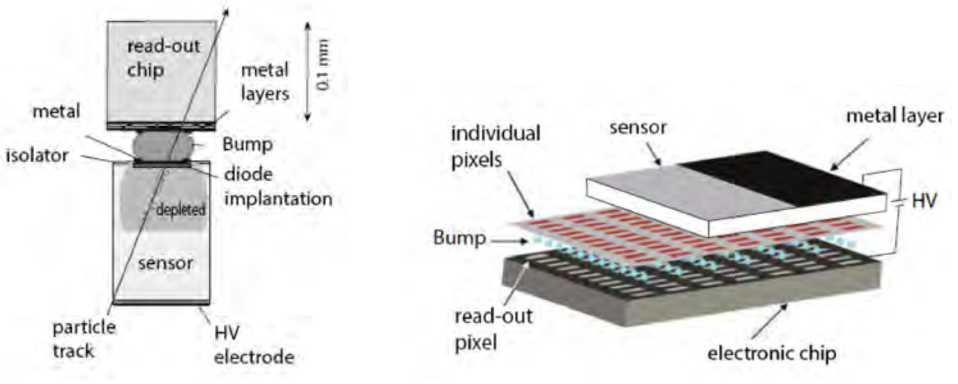
At the kinetic energies expected in the Mu3e detector, a higher energy (or momentum) electron loses more energy due to ionisation than a low energy electron, see Figure 8. Therefore a particle with higher energy creates a larger diode current, and results in a taller and wider output voltage signal.

The individual pixels are organised in a pixel matrix, which makes up the active area of a sensor. The depletion of the pixel improves the time resolution of the sensor. Electrons and holes are transported much faster inside the depletion zone, where the E-field accelerates them, than outside it, where they travel by diffusion. A larger depletion region means that more of the ionisation by passing particles occurs in the depleted region, and a better efficiency and time resolution can be achieved.

4.3.1 Hybrid Sensors

Conventionally, pixel sensors are produced as hybrid sensors. These consist of a sensor with a pixel matrix, and a read-out chip, which is connected to the sensor by bump-bonds. This is shown in Figure 12.

Hybrid sensors are not appropriate for particle detection in Mu3e. The separate read-out sensor and bump bonds, as well as a limited ability to reduce sensor thickness, means that they would not meet the material budget requirement. Therefore, the momentum resolution required to identify the Mu3e decay is not attainable with hybrid sensors.



(a) A hybrid pixel cell (b) A hybrid pixel sensor

Figure 12: Schematics showing the working principle of a hybrid pixel sensor [33].

4.3.2 HV-MAPS

MAPS, Monolithic Active Pixel Sensors, feature read-out electronics embedded in the pixels to eliminate the need for a separate readout chip. HV- MAPS are High-Voltage MAPS. They feature a high reverse bias voltage to increase the drift velocity of charge carriers in the pixel, which improves the time resolution of the sensor. HV-MAPS sensors consist of an active matrix of pixels and a periphery. The periphery is not sensitive to passing particles, but contains electronics for signal processing and data read-out. HV-MAPS feature analogue read-out electronics embedded in the n-well, as shown in Figure 13. These components amplify and transmit the signal to the periphery.

The amount of in-pixel integration varies across the different types of HV-MAPS sensors. Further analogue circuitry components can be embedded in the pixels, or placed in the periphery, which houses the digital circuitry components. In the sensors discussed in this thesis, the signals are filtered for noise, digitised, and read-out in the periphery.

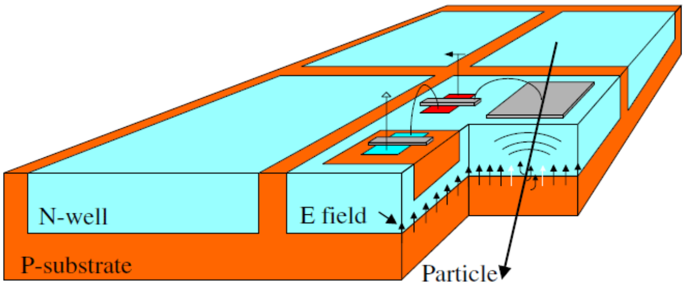


Figure 13: Visualisation of the pixel structure of a HV-MAPS sensor [21].

HV-MAPS sensors are a good option for the Mu3e detector because they are low-material sensors. Not only is there no need for a separate read-out chip, but the sensor itself can be thinned down to up to 50 µm after production. The thinning of the sensors for the pixel detectors is a critical step towards achieving the momentum resolution target of the Mu3e experiment.

Chapter 5

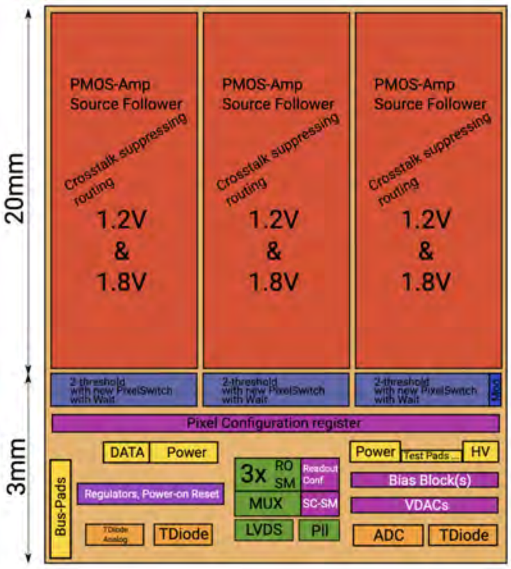
The MuPix11 Sensor

The MuPix11 sensor is designed for the tracking system of the Mu3e Experiment [34] [35]. Phase I of the Mu3e experiment will use MuPix11 for both the inner and outer detector layers.

The MuPix11 is an HV-MAPS sensor, as described in Section 4.3.2. The monolithic pixel technology of the HV-MAPS allows them to be thinned to small thicknesses to meet the very low material budget required by the experiment. MuPix11 are produced at both 70 µm and 50 µm thicknesses. The technical description of the MuPix11 sensor presented in this chapter is based on [20], and [34]. The key experimental requirements[1] for the pixel sensors are listed in Figure 14a. The layout of the MuPix11 is shown in Figure 14b.

Feature	Target
Sensor dimensions [mm]	$\leq$ 21 x 23
Sensor size [mm]	$\approx$ 20 x 20
Thickness [μm]	$\leq$ 50
Spatial resolution [μm]	$\leq$ 30
Time resolution [ns]	$\leq$ 20
Hit efficiency [%]	$>$ 99
Number of LVDS links (inner layers)	1 (3)
Bandwidth per link [Gbit/s]	$\geq$ 1.25
Power density [mW/cm^2]	$\leq$ 350
Operation temperature range [°C]	0 - 70

(a) Main MuPix11 requirements.


20mm
3mm
PMOS-Amp
Source Follower
Crosstalk suppressing routing
1.2V & 1.8V
PMOS-Amp
Source Follower
Crosstalk suppressing routing
1.2V & 1.8V
PMOS-Amp
Source Follower
Crosstalk suppressing routing
1.2V & 1.8V
2-threshold with new PixelSwitch with Wait
2-threshold with new PixelSwitch with Wait
2-threshold with new PixelSwitch with Wait
Pixel Configuration register
DATA
Power
Bus-Pads
Regulators, Power-on Reset
TDiode Analog
TDiode
3x
RO SM
Readout Conf
MUX
SC-SM
LVDS
Pll
Power
Test Pads
HV
Bias Block(s)
VDACs
ADC
TDiode

(b) MuPix11 block diagram.
Not to scale.

Figure 14: Main requirements of the MuPix11 sensor and MuPix11 block diagram [20].

The active region of the sensor is the pixel matrix. It is divided into three sub-matrices, of 42:43:43 double pixel columns, which are read out separately. The pixel diodes are

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[1] The requirement for a maximum thickness of 50 µm is under review. Sensors of 70 µm thickness will also be considered for installation.

implemented using a 200 Ωcm silicon substrate, which can vary between 200 Ωcm and 400 Ωcm due to production fluctuation. Measurements have shown the previously tested sensors to have a substrate resistivity of ∼ 369 Ωcm [32].
The digital electronics are mostly located in the periphery. In this way, the rapidly switching digital signals are separated from the analogue circuits, which reduces cross-talk. The periphery also contains connector pads for operation and testing. These supply power, ground, bias voltage, as well as differential links for sensor configuration and the readout of signal and monitoring data.

5.1 Sensor Mounting in the Pixel Detector

To meet the material budget of the detector, the sensors must operate with minimal connections for powering, settings and data readout. The materials used for mounting and powering should also have low atomic masses where possible.
The sensors will be mounted on High Density Interconnects (HDI), which is made from thin kapton-aluminium foil to meet the material budget. These HDIs supply power and bias voltage to the sensors, and transmit control signals and data. The sensors will be bonded to the HDIs using Single-point Tape- Automated Bonding (SpTAB), which is permanent, so the functionality of the sensors must be verified before they are connected. Sensors for the inner and outer layers are arranged in ladders of 6 and 18, respectively, which are joined to make modules of 4 ladders each. Layer 2 is an exception, which will consist of modules constructed of 5 ladders each. The glue used to attach the sensors to the HDIs has a temperature limit of 70°, which limits the maximum permitted power consumption by the sensors.

5.2 The Read-out Scheme

The electronic architecture of the read-out circuitry from incident hit to digital output is visualised in Figure 15.

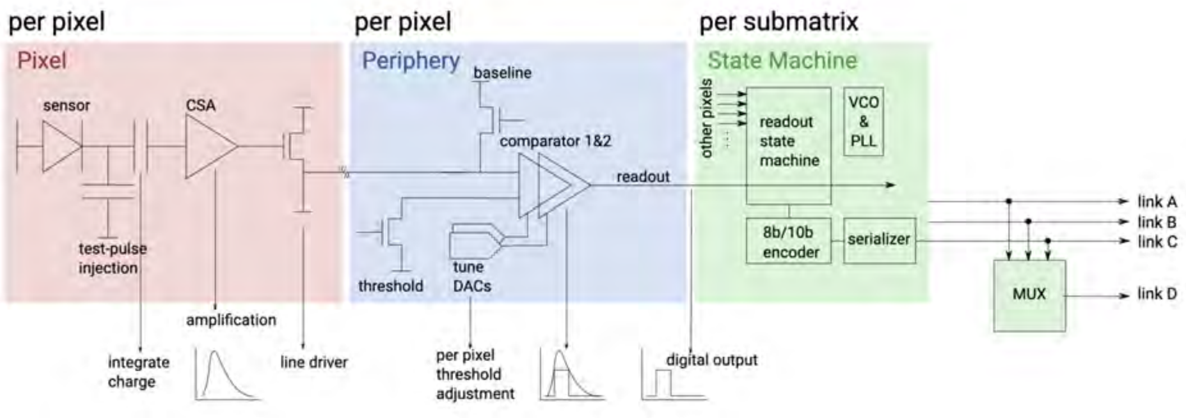

per pixel
Pixel
sensor
CSA
test-pulse injection
per pixel
Periphery
baseline
comparator 1&2
readout
threshold
tune DACs
per submatrix
State Machine
other pixels
readout state machine
VCO & PLL
8b/10b encoder
serializer
MUX
link A
link B
link C
link D
amplification
integrate charge
line driver
per pixel threshold adjustment
digital output

Figure 15: The Electronic Architecture of the MuPix11 sensor [34].

5.2.1 Signal Processing

After a signal is generated in the pixel, as discussed in Section 4.3, it is amplified by the charge sensitive amplifier (CSA), and transmitted to the periphery by the line driver, both of which are located in the pixels themselves.

Signals which arrive at the periphery pass through a comparator system. A comparator compares the voltage of the signal line to a threshold, in order to separate true hits from noise. The signals that stay below the threshold are discarded.

Signals that reach the threshold are digitised. The pixel address, Time of Arrival (ToA) at the threshold, and the Time over Threshold (ToT) values are recorded for each hit and collected by the internal state machine.

The signals shown in Figure 16 visualise a key feature of the pixel data, the timewalk effect. The signals of higher voltages, generated by particles of higher momentum, are steeper, and reach the thresholds with less time delay than lower signals. This is visualised in Figure 16.

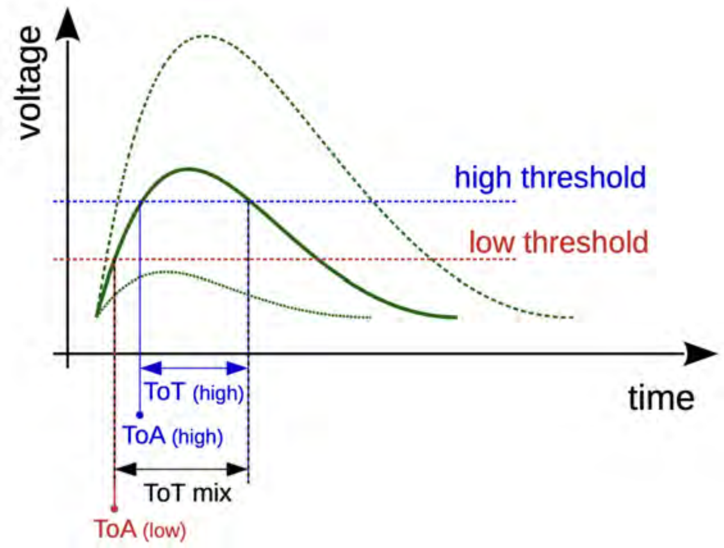


Figure 16: Visualisation of the analogue signal, and key signal characteristics [20].

The MuPix11 has a two comparator system. This allows the definition of a high and low threshold. The high thresholds can be used for hit flagging, while the low threshold can be used to find the time of arrival for the identified hits. This is beneficial as the higher threshold has a limited time resolution and stronger time walk effects, while the low threshold is more likely to accept noise.

5.2.2 Data Readout

The state machine serialises the hit information, which is then sent out through serial links. The links use Low Voltage Differential Signaling (LVDS) technology, and send out data at a rate of 1.25 Gbit/s per link.

The MuPix11 features a Voltage Controlled Oscillator (VCO), which is kept in phase with the external Mu3e reference clock using a Phase Locked Loop (PLL). VPVCO is a DAC (Digital-to Analogue Converter), which can be changed to configure the VCO. The links are clocked by the internal fast clock, which runs at 625 MHz, and is derived from the external clock by the VCO.

The LVDS links can be operated in parallel or multiplexed mode. In parallel, three links, named A, B and C simultaneously send out the hit information for each corresponding sub-matrix. The hit information for the pixel areas is separated. In multiplexed mode, the state machine alternates read out for the three sub-matrices, which is then sent through a single serial link, link D. Three link readout will be used for the inner layer, while hits from the outer layer will be read out in multiplexed mode. This is intended to reduce power consumption and external connections for these sensors, and is possible because they experience a lower hit rate than the inner detector.

The data sent out by the LVDS links is 8bit/10bit encoded. Each 8 bit data segment is accompanied by two control bits. Correctly read-out control bits verify that the internal and external clocks are still in phase. This is designed to detect misalignment between the external clock and the internal sensor clock, and therefore ensure the stability of the clocks and the accuracy of data read-out during operation.

5.3 Powering

The MuPix11 sensor is powered by two supply voltages. The VDDD supplies the digital domain, and the VDDA supplies the analogue domain. The two voltages are equal and therefore shorted to reduce the number of necessary connections to the sensor. The main voltage supply to the amplifier, the VSSA, is generated from the VDDA using an internal low dropout regulator (LDO) and then fed back to the chip via external loops in the HDI design. Upon turn on, the sensor is in standby mode, and must be configured before operation. The powering of the sensor must be regulated to compensate for power losses due to resistances in the internal power distribution. This is not exclusive to the MuPix11 sensor, but an important aspect of the powering strategy which will be investigated in this thesis.

The voltage arriving at the sensor is measured via the power supply using a sense line, which carries no current itself. An optimisation algorithm is used to ensure the correct voltages are being applied inside the sensors. The power supply then adjusts its supply voltage until the sensor receives the target voltage. This compensates voltage drops between the power supply and the sensors' internal power grids, but cannot compensate for resistances on the internal power grid. VDDD and VDDA are regulated by the external supply voltage, while VSSA is regulated using the ref_VSS DAC value. All three internal voltages are measured separately at the two sides of the sensor. For example, VSSA is representative of VSSA1 and VSSA2, which are each measured at one of the sensor partitions. The internal voltages are read out using a special test pad named ”TestOut”.

5.4 Global Configuration

The global configuration of the sensors powers the on-chip circuitry, and changes key configuration voltages, which set various settings on the sensor. The configuration is performed after powering to ready the sensor for operation. Two important registers for the global configuration are BiasBlock and VDAC, which operate in parallel. BiasBlock controls key circuitry components, as shown in Table 5.1

Component	Location	Relevant DACs	Purpose
Amplifier	Pixel	VNPix, VNFollPix, VSSA	Amplify signal
Line Driver	Pixel	VNOutPix	Drive signal to periphery
Comparator	periphery	VNComp	Discriminate signal
Clocking	periphery	VNDCL, VPDCL	Synchronised readout
LVDS driver	periphery	VNLVDS, VNLVDSDel	Drive data to FEB

Table 5.1: Key circuitry components set by the BiasBlock register.

VDACs are Voltage DACS, or Digital-to-Analogue Voltage Converters. Table 5.2 shows key VDACs and their respective functions. VSS1 and VSS2 are derived from the Ref_VSS DAC, which supplies the VSSA amplifier supply voltage to the two partitions of the pixel matrix separately. VSS1 and VSS2 represent the effect of Ref_VSS in partitions one and two, respectively.

VDAC	Purpose
Ref_VSS	Sets the amplifier voltage supply
BLPix	Sets the baseline voltage for the pixel
Baseline	Sets the baseline voltage for the amplified signal
ThHigh	Sets the threshold for comparator 1: high threshold for hit flags
ThLow	Sets the threshold for comparator 2: low threshold for timing

Table 5.2: The role of key VDACs for the function of the sensor circuitry.

The reliable operation of a MuPix11 sensor depends on its successful powering and global configuration.

5.5 Challenges in the MuPix11 Design

The high time-resolution, low-material MuPix11 design is necessary to fulfil the requirements of the pixel detector but carries with it potential risks for general sensor functionality.

The size of the active pixel matrix necessitates long analogue readout lines to send hit signals from the pixels to the periphery, which are concentrated into only three metal layers. Their length and dense routing makes them vulnerable to cross-talk, which can deteriorate the vertex resolution. To reduce this, they are split-routed. Split-routing is the alternation of the routing direction, to the left or right of the pixel, between pixels, so that neighbouring lines do not correspond to neighbouring pixels. This means that cross-talk between lines would generate a false hit in the second-to-next pixel to the original, not in the neighbouring pixel, making it easier to separate cross-talk from charge sharing effects. However, split-routing cannot reduce the short-risk of the routing scheme. Small production errors, such as dust in the production space, can lead to unwanted line connections due to the close proximity of the readout lines.

The thin sensor design poses a challenge for their efficiency and time resolution, because a thicker sensor produces more charge for an incident particle, which results in a larger signal. Smaller signals may not reach the threshold, decreasing the efficiency, or only reach the threshold close to the signal peak, deteriorating the time resolution. Thicker sensors allow a larger depletion depth, which decreases the pixel capacitance and therefore reduces pixel noise. The thin sensors are also prone to handling damage, as the thin silicon is extremely fragile.

The post-processing of MuPix11 wafers to achieve the necessary thicknesses of 50 µm or 70 µm can cause damage. After production, the bare p-substrate at the back-side of a wafer of sensors is thinned by grinding and plasma-etching. Thinning through grinding is known to damage the crystal structure deep inside the substrate in the form of sub-surface cracks [36][37], which increase the concentration of lattice impurities at the back-side of the sensor. Grinding also introduces high stresses to the wafers, causing the sensors to warp [37]. This could cause cracks and shifts in the on-chip circuitry. Removing the last few μm of silicon by plasma-etching can reduce the depth of sub-surface cracks [38]. The grinding and plasma-etching processes occur closer to the on-chip circuitry for 50 µm sensors. The quality control tests presented in this thesis will provide a first indication of how much this will affect the 50 µm yield.

Chapter 6

MuPix11 Quality Control

The main goal of quality control testing is to assess the performance of each MuPix11 sensor considered for use in the pixel detector. The procedure will ensure that all installed sensors are fully functional and meet certain experimental requirements.

As described in Section 3.2, the MuPix11 sensors are specialised to fulfil the requirements and experimental constraints of the Mu3e experiment. These constraints pose challenges for the sensor design and manufacturing, which may lead to characteristic failures (see Section 5.5). The quality control procedure is designed to include investigation of the challenges specific to the MuPix11 design.

6.1 Testing Strategy

The MuPix11 quality control procedure analysed during this thesis consists of five independent tests, carried out sequentially, each of which assesses a key function of the sensor. If the chip cannot carry out all of these key functions, it is unsuitable for use.

For each test, a series of measurements is performed on the chip. The outcome of each test is evaluated using precise numerical criteria, to assess if the measurement output shows the characteristic behaviour of a functional sensor. Each test then categorises the sensors according to the scheme shown in Table 6.1. The evaluation is described in Chapter 7.

Grade	Criteria
Strong pass	The chip shows the required functionality.
Weak pass	The chip shows functionality, but has limitations.
Failed	The chip cannot perform the tested function.

Table 6.1: The categorisation performed by each quality control test

The final quality control grade for a sensor is derived from the individual quality control tests, as shown in Table 6.2.

Grade	Criteria
A	5 strong passes
B	4 strong passes, no failures
C	3 strong passes, no failures
D	2 strong passes, no failures
E	1 strong pass, no failures
F	At least 1 failed test

Table 6.2: Definition of the QC final grading criteria

Chips with grades A to E are functional. However, sensors with grades B-E show behaviours which could limit their operation in the detector. Grade A-E sensors should be considered for installation in the Mu3e pixel detector, with the higher grades prioritised. The minimum quality a sensor must achieve for installation will be decided in the context of production.

6.2 The Quality Control Tests

To ensure that the sensors installed are able to detect particles, and transmit the relevant information accurately, the sensors must show reliability in their signal generation, general operation, data processing and data transmission. The key functionality indicators are listed in Table 6.3, as well as the tests designed for their evaluation.

Category	Key Function	Test
Signal Generation	The pixel matrix can be biased to sufficient hit sensitivity	IV Scan
General Operation	The on-chip circuitry can be turned on.	LV Power- On
General Operation	The sensor receives the correct internal voltages.	Internal Voltages
Data Processing	Essential voltages can be set.	VDAC Scans
Data Transmission	The chip can communicate data without 8b/10b errors.	LVDS links

Table 6.3: Overview of key functions and the corresponding quality control tests

These functionality indicators and testing procedures were defined before this thesis. This thesis presents a clearly defined evaluation scheme, which is then used to analyse and improve the existing quality control tests.

Test I: IV scan

Aim:	To test if the chip can be operated well at the intended HV bias voltage.
Strategy:	Investigate the leakage current with increasing HV bias voltage.
Parameters:	Minimum and maximum HV bias voltages, current limit, coarse step-size, fine step-size
Procedure:	The sensor is powered and configured. The bias voltage is increased in intervals of the coarse step-size, with the leakage current measured at each step. The test is stopped when the bias voltage reaches the maximum, or if the current limit is reached, in which case the measurements for the last 10 V are repeated at the fine step-size, for good resolution of key features like the final breakdown.
Outcome:	This test shows if the chip reaches and shows stable behaviour at the intended HV bias voltage. This is important for the chip's pixel sensitivity and therefore the efficiency and time resolution.

Test II: LV Power- On

Aim:	To test if the on-chip circuitry can be turned on.
Strategy:	Investigate the current consumption of the on-chip circuitry, as described in Section 5.4.
Parameters:	Biasblock setting
Procedure:	The biasblock setting defines the powering of the on-chip circuitry described in Section 5.4. It is set to 0, for which the circuitry is off, and the current is measured. The biasblock is then set to 5, which powers the on-chip circuitry, and the current is measured again.
Outcome:	This test shows if the on-chip circuitry has a suitable LV current. A suitably high current indicates the sensor's ability to power the on-chip circuitry, but very high currents could lead to a non-uniform power consumption in the detector, and could indicate the presence of shorts.

Test III: Internal Voltages

Aim:	To test if the chip's internal voltages can be set to target values.
Strategy:	Investigate the voltage received by the sensor after the voltage optimisation algorithm, described in Section 5.3.
Parameters:	Voltage targets for VDDD, VDDA and VSSA

Procedure: The voltage optimisation algorithm (see Section 5.3) is carried out simultaneously for VSSA, VDDA and VDDD, with specified step count. The voltage, ground and current are measured at each step, with the voltage and ground measured separately for the two sensor partitions. The effective voltage is the measured voltage, corrected for the ground. For a successful optimisation, the final effective voltage would be at the voltage target. This final voltage gives an indication of how much resistance there is on the way to the chip; how much compensation was necessary.

Outcome: This test shows if the chip can be set to the voltage settings used for operation, and if there is a higher resistance than expected in the routing. This would be an indication of an issue in the production of the sensor, or a faulty connection between sensor and setup.

Test IV: VDAC scans

Aim: To test if some important DAC settings can be set successfully.

Strategy: Investigate the chip's response to five key VDACs.

Parameters: Start and stop DAC values for Baseline, BLPix, ThLow, ThHigh, ref_VSS

Procedure: Each DAC value is increased in set increments from the start value to the stop value, and at each step the current and voltage are measured. Each DAC affects the function of a circuitry component, as discussed in Section 5.4. The chip's response to the increase in DAC setting is reflected in the voltage and current consumption.

Outcome: The VDAC Scan shows if the chip's DAC settings can be set successfully, and if the chip circuitry shows the correct response. The setting of each DAC is critical to the functionality of the corresponding circuitry component, such as the amplifier and comparator, and is therefore critical for the processing of detected signals.

Test V: LVDS links

Aim: To test if the sensor can transmit data without errors.

Strategy: Investigate the number of 8b/10b errors at different DAC setting.

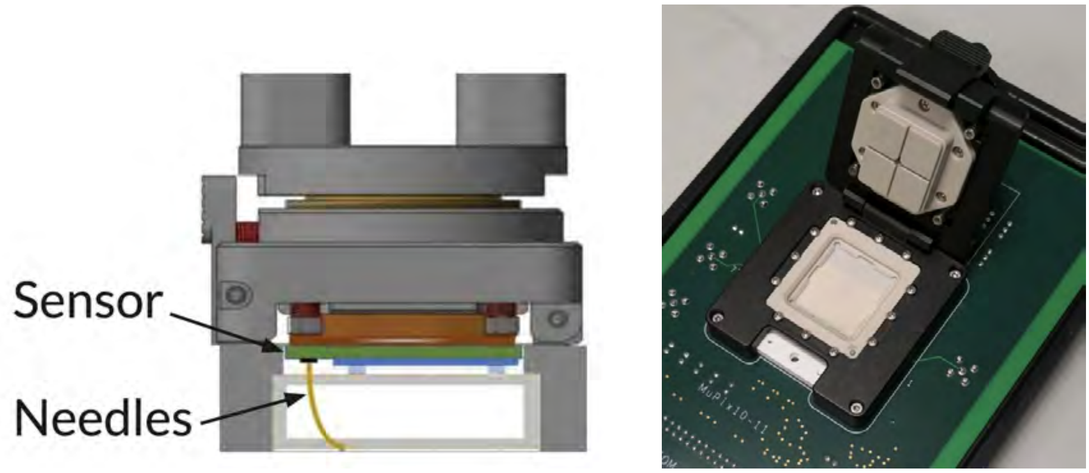
Parameters: VPVCO (VNVCO) setting

Procedure: Chip data is sent out through all four LVDS links. The number of errors in the data received over 10 s is recorded. This is repeated for multiple VNVCO settings. The VPVCO is set to VNVCO -1. These DACs regulate the internal PLL (see Section 5.2).

Outcome: This test will show if the chip can transmit data without errors.

6.3 Quality Control Set-up

The tests presented in this thesis were carried out as part of the Mu3e vertex detector pre-production phase, at the Institute of Physics in Heidelberg. The setup will be used for both pre-production and production testing phases to select sensors for the vertex detector.
The mounting used in the final experiment (see Section 5.1) does not allow for sensors to be removed once bonded. Therefore the functionality of the sensors must be ensured before they are mounted. The permanence of SpTAB makes it an unsuitable contact strategy for mass testing. The tests must be minimally invasive, and the connections to the chips fast to make and remove, to allow for the fast exchange of chips in the testing setup.



(a) Probe card schematic, side view (b) Probe card, front view

Figure 17: The probe card used for the vertex detector pre-production tests, produced by PTSL [39].

For the vertex detector quality control, these requirements are met using a probe card. The chips are inserted into a mount, as shown in Figure 17b, with a row of connector needles at the lower end. The connection to the chip is made by pressing the chip down, so that the connector pads make contact with the needles. This is visualised in Figure 17a, which shows the sensor-needle contact in the mount. As discussed in Chapter 5, the connector pads deliver the power supply and configuration voltages, as well as transmitting the readout data.

A control PC, referred to as switching PC, regulates the power supply to the MuPix11. It is connected to the power supplies by Ethernet cables, and can control the voltage applied to the High Voltage (HV) and Low Voltage (LV) circuits, as shown in Figure 18. The power supplies apply their voltage to the probe card, which transmits it to the chip's connector pads as shown in Figure 17a.

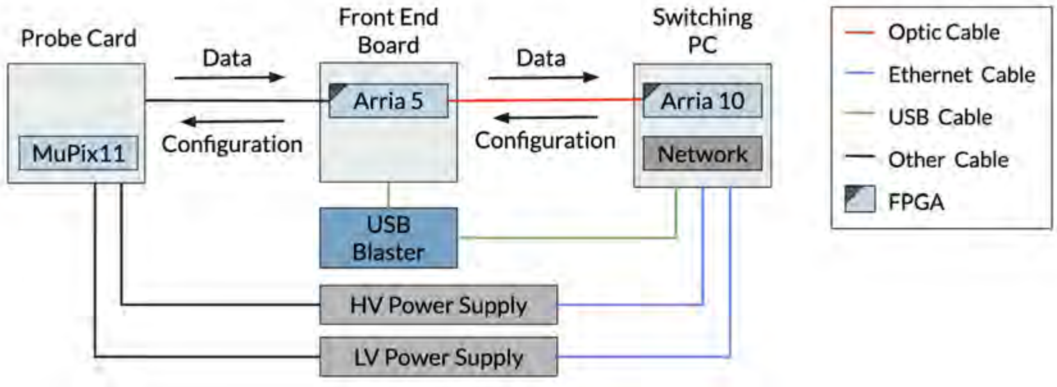

Probe Card
MuPix11
Data
Configuration
Front End Board
Arria 5
USB Blaster
Data
Configuration
Switching PC
Arria 10
Network
HV Power Supply
LV Power Supply
Optic Cable
Ethernet Cable
USB Cable
Other Cable
FPGA

Figure 18: Structure of the pre-production testing setup in Heidelberg

The control PC also provides the MuPix11 with configuration commands. These are delivered to the probe card using an Arria 5 FPGA on the Mu3e Front- End Board (FEB) [40]. The FPGA also facilitates the clock- synchronised readout of data, which is then transmitted back to the PC.

6.4 DAQ and Software

The quality control tests presented in this thesis are carried out by MIDAS sequencer scripts. MIDAS is a C/C++ based Data AQuisition (DAQ) system, developed at PSI and TRIUMF [41]. It includes MSL, a scripting language with high hardware proximity, which is used to write sequencer scripts. Sequencer commands can perform every action necessary for quality control testing.

The sequencer scripts can be viewed, edited and executed through a user interface. The improvements made to the quality control tests discussed in Chapter 9 and Chapter 8 were implemented by editing the relevant scripts to include new definitions, loops and subroutines, allowing the redefinition and introduction of improved testing parameters and procedures.

6.5 Pre-Production Testing

This thesis presents quality control in the context of pre-production testing. The pre-production tests are not restrained by the speed and efficiency requirements of the production quality control. They present a good opportunity to take additional data to investigate the sensors' failure profile. The large[1] number of sensors investigated in the context of vertex pre-production constitutes a unique opportunity to analyse MuPix11 functions with unprecedented statistics. This allows for the analysis of the testing scheme to introduce improvements to make it more accurate and reliable. This will be discussed in detail in Chapter 8 and Chapter 9. The tests previously described in this chapter should therefore be considered as preliminary, and are adapted in the course of this thesis.

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[1] Relative to previous testing campaigns

Chapter 7

Single Test Analysis

This chapter will present the analysis of the quality control tests carried out in the context of Mu3e vertex detector pre-production. The evaluation schemes will be presented for each test. The most relevant testing output is shown to illustrate the evaluation procedure and the sensors' behaviour during operation. This chapter will present results from the quality control tests of four plasma-etched wafers of MuPix11. Wafers 420-2 and 420-3 are thinned to 70 µm, and wafers 382-5 and 382-6 to 50 µm. These particular thicknesses were investigated because both are candidates for installation into the Mu3e detector.

7.1 The IV Scan

The IV scan was carried out as described in Section 6.2, with following test parameters:

- Coarse step-size (70 µm): 1 V
- Coarse step-size (50 µm) : 0.5 V
- Fine step-size: 0.1 V
- Current limit: −20 mA
- HV Bias voltage min: 0 V
- HV Bias voltage max: −120 V

The measurement intervals depend on the amount of detail necessary to resolve key features of the curve, which depends on the sensor thickness and is further discussed in Section 9.1.1. The output of an IV scan takes the form of Figure 19.

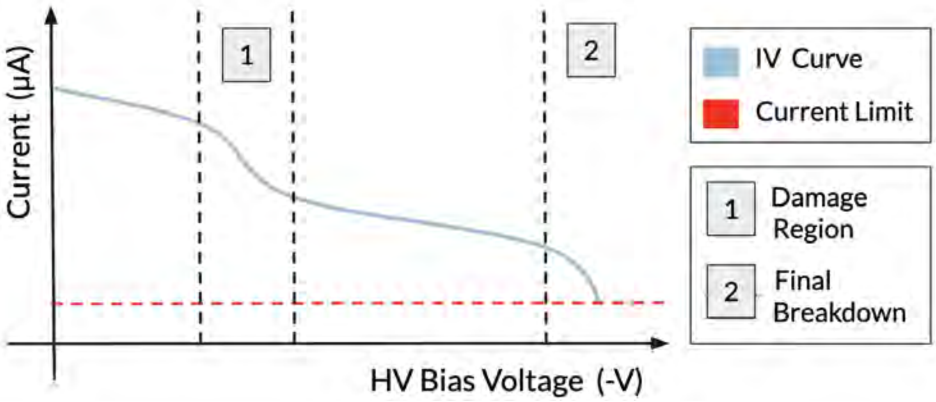

Figure 19: Expected IV curve, of leakage current against HV bias voltage, for fully depleted HV-MAPS sensors.

The IV scan shows a steady increase in the leakage current with HV bias voltage, due to the increase of the electric field inside the depletion zone. The scan also shows two distinctive increases in the leakage current.

The first is due to the damage region at the back of each sensor, which is caused by the wafer thinning process and further investigated in Section 7.6 and Section 9.1. The second is the final breakdown of the pixel diode, which was described in Section 4.2.

The high defect concentration in the damage region creates additional energy states in the band gap of the substrate, leading to more charge carriers being freed through thermal excitation. When this region is reached by the electric field, more charge carriers are accelerated by the electric field than in a non-damaged silicon substrate. Therefore the leakage current will increase more rapidly during depletion of the damage region. The leakage current will return to a stable increase when the damage region, and therefore the sensor, is fully depleted.

These IV curve features are important to the selection of a suitable HV bias voltage for operation, as a high leakage current leads to a low signal-to-noise ratio. The locations of these sudden current increases is an important variable for defining the acceptance criteria of the IV scan. An early diode breakdown or very high leakage currents are clear indications that a sensor cannot be operated as needed.

7.1.1 The Operating HV Bias Voltage

The data collected by the IV scan can be used to suggest a suitable HV bias voltage for the operation of the sensor in the Mu3e detector, which is referred to as the operating bias voltage in this thesis. The IV behaviour at different bias voltages provides information on a sensor's sensitivity and noise level. It also shows the stability of the sensor's operation at a given bias voltage. A sensor with early breakdown, or with insufficient contact, can be identified through the IV behaviour.

The HV bias voltage chosen for operation must be large enough to ensure a sufficiently large depletion zone. This is crucial for the sensor to fulfil the requirements for efficiency and time resolution, discussed in Section 3.2. However, the higher the HV bias voltage, the higher the leakage current, and therefore the higher the noise. In this context, the rapid leakage current increase in the damage region leads to a sudden increase in noise. Therefore operation before this region is preferable. As the operating bias voltage cannot be individualised for each sensor due to the ladder mounting described in Section 5.1, a suitable operational HV bias voltage must be chosen for all sensors together.

The ideal HV bias voltage for operation is therefore the highest possible HV bias voltage before the depletion reaches the damage region. This will allow the maximum sensitivity possible at low noise currents. Nevertheless, first characterisations showed that the 50 µm sensors can only achieve the efficiency and time resolution targets listed in Chapter 5 at full depletion [42], which corresponds to an operating bias voltage above the damage region on the IV scan. Therefore, the consequent increase in pixel noise is a necessary concession for the efficiency and time resolution requirements, and can be countered using tuning[1] and masking[2].

The most appropriate operating bias voltage for a wafer of sensors therefore depends on the location of the damage region. The accurate location of the damage region is therefore an important step for the analysis of the IV scan, and is done for each sensor thickness separately. The damage region can be found using k-value analysis, and is then used to define an operating bias voltage.

7.1.2 K-Value Analysis

K-value analysis is a useful tool for identifying areas of high variation in a curve [43]. This makes it useful for finding the damage regions of the IV curve shown in Figure 19.

The k-value is given by:

$$K = \left(\frac{|\Delta I|}{|\Delta V|}\right) * \left|\frac{V}{I}\right| \tag{7.1}$$

There is a continuous increase in leakage current with HV bias voltage, due to the increasing electric field strength in the depletion region. If the regular gradient were used to quantify the variation in the curve, this gradual increase could falsely simulate a breakdown, causing the selection of an unsuitable operating bias voltage, and undesirable behaviour in the sensors.

The k-value is an IV gradient scaled by $|\frac{V}{I}|$. Analysis of this adimensional function allows the effects of the damage region and the final breakdown to be separated from the steady increase of the leakage current [43].

The larger the k-value, the larger the variation of the IV scan. To identify areas of high variation in the IV scan, a k-limit is defined. If the k-values in a certain region on the IV scan are above this k-limit, the IV curve is considered to show high variation there. K-voltages are defined as the intercepts of the curve of k-values, the k-curve, with the k-limit. They allow the location of voltages where the IV curve enters a region of high variation. The k-limit is set empirically to a value which identifies the key feature of the curve, while still discriminating small fluctuations. The most suitable k-limit differs between the 50 µm and 70 µm wafers.

Figure 20 highlights how key features of the IV curve appear in the k-curve, which shows k-value against HV bias voltage. The figure shows how a well chosen k-limit can identify areas of high variation. The values of the boundary voltage (marker 1 in Figure 20) and the stabilisation voltage (marker 2 in Figure 20), can be used to define the limits of the damage region, in order to define a suitable operating bias voltage.

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[1] Tuning: the adjustment of single pixel thresholds to reduce noise effects

[2] Masking: The exclusion of a pixel showing a high noise level.

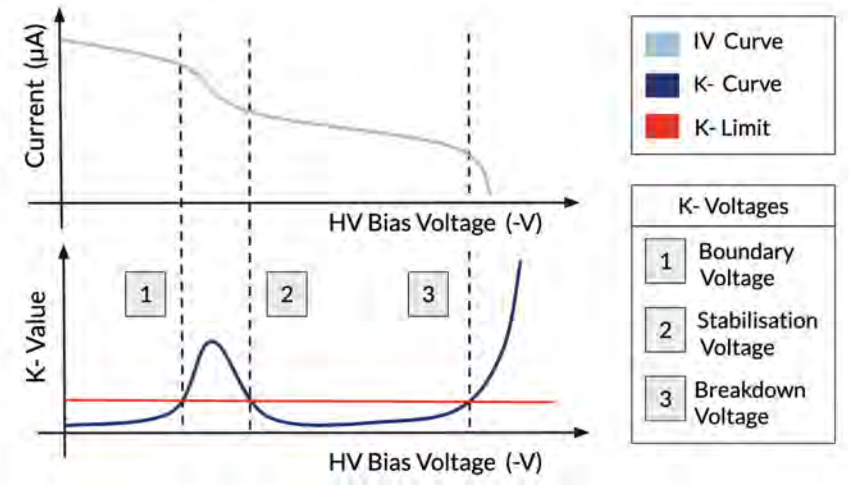

Current (μA)
HV Bias Voltage (-V)
K- Value
HV Bias Voltage (-V)
1
2
3
IV Curve
K- Curve
K- Limit
K- Voltages
1 Boundary Voltage
2 Stabilisation Voltage
3 Breakdown Voltage

Figure 20: Visualisation of the k-value analysis performed on the IV scan.

7.1.3 The Evaluation Criteria for the IV Scan

To be suitable for the Mu3e pixel tracker, and therefore to pass the IV scan, a chip must be able to reach the operating voltage, and show stability there.

A control voltage is used to verify the stability of the chip at the operating bias voltage. If the sensor was in breakdown at the operating bias voltage, the control voltage would not be reached. A control voltage is used to verify the stability because the considerable sensor-to-sensor variation in the boundary and stabilisation voltages renders gradient considerations unreliable for the verification of an IV curve's stability. The general operating voltage may cause some sensors to operate in in their damage regions, and so the gradient at the operating voltage would be high, even though the sensor is functional and stable. The control voltage is therefore defined safely above the stabilisation voltage.

K-value analysis is used to locate the damage region for different sensor thicknesses, to allow the definition of the operating and control bias voltages. The pass criteria are visualised in Figure 21 and summarised in Table 7.1.

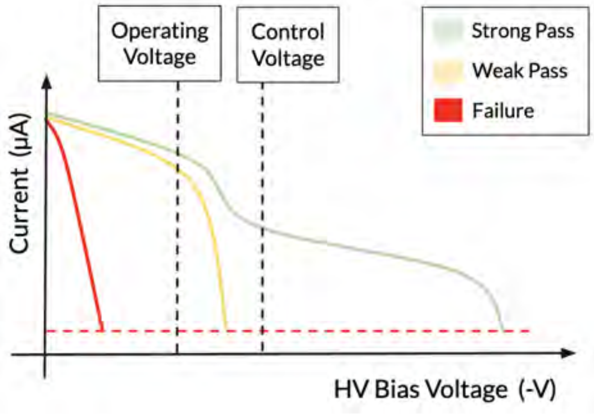

Operating Voltage
Control Voltage
Strong Pass
Weak Pass
Failure
Current (μA)
HV Bias Voltage (-V)

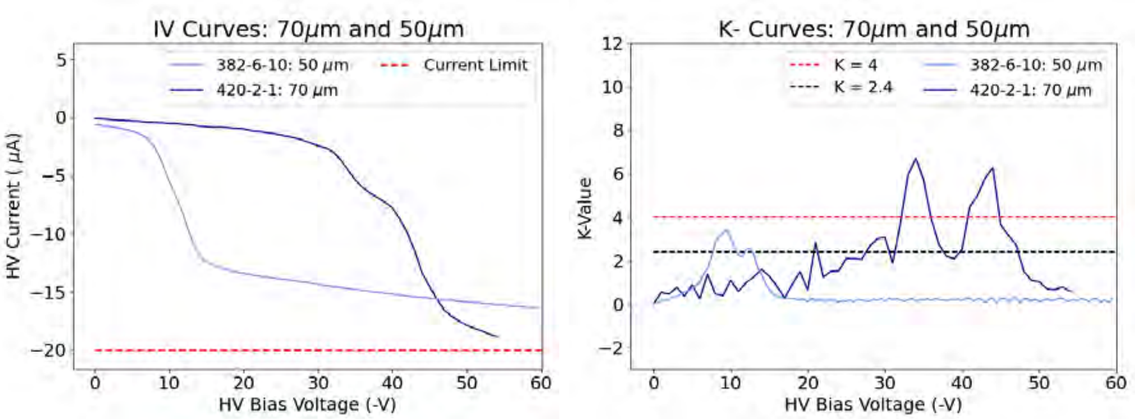
Figure 21: Visualisation of pass criteria for the IV scan, with markers for the operating and control HV bias voltages.

Result	Criteria
Strong Pass	The IV scan reaches the operating and control bias voltages.
Weak Pass	The IV scan reaches the operating bias voltage.
Failure	The IV scan does not reach the operating bias voltage.

Table 7.1: Pass criteria for the IV scan.

7.1.4 Selection of K- Limits

Figure 22 shows the IV scan and k-curve for one 50 µm and one 70 µm MuPix11 sensor, which where chosen to exemplify the effects observed across all four tested wafers.



(a) IV curves

(b) K-curves

Figure 22: Examples of IV and k-curves for two exemplar 50 µm and 70 µm sensors, with the current limit and proposed k-limits marked.

The 50 µm sensor depletes of the damage region at lower bias voltages, which leads to lower current increases due to the lower E-field. The lower current increase for thinner sensors explains why they show less curve variation and so require a lower k-limit to resolve the features of the curve, while thicker chips require a higher k-limit to avoid false noise-induced peaks. The proposed k-limits for each sensor type are listed in Table 7.2.

Chip Thickness	K-Limit
70 µm	4
50 µm	2.4

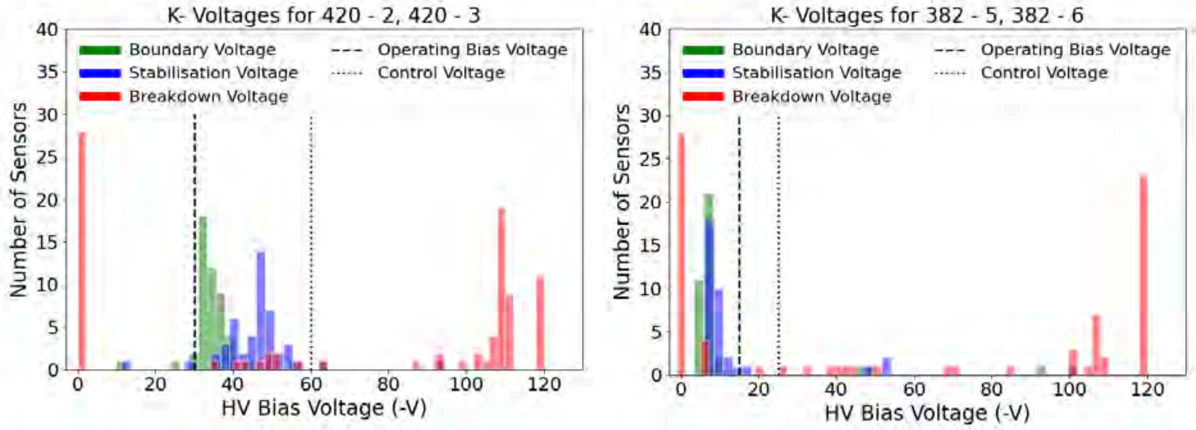
Table 7.2: Proposed k-limits for the IV scan.

Figure 22 shows an unexpected feature: a second current increase in the damage region. The effect is more prominent on the IV scan for 70 µm sensors that for 50 µm sensors. However, the k-curve clearly shows two separate k-peaks, corresponding to two separate regions of current increase, for both 50 µm sensor as well as for the 70 µm sensors.

This two-step current increase can be explained through deeper analysis of the depletion process, which is carried out in Section 9.1.3.

7.1.5 The Evaluation Voltages

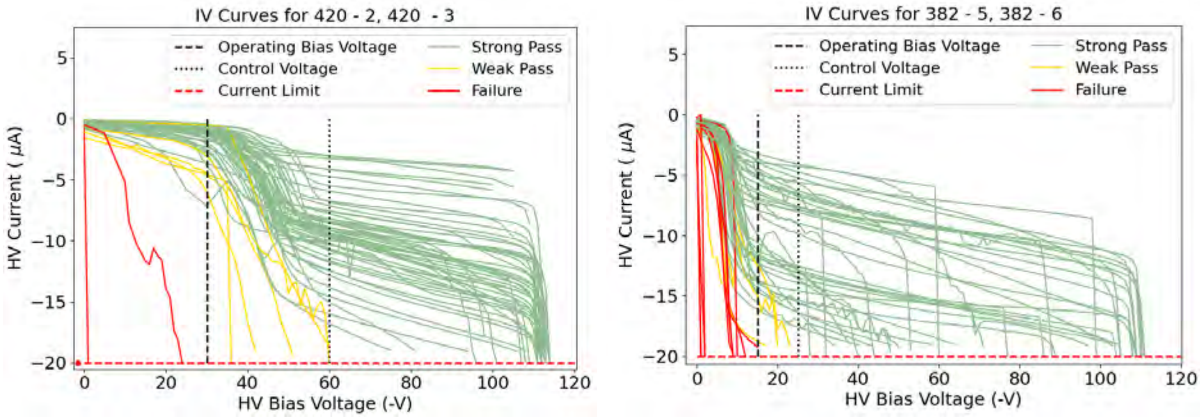
The IV curves of the tested wafers were investigated using k-value analysis. The distributions of k-voltages for each wafer thickness are shown in Figure 23.



(a) K-Voltage Distributions (70 µm) (b) K-Voltage Distributions (50 µm)

Figure 23: Distributions of k-voltages for 70 µm and 50 µm sensors, with proposed operating and control voltages marked.

The boundary and stabilisation voltages mark the beginning and end of the damage region on the IV curve, as shown in Figure 24. The breakdown voltage is defined as the final k-voltage registered before the end of the test. If no k-voltages are detected after stabilisation, the final breakdown does not occur in the voltage range of the test and is the breakdown voltage set to 120 V by default. Figure 24 shows that the damage region is located between −30 V and −60 V for the 70 µm sensors, and −4 V and −18 V for the 50 µm sensors.



(a) IV curves (70 µm) (b) IV curves (50 µm)

Figure 24: IV curves for 70 µm and 50 µm sensors, with proposed operating and control voltages marked.

The proposed evaluation voltages are shown in Table 7.3:

Chip Thickness	Operating Voltage (-V)	Control Voltage (-V)
70 µm	30	60
50 µm	15	25

Table 7.3: Proposed evaluation voltages for the IV scan.

The chosen operating and control voltages for the 70 µm sensors can be set just before and after the damage region as intended. However, the damage region is reached at very low bias voltages for the 50 µm sensors so, as discussed above, operation before the boundary voltage distribution would lead to insufficient efficiency and time resolution. The operating bias voltage is therefore set just after the damage region, at the lowest possible HV bis voltage after full depletion, $-15\,\mathrm{V}$, to limit a further increase in pixel noise. The control voltage is set to 10 V below the operating bias voltage, as sensors which do not recover stability of the leakage current after the damage region do not reach $-25\,\mathrm{V}$. The performance of the MuPix11 sensors in test beam environments was also taken into consideration for the evaluation voltages.

The choice of $-30\,\mathrm{V}$ as the operating bias voltage for the 70 µm sensors is supported by the test beam results [42]. The first test beam characterisation results showed $-30\,\mathrm{V}$ to be the optimum operating bias voltage, as the sensors meet the Mu3e efficiency and time resolution requirements at this voltage, and a further HV bias voltage increase only leads to minimal efficiency improvements and large noise increases.

The results from the test beam characterisation of a 50 µm sensor at a bias voltage of $-15\,\mathrm{V}$ showed limitations in the sensor's efficiency and time resolution, indicating that operation at lower voltages is not possible if the detector requirements are to be met. This supports the proposed operation of the 50 µm sensors after the damage region.

7.2 The LV Power-On Test

The LV power-on test evaluates the power-on of the on-chip circuitry. It is carried out as described in Section 6.2. The off-state is defined by the biasblock being set to 0, and the on-state is defined by a biasblock set to 5, which turns on key elements of the on-chip circuitry discussed in Section 5.4

7.2.1 Evaluation criteria

When powered, the LV current for the on-chip circuitry is an indication of its functionality. A low current would indicate an inability to turn on the circuitry, while a high current is evidence of shorts, which could lead to unreliable behaviour. Based on the observation of LV currents of well-functioning sensors, the MuPix11 are expected to consume a minimum 350 mA of LV current when the on chip circuitry is switched on. A lower current is an indication that not all circuitry components are functional. An LV current above 550 mA is undesirable for the cooling concept of the Mu3e detector. Although the cooling strategy is designed to accommodate a power consumption per unit area of 350 $\frac{\mathrm{mW}}{\mathrm{cm}^2}$ [20], which is more than the MuPix produce at 550 mA, the uniformity of heat dissipation in the detector must be maintained, so sensors with excessive LV currents should not be installed. A high LV current for the on-chip circuitry can also be an indication of shorts on the sensor, which can affect key functions. In addition, the uniformity of power consumption must also be ensured during initial powering of the Mu3e detector. An upper limit of 200 mA is imposed for the LV current at initial powering, so when the sensors themselves are powered, but not the on-chip circuitry.

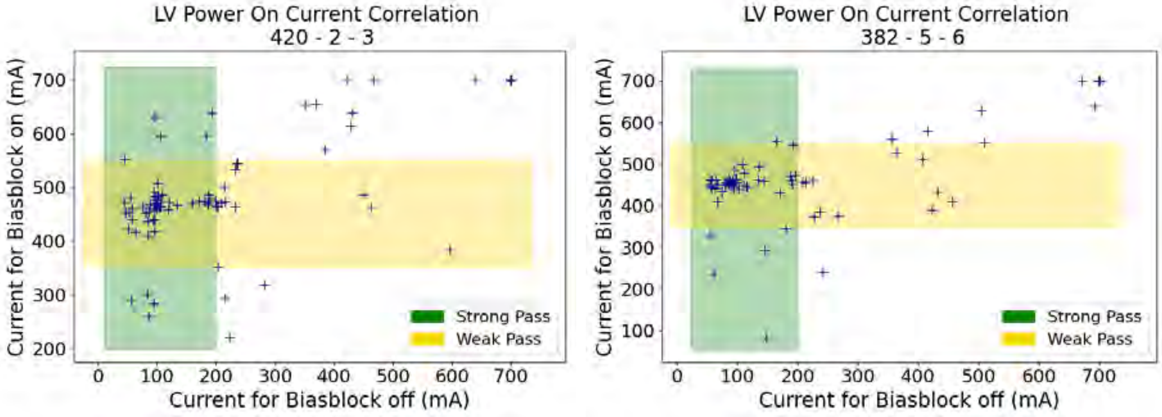
Result	Criteria
Strong Pass	The current before power-on does not exceed 200 mA
Weak Pass	The current consumption after power-on is within the expected range of 350 mA and 550 mA after the power- on.
Failure	The requirement for the weak pass is not fulfilled

Table 7.4: Evaluation criteria for the LV power-on test.

7.2.2 LV Power-On Results

Figure 25 shows the correlations of LV current before and after power-on of the on-chip circuitry. There does not seem to be a considerable difference in the powering behaviour between 50 µm and 70 µm sensors.

All sensors within the yellow bar passed the LV power-on test. Sensors below the yellow bar could not turn on the on-chip circuitry, and sensors above the yellow bar consumed excessive current due to damages. Sensors in the overlap between the yellow and green bars passed with a strong pass. The high concentration of sensors in the strong pass region show that most functional sensors also fulfil the strong pass criteria. The strong pass yield could be improved by raising the upper current limit for the LV current consumption before powering. The total LV power-on yield could be improved by raising the maximum accepted current after powering. The possible exclusion of functional sensors by the limits of the LV power-on test is discussed in Section 9.2.1.



(a) Correlation for the 70 µm Sensors (b) Correlation for the 50 µm Sensors

Figure 25: Correlations of LV currents before and after switch-on of the on-chip circuitry for 50 µm and 70 µm Sensors.

Before the work of this thesis the power-on was evaluated using the difference in LV current before and after the powering of the on-chip circuitry. Figure 25 shows why this method was inherently flawed. Sensors with inherently high LV current and damage to the on-chip circuitry can show the same current difference as a functional sensor. A chip with a current increase of 450 mA to 700 mA after powering does not fulfil the requirements of the detector for uniformity of heat dissipation. Evaluation using the LV current difference would categorise this sensor as just as functional as a sensor with an LV current increase from 150 mA to 400 mA after powering. Furthermore, evaluation with the current difference loses the information on the type of damage causing the failure. No increase in the LV current is evidence for a failed power-on when the LV current remains low, and the presence of shorts when the LV current was high to begin with.

Evaluation using the currents before and after powering looks for the exact powering behaviour required for operation. However, the information provided by this test on the exact cause of the power on failure is still limited, which is further addressed in Section 9.2.2.

7.3 The Internal Voltages Test

The internal voltages test evaluates the success of the voltage optimisation algorithm described in Section 5.3. The test is carried out as described in Section 6.2, with the target voltages listed in Table 7.6. The VDDD and VDDA are the supply voltages for digital and analogue circuitry, respectively, and the VSSA is the supply voltage for the amplifier.

7.3.1 Evaluation Criteria

The internal voltages test should evaluate if a sensor's internal voltages can be optimised, to correct for resistances between voltage supply and the sensor's internal power grid. A functional sensor will receive the target voltage at the internal power grid after optimisation. Minimum and maximum accepted voltages are defined to accommodate small fluctuations from the target voltage. The tolerance of $-0.05\,\mathrm{V}$ is intended to accommodate measurement errors due to resistance in the sense line, while the allowance for higher voltages is larger, at $0.15\,\mathrm{V}$, because target voltage is concipated as a lower limit and variations to slightly higher voltages do not limit sensor functionality. The upper limit was set empirically, as sensors with very high final voltages also do not show the ability to set a target voltage, and should therefore be excluded.

Result	Criteria
Strong Pass	The LV current is between 350 mA to 550 mA after the voltage optimisation.
Weak Pass	All three on- chip voltages are within the minimum and maximum voltages listed in Table 7.6.
Failure	The requirement for the weak pass is not fulfilled.

Table 7.5: Evaluation criteria for the internal voltages test.

The weak pass criteria verifies that the voltage optimisation algorithm is functional. The strong pass criteria evaluates if the LV current reflects regular operation after the optimisation. Some fluctuation in the current after optimisation is normal and expected. The purpose of the algorithm is to apply a set voltage and correct for differences in routing resistances, which can lead to small differences in the final current. However, low currents after optimisation can be a sign that the on-chip circuitry is not consuming enough power, and very high currents after optimisation could be due to shorts. Both of these issues will affect the behaviour of the sensor and are limitations to its ability to set the internal voltages.

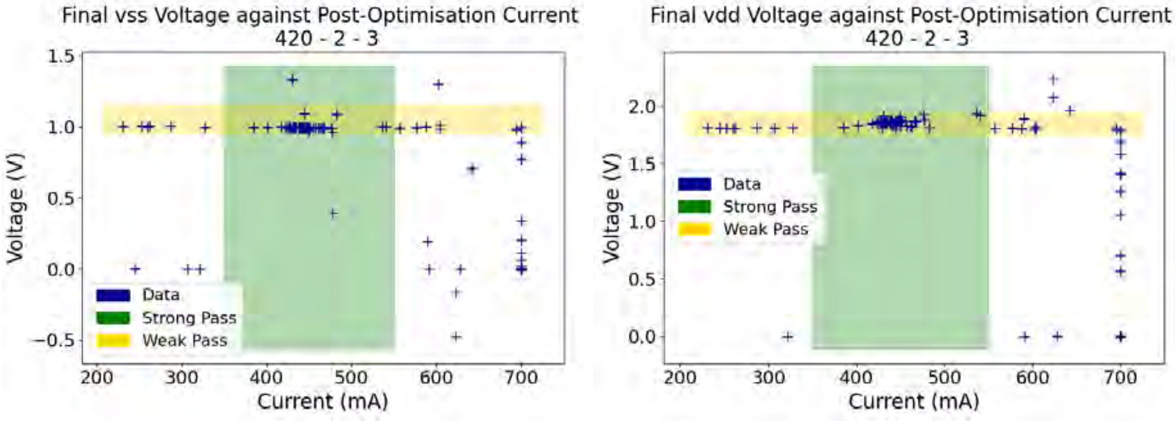
Internal Voltage	Chip Thickness [μm]	Target Voltage [V]	Minimum Voltage [V]	Maximum Voltage [V]
VSSA	50	1.1	1.05	1.25
VSSA	70	1.0	0.95	1.15
VDDD/VDDA	50	1.8	1.75	1.95
VDDD/VDDA	70	1.8	1.75	1.95

Table 7.6: Target values for the internal voltages, each with a maximum and minimum accepted voltage defined by the tolerance of $-0.05\,\mathrm{V}/+0.15\,\mathrm{V}$.

The difference in the VSSA target voltage between the chip thicknesses is not a technical effect but a consequence of changes to the testing strategy. After the tests of the 70 µm sensors the target voltage was increased to 1.1 V to ensure that the test is carried out in the operational voltage range of the amplifier. The threshold voltage for the amplifier's operational range is referred to as the activation voltage throughout this thesis. The amplifier activation voltage was not definitively known at the time of testing. The target voltage was therefore increased to 1.1 V, to ensure that the activation voltage would be reached even if it were higher than the estimated maximum of ~1.0 V. This was done to ensure that the amplifier is at working point during the internal voltages test.

7.3.2 Internal Voltages Results

Figure 26 shows the correlations of final voltages and LV currents after the voltage optimisation (post-optimisation currents) for VSSA and VDDD, for sensors of 70 µm thickness. The correlations for 50 µm sensors are very similar to those of 70 µm sensors.



(a) Final VSSA voltage against post- optimisation current

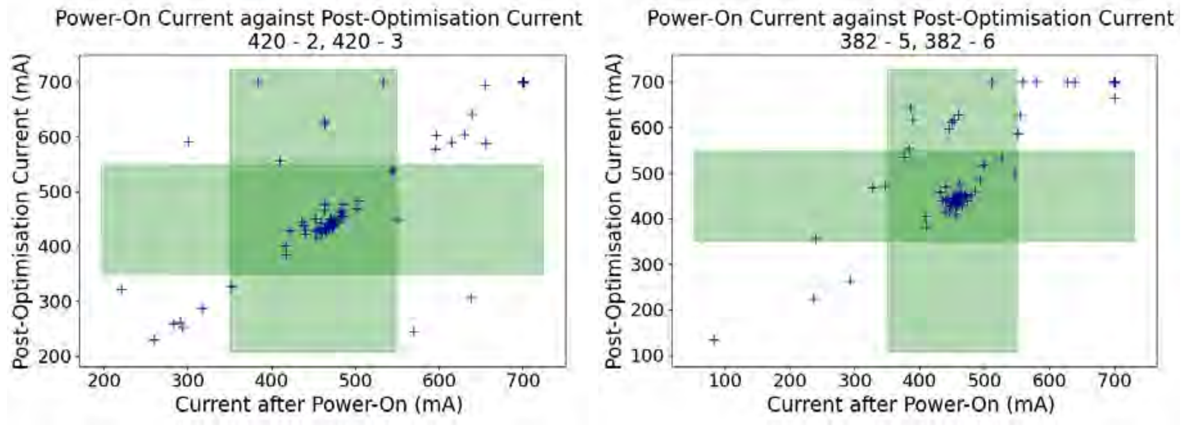
(b) Final VDDD voltage against post- optimisation current

Figure 26: Correlations of final VSSA and VDDD voltages against the post- optimisation currents for 70 µm sensors, with the areas marked in which the pass criteria are fulfilled.

The sensors marked in the yellow bar pass the internal voltages test. Only very few sensors with a suitable LV current could not successfully optimise their supply voltage. The sensors in the overlay of the two bars show a strong pass. There is a clear concentration of sensors in the strong pass region, but a significant amount of successfully optimised sensors despite unsuitable LV currents, which is indicative of a contact error. This will be discussed in detail in Section 8.1 and Section 9.2.

7.3.3 The LV Current after Voltage Optimisation

The effect of the optimisation algorithm on the LV current gives information on the functionality of the sensors. Figure 26 shows the current consumed by the sensors in directly powering of the on-chip circuitry, and after the voltage optimisation.



(a) 70 µm

(b) 50 µm

Figure 27: Correlations of the post-optimisation currents against the default current after switch-on for 50 µm and 70 µm Sensors.

The green bars mark the regions of strong pass criteria. It should be noted that the plot does not show which sensors passed the weak criteria as the purpose of this plot is to evaluate the effect of the voltage optimisation on the current consumption. There is a clear grouping of strong chips in the centre of the plot. This shows that most of the sensors with suitable LV current before optimisation, also show a suitable LV current after optimisation. The LV current after optimisation is approximately equal to the LV current before optimisation, but some sensors with suitable currents after the power-on, showed raised currents after the voltage optimisation. This is an indication of unusually high routing resistance, and could be a sign of damaged circuitry or insufficient contact. Some few sensors with a low LV current after the power-on showed an LV current in the correct range after the voltage optimisation. The voltage optimisation showed that these sensors failed LV power-on test due to high resistances between the voltage supply and the sensors' internal grids, perhaps due to insufficient contact, not due to limited functionality. The possibility of recovering is described in Section 8.2.

7.4 The VDAC Scan

The VDAC scan observes the sensors' ability to set key DAC Values in the chip, which set operational voltages, the purposes of which are discussed in Section 5.4. The test is carried out as described in Section 6.2, with following parameters:

- Tested DAC range for BLPix, Baseline and ThHigh: 90 - 120
- DAC measurement interval for BLPix, Baseline and ThHigh: 5
- Tested DAC range for VSS1 and VSS2: 140 - 210
- DAC measurement interval for VSS1 and VSS2: 10

The range of tested DAC values was chosen to include the DAC values considered as the most relevant for operation. The DAC value for each VDAC is increased in set intervals, and the voltage applied by the DAC and current are measured at each step. The output of the VDAC scan therefore includes a scan of voltage against DAC value, referred to as the voltage scan, and a scan of current against DAC value, referred to as the current scan. The connection for the ThLow configuration was damaged at the time of these pre-production tests, and therefore there are no results for this VDAC at this stage in testing. Results from later tests, presented in Section 9.6, will include results for ThLow.

7.4.1 Evaluation criteria

The VDAC test is evaluated using criteria for the voltage scan. The current scan gives further information on the response of the sensors to the VDAC settings but is not used for evaluation at this stage.

A functional sensor will show a linear increase in the applied voltage with DAC setting. The VDACs can set the applied voltage from 0 V to 1.8 V. The increase in applied voltage per digital DAC value is given by the total voltage range of 1.8 V divided by the maximum value of 256 for these DAC settings. The expected gradient for the voltage scan is therefore 7.03 mV for every VDAC tested in the quality control procedure[3].

Therefore, for a sensor to pass the VDAC scan, the voltage scan must show a gradient within an error margin of ± 2.0 mV of the target gradient of 7.0 mV. The error margin was empirically set to 2.0 mV to allow for the range of gradients observed in the voltage scans. The voltage scan must also reach a lower voltage limit of (0.5 V) at a sample DAC value close to the beginning of the voltage scan, to exclude sensors which apply too low voltages.

The strong pass requires the sensors to show a low deviation for the voltage scan, as an uneven applied voltage increase with DAC value could suggest that some DAC values were set incorrectly. The deviation is defined as the standard deviation of residuals about the least squares regression line of the voltage scan, and is also referred to as the root mean square (RMS) deviation.

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[3] It is important to note that this does not apply for all VDACs on the MuPix11.

The DAC scan inherently contains an significant RMS deviation. The voltage scan appears linear when the DAC values are arranged in order of magnitude, but the DAC values are discrete variables. The voltage scan is not continuous, but rather a step- wise increase of applied voltage in response to each DAC value. This means that there is an inherent deviation from the least-squares regression line. A deviation below 7 mV shows that each DAC value was set correctly, as a wrongly set DAC value would cause a deviation from linearity above 7 mV. The deviation target for VSS1, VSS2 and BLPix are set to 14 mV because observation of the VDAC behaviour showed that functional sensors also show high deviations for these VDACS. This is discussed in detail in Section 7.4.3.

Table 7.7 and Table 7.8 show the evaluation criteria for the VDAC scan. The same grading parameters are used for the voltage scans of 70 µm and 50 µm sensors.

Result	Criteria
Strong Pass	1. The linearity deviation does not exceed the maximum listed in Table 7.8.
Weak Pass	1. The linearity constant lies within an error margin of ± 2.0 V of the target gradient of 7.0 V 2. The starting voltage exceeds the minimum listed in Table 7.8
Failure	1. The criteria for the weak pass are not fulfilled.

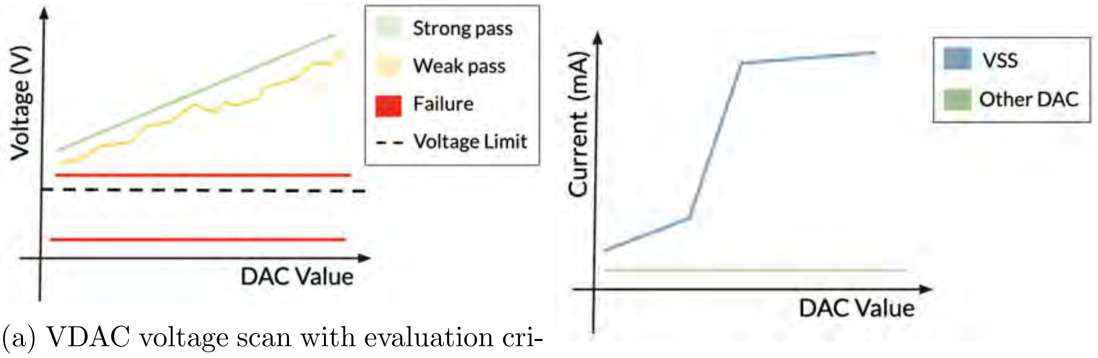
Table 7.7: Evaluation criteria for the VDAC voltage scan

VDAC	Gradient Range (mV)	Sample DAC Value [dec]	Lower Voltage Limit (V)	Maximum Deviation (mV)
VSS1/VSS2	5 - 9	150	0.5	14
BLPix	5 - 9	100	0.5	14
Other	5 - 9	100	0.5	7

Table 7.8: Evaluation Parameters for the VDAC Voltage Scan

Figure 28a visualises the evaluation criteria on the voltage scan. Figure 28b shows the expected result of the VDAC current scan for functional sensors. The current scan shows a characteristic S-curve for VSS1 and VSS2. These two measurements represent the voltage supply for the signal amplifier, regulated by the VDAC ref_VSS, as it arrives on the two sensor partitions, 1 and 2. At low ref_VSS the amplifier is not in the operational range. As the supply voltage to the amplifier, and therefore VSS1 and VSS2, increases, the amplifier reaches working point, and contributes to the LV current. This causes the sudden current increase. The voltage at which the amplifier reaches the operational range is marked by the stabilisation of the LV current, and is referred to as the activation voltage in this

thesis. The amplifier reaching the operation range is referred to as its activation.
The current is not used for evaluation in the single chip QC. However, the MuPix11 ladders can only provide information on the power consumption of the sensors, and not read out the individual voltages applied on the sensors. The ladder quality control procedure will have to define new criteria for the VDAC scan, based only on the current scan. The single chip QC presents a good opportunity to understand the defining features of a current VDAC scan for a functional sensor, to allow the informed definition of QC criteria for future ladder quality control procedures.



(a) VDAC voltage scan with evaluation criteria

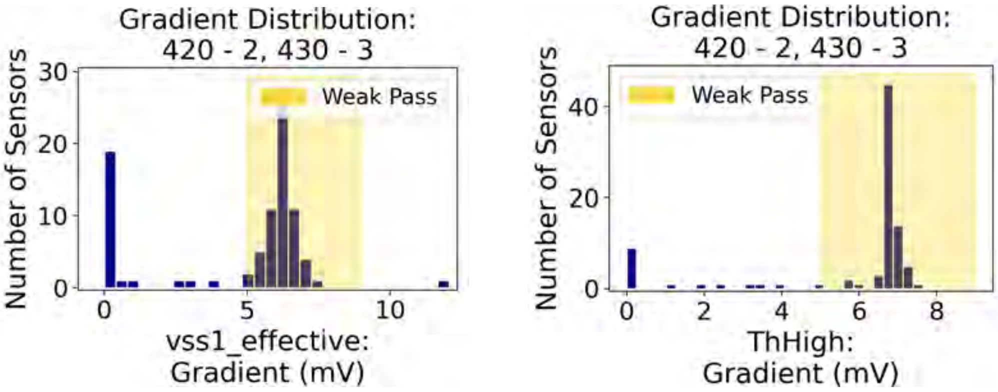
(b) The VDAC current scan

Figure 28: Visualisation of the VDAC voltage scan, highlighting the evaluation criteria, and the current scan, demonstrating the amplifier switch-on.

The current scan also offers valuable information on the function of the sensor's amplifier. The activation voltage can be deduced from the current scan by reading out the DAC value at the beginning of the current plateau, see Figure 28b. The activation voltage is the voltage applied at this DAC value. The plateau gradient of the current scan can also be observed to investigated the stability of the amplifier after activation.

7.4.2 VDAC Voltage Dependency

The gradients of the voltage scans were calculated for each DAC value. The gradients for VSS1 and ThHigh, for the 70 µm sensors, are shown in Figure 29.



(a) Gradient distribution for VSS1

(b) Gradient distribution for ThHigh

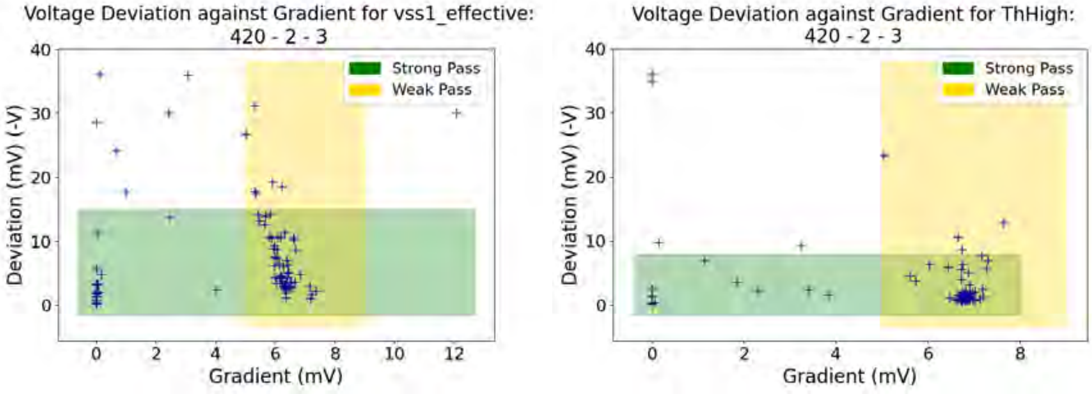
Figure 29: Gradient distributions for a) VSS1 and b) ThHigh, for 70 µm sensors.

The gradient and RMS deviation of the least squares regression line was determined for each sensor individually, and then these values were averaged for each wafer separately. Only sensors which fulfilled the VDAC criteria were included in these averages, because the aim is to understand the effect of the VDAC settings on the applied voltage for functional sensors. This will help to adapt the pass criteria in Section 9.6. Table 7.9 shows the resulting averages.

VDAC	Gradient Target ($\frac{\text{mV}}{\text{DAC}}$)	Deviat. Limit (mV)	70 µm Gradient (mV/DAC)	70 µm Deviation (mV)	50 µm Gradient (mV/DAC)	50 µm Deviation (mV)
VSS1	7	14	5.85 ± 1.24	8.87 ± 8.23	5.74 ± 1.71	8.58 ± 8.72
VSS2	7	14	5.85 ± 1.29	8.83 ± 7.66	5.73 ± 1.72	8.84 ± 9.37
BLPix	7	14	6.08 ± 1.47	10.83 ± 4.63	5.28 ± 2.37	11.20 ± 6.92
Baseline	7	7	6.88 ± 0.33	2.34 ± 2.53	6.90 ± 0.33	1.60 ± 1.82
ThHigh	7	7	6.78 ± 0.34	2.69 ± 3.46	6.84 ± 0.24	2.46 ± 5.02
ThLow	7	7	-	-	-	-

Table 7.9: Mean values for the gradients and RMS deviations from linearity for the VDAC voltage scan for each DAC value, for functional 50 µm and 70 µm sensors from all four wafers.

There are two distinct categories of VDACs which show a different effect on the voltage applied: VSS1, VSS2 and BLPix show similarity, and Baseline shows similarity to ThHigh. VSS1, VSS2 and BLPix show low gradients and high deviations. ThHigh and Baseline show gradients closer to the target value of 7 mV/DAC. They also feature deviations below their voltage scan gradient value, which demonstrates that functional sensors could set their DAC values correctly. The deviation-gradient correlations presented in Figure 30 show that functional sensors with lower VSS1 gradients have higher VSS1 deviations. The gradients for ThHigh are concentrated close to 7 mV/DAC, and show less deviation.



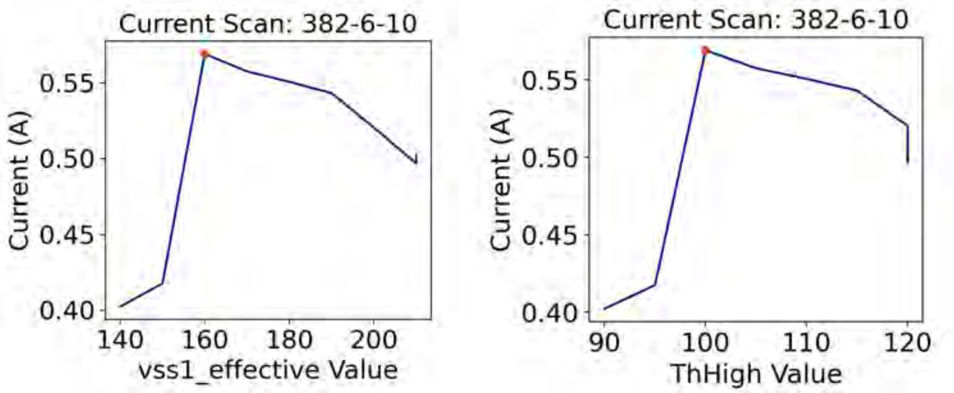
(a) Deviation- gradient correlation VSS1 (b) Deviation- gradient correlation ThHigh

Figure 30: Correlations of the voltage rms deviation against the voltage gradient for VSS1 and ThHigh DACs, for 70 µm sensors.

The high deviation shown by VSS1, VSS2 and BLPix suggests that the a linear increase is not the right model for the voltage scans of these DACs. There appears to be a different voltage response to these DACs than expected. This will be discussed further in Section 9.6, which describes improvements made to the VDAC scan procedure.

7.4.3 The Current Scan

The current scan shows the change in LV current in response to changes in the DAC values. Figure 31 shows two current scans for a 50 µm sensor.



(a) VSS1 Current Scan for 50 µm (b) ThHigh current scan for 50 µm

Figure 31: VDAC current scans for a) VSS1 and b) ThHigh, for a 50 µm sample sensor.

All functional sensors showed a similar current scan. The key features of the curve are better visible on a single plot, so one sensor is presented to exemplify the output of the current scan. The red circle marks the point recognised as the activation by the analysis code. This is the DAC value which determines the activation voltage.

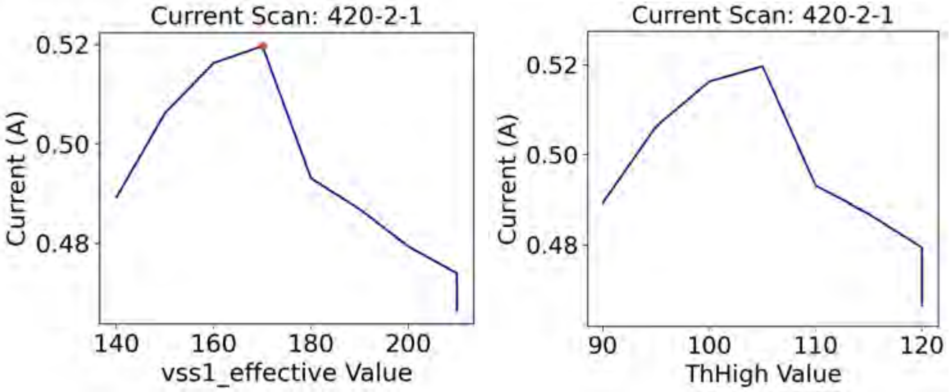
Figure 31 shows that the current scan does not show the expected S-curve that is characteristic of the amplifier reaching the operational range. The amplifier itself demonstrates functionality in the characteristic current increase in the current scans. However, after the amplifier is activated, the voltage decreases. There is no plateau after activation.

Additionally, both current scans show the current increase due to amplification, even though this is a process that only affects VSS1 and VSS2. The current scan for ThHigh should be linear.

These uncharacteristic results are due to the testing procedure of the VDAC scan. The scans presented in this section were carried out simultaneously. They therefore show the effect of multiple DACs being changed at once. The LV current increases with VSS1 and VSS2, but decreases with the thresholds, ThHigh and ThLow. The information on the effect of individual DAC changes is lost. The VDAC scan procedure will be changed to allow separate analysis of the individual DACs in Section 9.6.

The current decrease at higher VDAC values is due to the threshold DACS, ThHigh and ThLow. At low thresholds, a lot of noise is observed, increasing the current consumption.

At higher thresholds, the amount of detected noise decreases, and the LV current will drop.
Figure 32 shows that, for 70 µm sensors, the scan starts midway through activation.



(a) VSS1 current scan for 70 µm (b) ThHigh current scan for 70 µm

Figure 32: VDAC current scans for a) VSS1 and b) ThHigh, for a 70 µm sample sensor.

The scan should therefore be amended to start at lower DAC values, as is discussed in Section 9.6. This will allow the activation of the amplifier to be resolved better in future scans.

7.4.4 The Activation Voltage

The issues with the VDAC scans due to simultaneous DAC changes, discussed above, will have affected the measured activation voltage.
The measured activation voltages from the pre-production quality control tests are listed in Table 7.10, but these values should not be considered as accurate due to the inherent problems with the VDAC scan. The activation voltages presented in Section 9.6 more accurately reflect the behaviour of the amplifier.

	Average Activation Voltage $\mu \pm \sigma$ (V)	
VDAC	70 µm	50 µm
VSS1	0.91 ± 0.08	0.87 ± 0.09
VSS2	0.91 ± 0.09	0.88 ± 0.10

Table 7.10: Average activation voltages for functional sensors for 70 µm and 50 µm.

7.5 LVDS Links

The LVDS links test evaluates a sensor's ability to transmit data without 8b/10b errors. The test is carried out as described in Section 6.2, with following parameters:

- VNVCO values: 13, 18, 23, 28, 33, 38
- VPVCO values: 12, 17, 22, 27, 32, 37
- High threshold: 138/137
- Low threshold: 118/117

7.5.1 Evaluation criteria

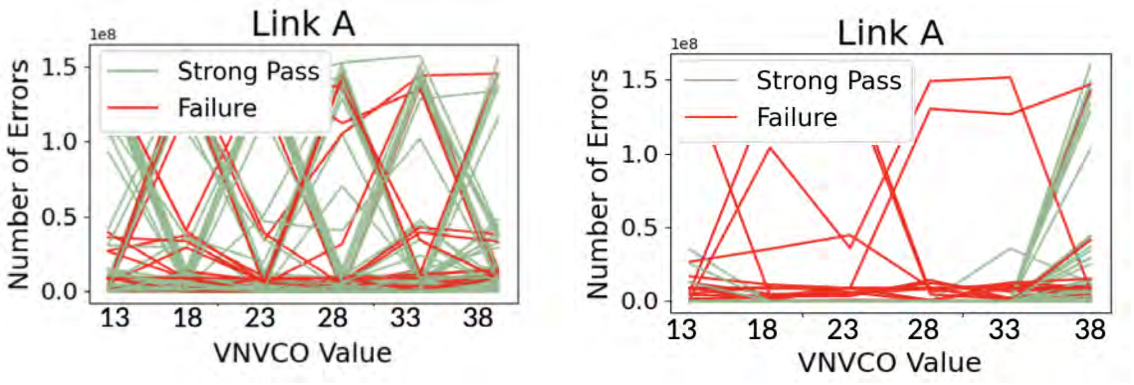
The Evaluation criteria for the LVDS links test must evaluate if a sensor can transmit data without errors. This means that there must be at least one VPVCO (VNVCO) setting at which all links transmit data without 8b/10b errors. In the test, both the VNVCO and VPVCO values are changed, but VPVCO is the DAC which changes the VCO setting.

Result	Criteria
Strong Pass	There is at least one VPVCO (VNVCO) value, for which no errors are recorded across all links at the default comparator threshold.
Weak Pass	There is at least one VPVCO (VNVCO) value, for which no errors are recorded across all links at the increased comparator threshold.
Failure	The criteria for the weak pass are not fulfilled.

Table 7.11: Evaluation criteria for the LVDS links test.

7.5.2 Results of the LVDS links test

Figure 33 shows the error rates for link A, for the 50 µm sensors. The plots for the other links are very similar. The differences in LVDS behaviour between 50 µm and 70 µm sensors are better visualised in other plots and will be presented later in this section.



(a) Link errors at default Threshold (b) Link errors at increased Threshold

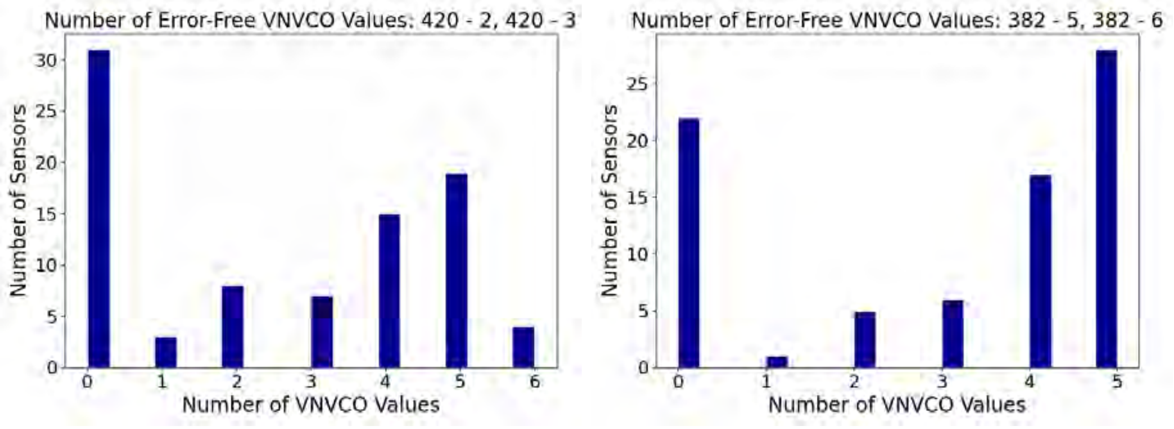
Figure 33: Link errors for 50 µm sensors.

Figure 33a shows that the default threshold of ThHigh=118/ThLow=117 chosen for the test was below the noise level, while the increased threshold of ThHigh=138/ThLow=137 did not show these noise effects. As the Baseline was set to 112, this means that the noise level was between the two corresponding effective thresholds of 42 mV and 182 mV. The effective threshold is the difference between the DAC values for the threshold and the Baseline, multiplied by the voltage increase per DAC value of ∼7 mV.

The data readout at the default threshold was therefore dominated by errors caused by noise. This is further evidenced by the fact that sensors which function well at the increased threshold show a similar amount of errors to the failed sensors at the default threshold. In addition, many functional sensors do not succeed in error-free data transmission for a VPVCO (VNVCO) of 37 (38).

As the scan at the default threshold did not contain information as to the success of the sensors' read-out, the criteria were adapted. The criteria for the strong pass, which depended on the result of the scan at default threshold was removed. Therefore every sensor that failed to transmit data without errors failed, and every sensor that succeeded in data-free error transmission at the increased threshold passed with a strong pass.

The distributions shown in Figure 34 show that sensors with functional links mostly function for multiple VPVCO (VNVCO) values. This information is useful for construction, because operating a ladder of sensors at the same VPVCO (VNVCO) value will reduce the single- chip configuration necessary for the final detector. The plot also shows that the 50 µm sensors show better LVDS link performance than 70 µm sensors. There are fewer failures, and more sensors with many functional VPVCO (VNVCO) settings.



(a) Distribution for 70 µm sensors

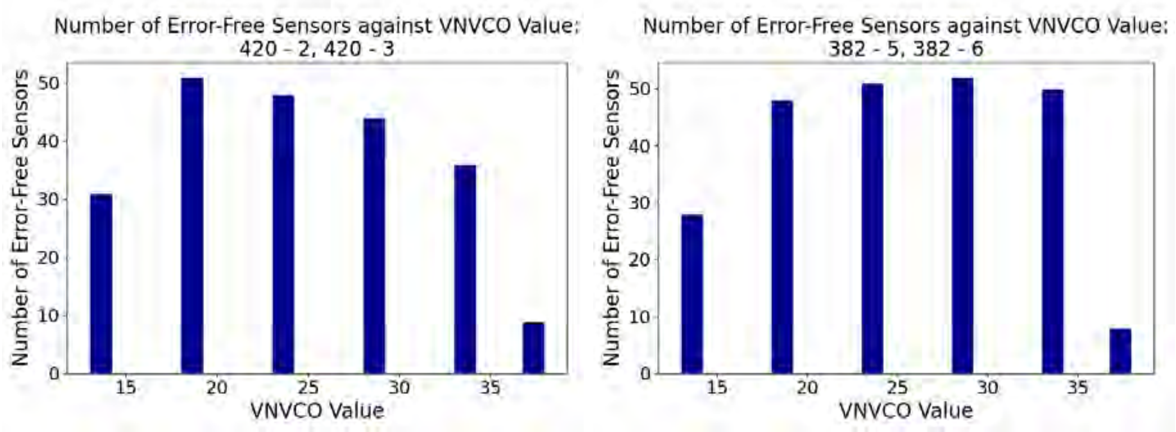
(b) Distribution 50 µm sensors

Figure 34: Distribution of error- free VPVCO (VNVCO) values, for 50 µm and 70 µm sensors.

7.5.3 Effect of Sensor Thickness on the Error Rate

Figure 35 shows the number of sensors without 8b/10b encoding errors for different VPVCO (VNVCO) values, for 50 µm and 70 µm sensors. The 70 µm sensors showed fewer

8b/10b errors at low VPVCO (VNVCO) values, with a VPVCO (VNVCO) value of 18 showing the least 8b/10b errors in transmission. In comparison, the 50 µm sensors showed fewer 8b/10b errors at higher VPVCO (VNVCO) values, with the most reliable VPVCO (VNVCO) value being 28. The analysis of the error-rates during data transmission at different VNVCOs (VPVCOs) provides useful information for detector construction, because it allows informed selection of VPVCO (VNVCO) settings for operation.



(a) Distribution for 70 µm sensors

(b) Distribution for 50 µm sensors

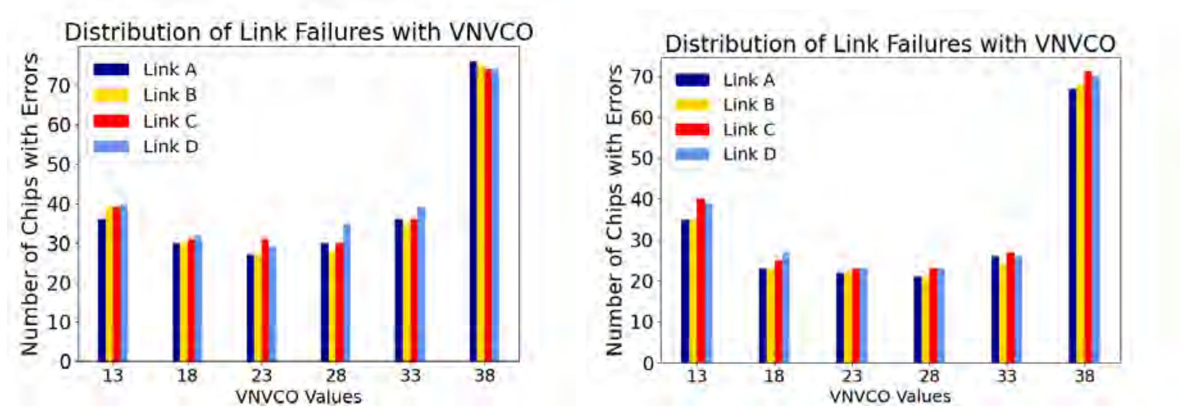
Figure 35: Number of error-free sensors for each VPVCO (VNVCO) value, for 50 µm and 70 µm sensors.

There were more contact issues for the 70 µm sensors at this stage in testing, as will be discussed in Section 8.1. As failure of the LVDS links test can be caused by poor contact at the LVDS links connector pads, and the sample size for this data is still low, these distributions should be considered as preliminary. Figure 35 shows that some VPVCO (VNVCO) values, such as 38, have a significantly lower rate of error-free data readout than others. This information introduces the possibility of optimising the LVDS test for the production-phase quality control tests by prioritising the test of VPVCO (VNVCO) values with a higher read-out success rate. This is discussed in section Section 9.7.

7.5.4 Link Performance

The LVDS links test also allows us to investigate and compare the performance of the individual links to investigate if specific links fail more frequently and limit the overall LVDS yield. Figure 36 shows the distributions of link failures (8b/10b errors present in the transmission for this link) for each of the links in comparison.

The distributions of error rates were analysed in detail, as shown in Table 7.12. The number of links is too small to generate informative μ and σ values. However, by finding μ and σ for the links and excluding the worst value, the skewing of the statistics by the value to be observed was reduced. While the sample size of observed sensors limits the informative value of this analysis, the consistency in the relative error-rates allows us to nevertheless draw meaningful conclusions. The relative link error rates at a VPVCO (VNVCO) of 37 (38) are not considered, due to the general high error-rate at this value.



(a) Distribution of link failures: 70 µm

(b) Distribution of link failures: 50 µm

Figure 36: Link failures for each VPVCO (VNVCO), for 50 µm and 70 µm sensors.

	70 µm				50 µm			
VPVCO (VNVCO)	Worst Link	value	$\mu \pm \sigma$ of other links	Dev. from μ	Worst Link	value	$\mu \pm \sigma$ of other links	Dev. from μ
13	D	40	38.0 ± 1.4	$1.4\ \sigma$	C	40	36.3 ± 1.9	$1.9\ \sigma$
18	D	32	30.7 ± 0.5	$2.6\ \sigma$	D	27	23.7 ± 0.9	$3.7\ \sigma$
23	C	31	27.7 ± 0.9	$3.5\ \sigma$	C/D	23	22.0 ± 0.0	-
28	D	35	29.3 ± 0.9	$6.3\ \sigma$	C/D	23	21.0 ± 0.0	-
33	D	39	35.7 ± 0.5	$6.6\ \sigma$	C	27	25.3 ± 0.5	$3.4\ \sigma$
38	A	76	74.3 ± 0.5	$3.4\ \sigma$	C	71	68.3 ± 0.7	$3.9\ \sigma$

Table 7.12: Deviation calculations for the worst links for 50 µm and 70 µm sensors

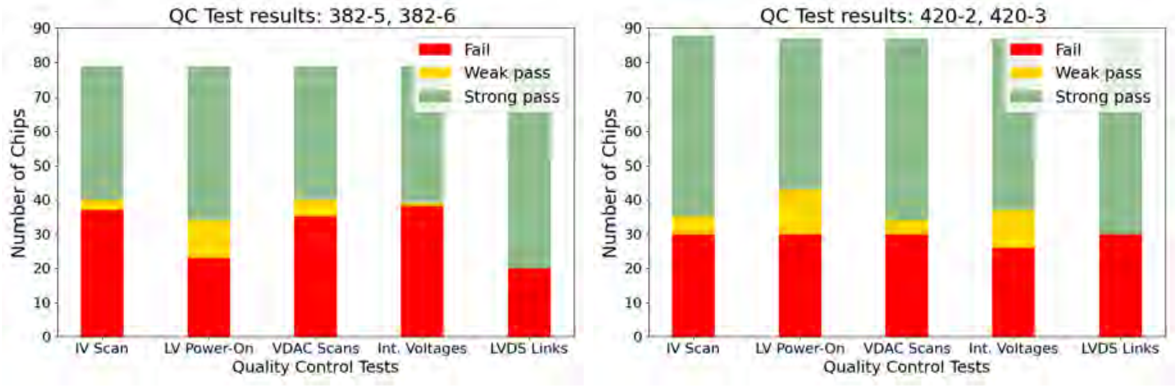
Links C and D consistently show a higher error rate than Links A and B for both 50 µm and 70 µm sensors. The high error rate for Link C (also referred to as Link 2) were also observed for previous MuPix designs, such as MuPix8 [20]. This leads to the conclusion that they are inherent to the links themselves, and not the consequence of different contact qualities between the link connector pads and needles in the probe card.

There are power drops in the internal circuitry across the LVDS links. Link C therefore experiences less voltage than links A and B, which can correspond to a lower internal clocking frequency, leading to more misalignment errors. The higher error-rate for links C and D is therefore inherent to the design of the sensors and their failure profile.

This is important information for the quality control procedure quality control procedure because the high error rates for links C and D could be interpreted as set-up issues by the operator. This behaviour is chip-internal and does not require re-testing or amendments to the setup.

7.6 Preliminary Yield

The pass rates for the individual quality control tests, for 50 µm and 70 µm sensors are visualised in Figure 37, and listed in Table 7.13.



(a) 50 µm

(b) 70 µm

Figure 37: Preliminary yields for the individual quality control tests, for 50 µm and 70 µm sensors.

	50 µm Yield (%)		70 µm Yield (%)	
Test	Strong	Weak	Strong	Weak
IV Scan	49.4	53.2	60.2	65.9
LV Power-On	57.0	70.9	50.6	65.5
Internal Voltages	50.6	51.9	57.5	70.1
VDAC Scan	49.4	55.7	57.5	65.5
LVDS Links	74.7	74.7	65.5	65.5

Table 7.13: Preliminary yields for the individual quality control tests, for 50 µm and 70 µm sensors.

The quality control yield for the 70 µm sensors is limited by the LV power-on test. This test is selective, but the cause for this low yield is likely to be contact issues for wafer 420-2, not a limited sensor functionality, as will be discussed in Chapter 8. This is also likely the cause for the lower yield for the LVDS links test, which showed a high yield, relative to the other quality control tests, for the 50 µm sensors, suggesting that the read-out mechanism itself has a low failure rate.

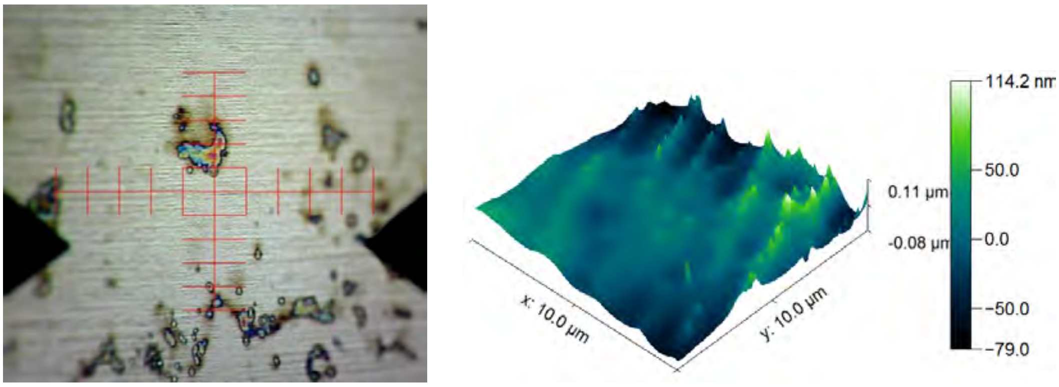
The quality control yield for the 50 µm sensors is limited by the IV and VDAC scans. The VDAC scan showed inherent problems to the simultaneous testing of the VDACs. Section 9.6 will discuss how this is improved, and also present a detailed failure analysis to identify which VDACs are limiting the VDAC scan yield. The low yield for the IV scan is due to the depletion of the damage region to achieve maximum sensitivity for the 50 µm sensors. Some sensors do not show stabilisation of the leakage current after the damage region. The possibility of lowering the operating bias voltage for 50 µm sensors

to increase the yield could be investigated further, as the test beam results only represent one sensor, and analysis with a larger sample size may show improved efficiency at lower HV bias voltages. If this is not the case, the low IV yield for 50 µm sensors will remain a necessary concession for high precision in the Mu3e experiment.
The preliminary total quality control yields are listed in Table 7.14, with the results shown separately for each wafer, as well as averaged for each sensor thickness.

Sensor Type	Wafer	Strong Yield (%)	Weak Yield (%)
70 µm	420-2	16	18
	420-3	36	43
	Total	26	31
50 µm	382-5	11	20
	382-6	30	36
	Total	22	29

Table 7.14: Preliminary total quality control yields, for 50 µm and 70 µm sensors.

There are large wafer-to-wafer yield variations for both sensor thicknesses, which are not only due to regular fluctuation in production losses. The yield for wafer 420-2 is artificially reduced by numerous contact errors, as mentioned above. The 50 µm wafers discussed in this thesis showed significant performance variation despite being tested with the same contact strategy. Closer inspection of wafer 382-5 revealed black spots on a significant amount of the wafer back-side, as shown in Figure 38a. The black spots where investigated using an Atomic Force Microscope (AFM) [44], and a Dektak profilometer [45] to see if they were caused by a production or handling error, and if they could be the cause for the low yield.



(a) Image of black spot damage through the Dektak miscroscope

(b) Profile of black spot damage taken by the AFM

Figure 38: Investigation of the black spots with a) a Dektak [45], and b) an AFM [44].

The AFM profiles of black spots appears to show a smoothening of the surface but DekTak measurements showed them to be raised in height from the wafer surface. The black spots lie on the back of the sensor and range in size, within the order of magnitude shown in Table 7.15, which shows the dimensions of the black spot shown in Figure 38a.

Vertical displacement from wafer surface	$\approx 0.18\,\mu m$
Length of the spot as selected in Figure 38a	$\approx 200\,\mu m$

Table 7.15: Dimensions of one exemplar black spot on wafer 382-5

The discrepancy between the AFM and DekTak description of the black spots lies in the physics of the AFM and suggests that the black spots consist of a different material to the sensor backside. The black spots are raised, but apply a weaker force on the AFM needle, leading to the needle being repulsed less by the black spots and the AFM interpreting this as a reduction in height. This suggests that the black spots consist of a material with a lower adhesion force than silicon. Further AFM measurements could be carried out to determine the adhesion force and the Young's modulus of the material for its identification.

The black spots could be residue from production which was left on the wafers and then burnt onto them during plasma etching. Identifying the material could help confirm this. This could be avoided if the sensors were better cleaned between processing steps to avoid residue on the sensors during plasma-etching. The residue is too thin to change the distribution of pressure to the back-side of the sensors during testing, but could be an indication of further damage to the sensors during plasma-etching, which could explain the low yield for wafer 382-5. While this requires further investigation, it highlighted that the quality control procedure could be extended to ease the identification of systematic production errors. This is further discussed in Section 8.3.

Chapter 8

Improvements to the QC strategy

This chapter describes improvements made to the quality control strategy, which aim to increase the quality control yield by reducing testing errors. The vertex detector pre-production quality control presented in Chapter 7 provided information on the performance of the quality control tests and on the behaviour of the sensors. This highlighted key issues with the testing scheme, such as frequent contact problems. The main aim of this chapter is the reduction of yield loss due these testing issues, and the implementation of a chip recovery strategy. The quality control strategy is also extended to make systematic production errors easier to identify. Proposals are made for increasing efficiency of the testing scheme for the production phase.

8.1 Optimising the Contact Strategy

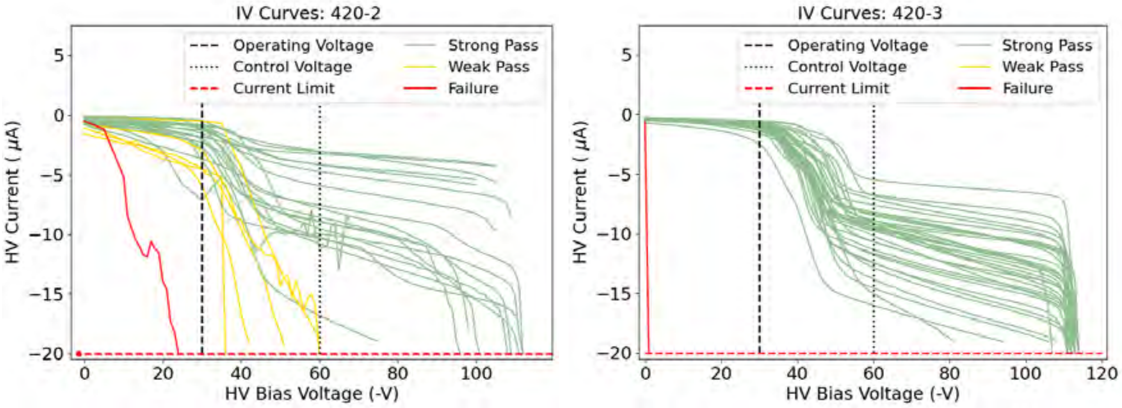
The electrical contact of the sensor to the testing setup is essential for the quality control tests. An insufficient contact could cause a functional sensor to fail the quality control, artificially reducing the yield.

For the vertex detector pre-production quality control the contact is made using a probe card, as discussed in Section 6.3. The contact can be improved through shifting of the sensor in the mount, or by adjusting the downwards pressure pressing the sensor onto the contact needles. During the vertex detector pre-production quality control, the contact strategy was changed from a fixed contact strategy to a flexible contact strategy. The fixed contact strategy consisted of the application of the same pressure to every sensor, using a marker on the probe card. The method did not guarantee uniformity for the pressures applied to the sensors, as the precision of the pressure applied was limited by the thickness of the marker.

For the flexible contact strategy, pressure is applied to each sensor until the needles and connector pads are in sufficient contact. This can be identified because both the LV and HV currents will increase when the contact is established. The HV current will typically increase to from an order of magnitude of 10^{-6} µA to currents in the order of

10^{-1} µA, while the LV current will increase from 0 mA to between 30 mA 200 mA. The LVDS links can show 8b/10b errors at the lowest contact pressure due to voltage drops caused by high resistances between sensor and needles. During testing, the pressure was increased slightly to recover this, but this may not always be necessary as the voltage optimisation can adjust the supplied voltage to compensate for these voltage drops. This flexible contact strategy intends to apply the minimum possible pressure to each sensor which guarantees a sufficient contact. The pressures applied to the individual sensors are expected to remain very similar, but this method has the clear advantage of a more individual contact establishment. The amount of pressure applied is adjusted to the behaviour of each individual sensor.

While there are natural wafer to wafer performance variations, the wafers tested with the flexible contact strategy show fewer characteristic contact issues than the wafer tested with the fixed contact strategy. Sensors with insufficient contact show a lot of fluctuations in their IV scan. The IV scans for the flexible contact strategy shows significantly fewer IV curves with high fluctuations, as shown in Figure 39. Also, more sensors reach the control voltage and final breakdown. The result of the quality control test is more reliable with the flexible contact strategy, as less sensors fail due to contact issues, artificially reducing the yield.



(a) Fixed contact strategy

(b) Flexible contact strategy

Figure 39: IV scans for two different 70 µm wafers, for the fixed and flexible contact strategies.

To further reduce contact issues, a pre-testing contact verification was developed using a sequencer script. The contact verification procedure can be used to verify the contact of a sensor after the flexible contact strategy was employed. It tests the power consumption of the sensor, and whether it can be configured successfully.

Towards the end of the vertex detector pre-production tests discussed in this thesis, the probe-card setup showed sporadic contact errors characteristic to the wearing down of the probe card needles. The repeated contact between needles and sensors can wear down the tips of the needles. The resistance at the contact point between sensors and needles is increased, leading to drops and instability in the supplied voltage. This limited the ability to test the contact script across an entire wafer, which is necessary before the contact script is universally added to the quality control procedure. Regular replacement of the probe card needles is a standard procedure, and is expected to solve the observed contact issues to allow for further testing of the contact script.

8.2 Chip Recovery

It is important to reduce the loss of sensors due to testing issues such as unstable contact. Sensors are therefore flagged for retesting if their quality control tests showed characteristic contact errors, or contradictory results.

Sensors which show high fluctuations in the IV scan should be flagged for re-testing, as this is a very characteristic effect of unstable contact. Sensors which fail the internal voltages test due to a failed VDDD or VDDA optimisation are flagged for retesting if the VDAC scan or LVDS links test are passed. The VDDD and VDDA tested during the internal voltages test regulate the DACS tested in the VDAC scan and the function of the LVDS links. This means that a sensor with issues with these internal voltages would not show a regular VDAC scan, and would not be able to transmit data without 8b/10b errors through the LVDS links. This contradictory output is characteristic of a contact error.

A failed LV power-on test can also be recovered, but this does not require flagging or retesting. A sensor which fails the LV power-on test may show good final voltages for VDDD and VDDA after the voltage optimisation performed in the internal voltages test. The successful voltage optimisation of the internal circuitry proves that it can be successfully powered, so the sensor failed the LV power-on test due to a high or low current after powering. This can be caused by too much or too little pressure affecting the resistance at the contact between needles and sensor. If the voltage optimisation can successfully recover the LV current to the desirable range, the sensor's on-chip circuitry shows functionality and the result for the LV power-on test should be changed to a weak pass.

Unfortunately the re-testing of flagged sensors for this thesis was limited by time constraints, and by the usage of flagged sensors for other tests. The success of this recovery scheme in improving the yield by reducing testing errors can be evaluated in future quality control tests.

8.3 Identifying Systematic Production Errors

For each sensor, the quality control result was mapped to its position on the wafer. This is intended to help identify systematic production errors which could cause more failures in a specific region, for example due to clamping, or inconsistencies in the plasma temperature during plasma-etching. An example for a damage location plot is shown in Figure 40.

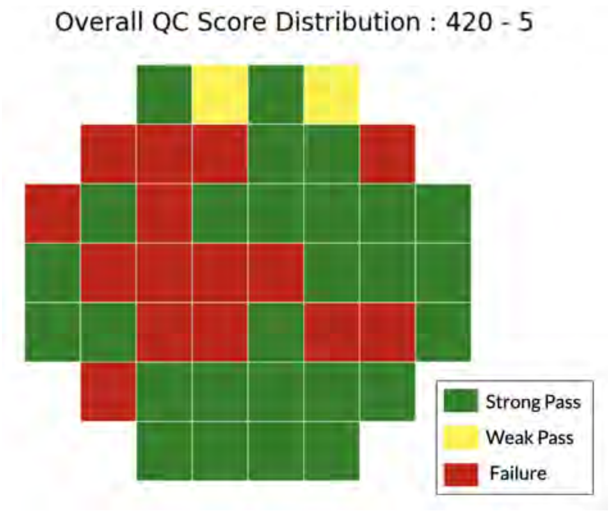


Figure 40: Damage location plot for wafer 420-5 of 70 µm sensors.

The more wafers are tested, the better systematic production errors can be identified. For the six wafers studied (two more are introduced in the following chapter), no significant dependency of failure modes on the chip position on the wafer has been observed. This is a valuable extension of the quality control procedure because it can help identify losses through systematic production errors if these occur.

8.4 The Safety Threshold

During the individual quality control tests (apart from the LVDS links test, for which the threshold is an independent variable), ThLow and ThHigh are set to a constant value, to reduce noise interference by providing a safety threshold.

This threshold was previously at ThHigh: 118, ThLow: 117, which corresponds to an effective threshold of 42 mV at the Baseline of 112. The results from the LVDS links analysis in Section 7.5 showed that the default threshold value of 118 was not high enough to remove noise effects.

The threshold was therefore raised to ThHigh: 138, ThLow: 137, equivalent to an effective threshold of 182 mV, for all tests. This threshold was chosen as the LVDS links test in Section 7.5 did not show significant noise effects at this threshold. Noise effects could affect the test outcomes as the processing of noise hits not only raises the LV current beyond normal operation levels, but also increases the heat dissipated, which can affect the functionality of other components.

8.5 Procedure Changes for Production testing

The quality control procedure should be optimised for final production testing. The principle aim of production testing is the fast evaluation of the sensors. The tests should therefore take reduced data, and focus only the essential information needed for evaluation. This is necessary because of the large number of sensors (2844 [46]) required for the Mu3e detector. Certain optimisations to the single chip tests are addressed in Chapter 9, but the general quality control strategy can also be optimised.

Gaining information on the sensors function and the efficiency of the testing procedure was an additional aim of pre-production quality control, so all tests were carried out regardless of the functionality of the sensor.

For the production testing, it makes sense to stop testing when it is clear that a sensor is not functional. The testing order should prioritise the most selective tests to accelerate the quality control. However, the testing order must also respect dependencies between tests and the fact that the selectivity of tests varies between the two different sensor thicknesses. The VDAC scan and LVDS links tests must come after the internal voltages test because they require an optimised supply voltage. The ideal order for the IV scan and the power-on test is different for the two sensor thicknesses due to the extreme selectivity of the IV scan for 50 µm. Due to the tests being more selective in general for the 50 µm sensors, and the changing of the running order coming at the risk of unexpected cross-test effects, the ideal running order for 50 µm was chosen, which corresponds to the one previously implemented.

Ending the quality control at the first failure is a sensible strategy for reducing the testing time, but efficiency concessions must be made to allow for the chip recovery discussed in Section 8.2. The running order, adapted to allow for chip recovery, is shown in Table 8.1.

Testing Order	Single Chip Test	Stop QC if Failed?
1	IV scan	✓
2	LV Power-On	×
3	Internal Voltages	×
4	VDAC scan	✓
5	LVDS links	✓

Table 8.1: Proposed testing strategy for the production quality control procedure.

Ending at first failure is not an issue for the recovery of sensors which showed unstable contact during the IV scan, as the contact issue is identified through analysis of the IV scan itself. However, the recovery of sensors which failed the internal voltages test or the LV power-on test relies on the results of later tests, as discussed in Section 8.2. The QC testing should therefore not be ended after a failure in these tests to allow continued identification of testing errors.

The artificial failures for the LV power-on and internal voltages tests are mostly due to contact issues, which should be significantly reduced through the contact validation script discussed in Section 8.1. However, the chip recovery strategy should nonetheless be maintained because it is an important step towards reducing yield loss due to errors during testing.

Chapter 9

Improvements to the Quality Control Tests

This chapter describes the improvements made to the individual quality control tests, and will present first results from this testing scheme. The analysis in Chapter 7 highlighted issues with the testing procedures and showed which areas of functionality should be explored in greater detail. The tests are improved to reduce yield loss due to false negative results and expand the investigation of failure modes. Small adjustments were made to reduce the duration of tests, although this is not a main goal at the pre-production stage. Results are shown for two wafers: 420-5, which consists of 70 µm sensors, and 382-9, which consists of 50 µm sensors. The changes to the testing procedures and parameters are made by editing the responsible sequencer scripts, while changes in the analysis and evaluation of the tests are implemented in the evaluation code.

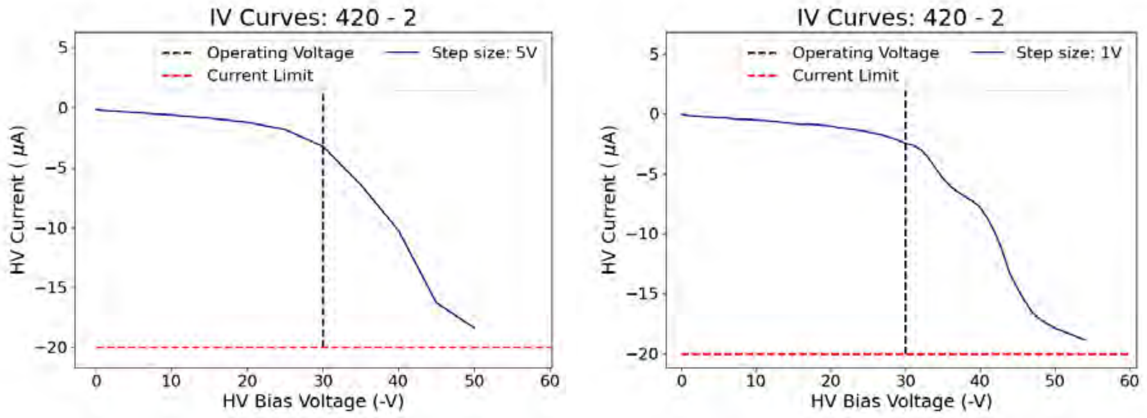
9.1 The IV Scan

The testing parameters for the IV scan were adjusted to better fit the aims of the test. The voltage range investigated by the IV scan was reduced from 0 V-120 V to 0 V-65 V. The test is ended just after the control voltage for 70 µm to reduce the duration of the test. The curve above this point is not required for the final evaluation. In addition, the repetition of measurements at a fine step-size was removed. The scan is taken once at an optimised step-size, which is identified by the step-size study described in Section 9.1.1. The IV scan for 50 µm could be further shortened to just above the 50 µm control voltage, but this was not done at this stage to allow for better comparison of the IV curves for the two sensor thicknesses.

9.1.1 The Step-Size Analysis

The k-value analysis is important for the identification of a suitable bias voltage for operation, as discussed in Section 7.1. The success of this analysis depends on the step-size of the IV scan.

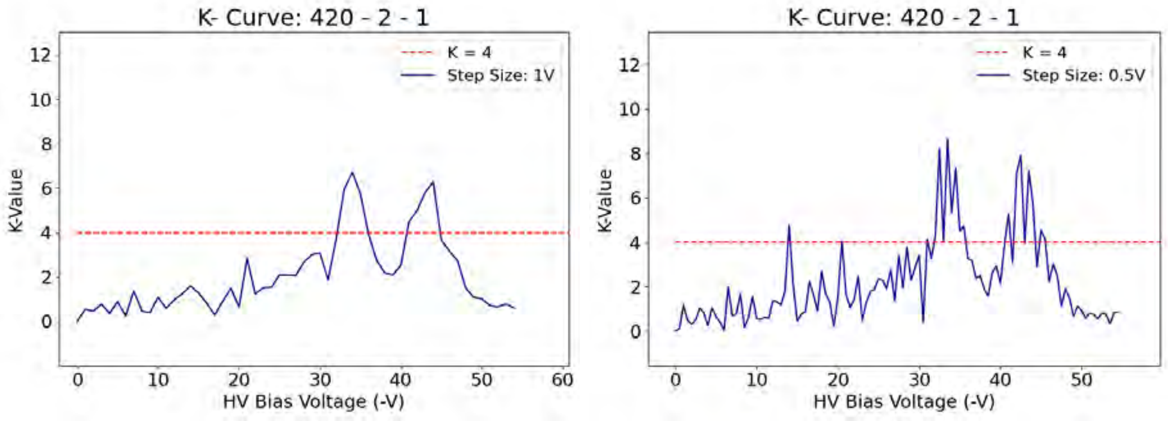
A step-size analysis was therefore carried out to investigate which step-size showed the best resolution for the IV scan. A large step-size will smooth out the curvature, leading to falsely diminished k-values, as shown in Figure 41, while a too small step-size leads to disproportionately large k-values for small deviations,as demonstrated in Figure 42. In either case the damage region cannot be located accurately.



(a) Step-size=5 V

(b) Step-size=1 V

Figure 41: Step-size study of the 420-2-1 70 µm sensor, demonstrating the loss of key curve features at large step-sizes.



(a) Step-size=1 V

(b) Step-size=0.5 V

Figure 42: Step-size study of the 420-2-1 70 µm sensor, demonstrating the loss of key curve features due to high k-value fluctuations at small step-sizes.

The ideal step-sizes were found to be 1 V for the 70 µm sensors, and 0.5 V for the 50 µm sensors, as the thinner sensors showed less variation in the IV curve, as is discussed in Section 9.1.3

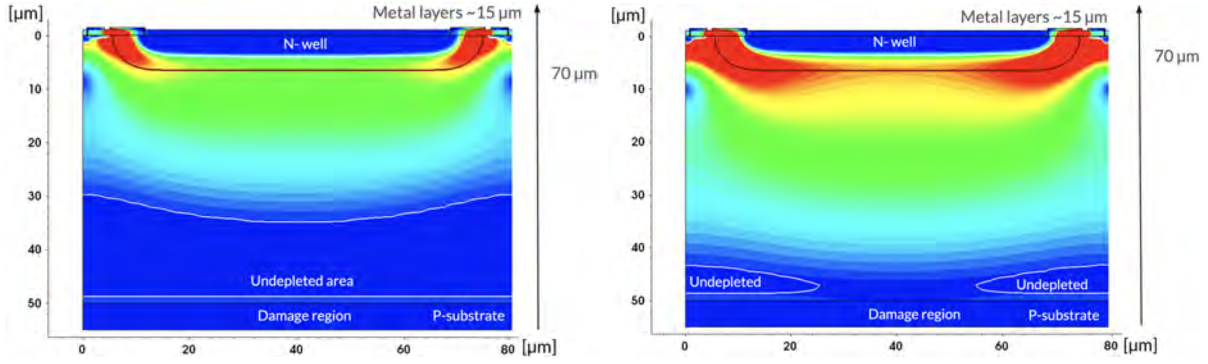
9.1.2 Summary of Parameter Changes

- Step-size (70 µm): 1 V
- Step-size (50 µm) : 0.5 V
- Bias voltage range: 0 V to −65 V

9.1.3 The Two-Step Current Increase

The step-size analysis enabled the generation of IV curves with a high resolution in the damage region, as is shown in Figure 41b. These show an unexpected feature: a second current increase in the damage region. This two-step increase can be explained through deeper analysis of the depletion process using Technology Computer Aided Design (TCAD) simulations [47].

Current simulations assume a damage region of $\sim 5\,\mu\text{m}$ at the back-side. In this region, additional levels were added in the band gap to simulate the effect of the defects created during the wafer thinning process. Figure 43 shows TCAD simulation results of the depletion depth at different HV bias voltages for a 70 µm MuPix11 sensor with a 355 Ωcm substrate. Figure 43a visualises the depletion zone at a voltage before the damage region is reached, and Figure 43b shows the depletion zone at a voltage at which the damage region has been reached.



(a) Bias voltage = −30 V

(b) Bias voltage = −60 V

Figure 43: TCAD simulation for a 70 µm sensor with a 355 Ωcm substrate and a 5 µm damage region at −30 V and −60 V, modified from [47].

The simulation shows that the depletion zone does not increase evenly, but follows the shape of the n-well. The damage region is first reached by the region under the pixel centre. At this point, there are undepleted areas to both sides of the pixel corner, as shown in Figure 43b. The depletion of these areas at larger voltages causes the second current increase due to increased conductivity paths between the thermally generated charges in the back-side and the pixel electrodes [47]. The 50 µm sensors have a less pronounced second step because the damage region is reached at lower bias voltages. Due to the square root dependency of depletion depth on the bias voltage, at lower bias voltages the increase in depletion for a given voltage increase is larger. Therefore the delay between two current increases is shorter. Furthermore, the lower depletion voltage for the 50 µm sensors generates a lower E-field, which leads to lower leakage currents, even when the damage region is reached. These two effects lead to the smaller, closer bump structure for 50 µm sensors.

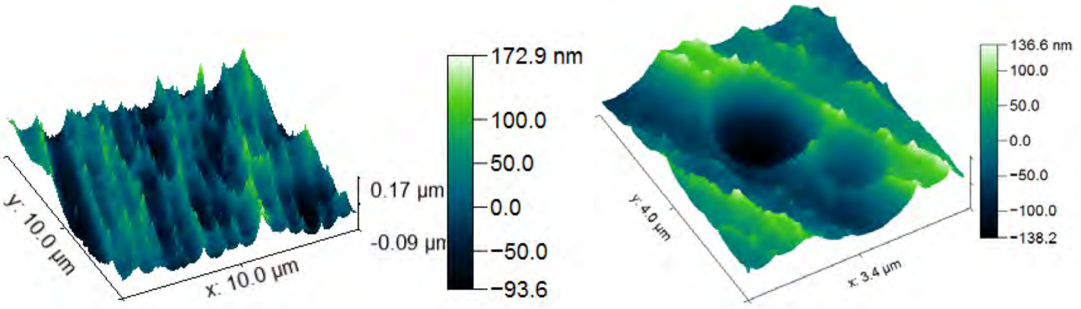
The simulation results enhanced the understanding of the MuPix11 depletion process and enabled improved quality control evaluation. Two k-peaks are registered inside the damage region so the k-value analysis must consider stabilisation to occur after the fourth k-voltage, not the second. Otherwise the control voltage would be set too early, before stabilisation, falsely awarding strong pass results to weak sensors.

The depletion simulation explains the formation of the two-step current increase, but predicts the damage region to be reached at higher bias voltages than observed. According to Figure 43b, the second current increase should happen after 60 V, but it occurs earlier in the measured IV scans.

The substrate resistivity used in the depletion simulation influences the size of the depletion region at a given bias voltage as described in Section 4.1. The resistivity can vary from sensor to sensor, but was previously measured to $\approx 369\,\Omega$cm [32]. The higher the resistivity the greater the depletion region for a given bias voltage. If the resistivity of the sensors is not considerably higher than the assumed $355\,\Omega$cm, the sub-surface cracks caused by grinding may extend deeper into the sensor than assumed in the simulation, which would explain the earlier current increase in the IV scan. While the 70 µm sensors have a thicker silicon layer, the substrate with sub-surface cracks is reached early into the depletion process for 50 µm sensors, causing high leakage currents at low HV bias voltages. A resistivity measurement of the sensors is necessary to confirm this.

9.1.4 Investigation into Post-Processing damage

A good description of the dimensions of the damage region can improve the accuracy of simulations, to aid interpretation of the results seen in the quality control tests. The wafers are thinned after production. First they are thinned through grinding, which causes sub-surface cracks and sensor warping [36][37], and then plasma etched to minimise the sub-surface cracks at deeper levels, and etch away those at the surface. The plasma etching only damages the wafer surface, so the damage to deep-lying circuitry should be minimised by this strategy. The surface scans shown in Figure 44 were taken with an Atomic Force Microscope (AFM) [44].



(a) Characteristic surface damage from plasma-etching

(b) Large etching pits at the edge of the Plasma-etching process

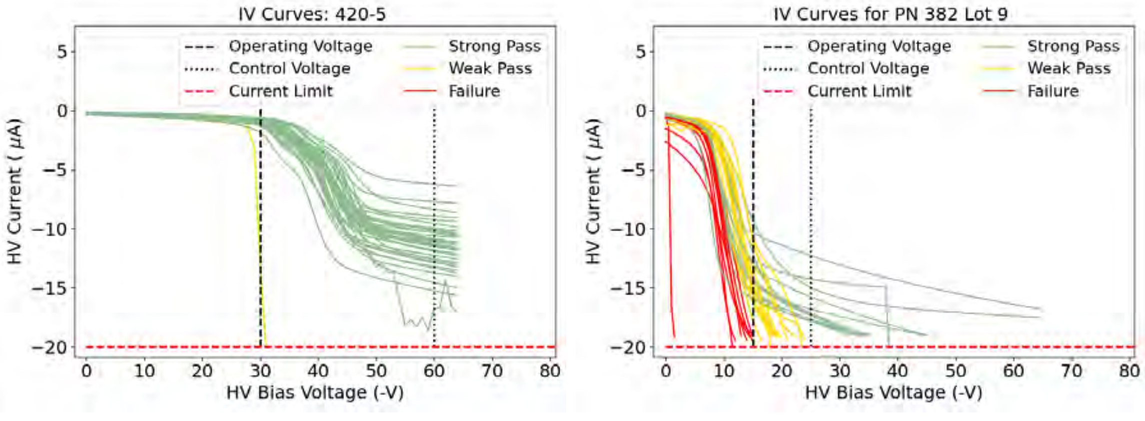
Figure 44: Scans of characteristic surface damage due to plasma-etching.

The observed samples were spare silicon shards from the edge of the respective wafers. However, as the shards were directly adjacent the sensors on the wafer, and the damage structures are characteristic to the plasma-etching process [38], it can be assumed that the same damage structures are also present on the sensors themselves. The peak-and-valley damage structure shown in Figure 44a is characteristic to the Gaussian distribution of particles in the plasma, and covers the entire back-side of the wafers. The individual deep etching pits in the back-side of the wafer shown in Figure 44b were up to approximately 100 nm deeper than the regular damage region, and are expected to be larger at the edges of the wafer.

The contribution of plasma-etching to the energy states in the band gap in the damage region is not fully understood. All electrons thermally emitted during plasma-etching are reabsorbed, but the high temperatures could lead to new dopants at the surface of the silicon. The surface damage from plasma etching shown in Figure 44 is more shallow than the one assumed for the sub-surface cracks in the simulations shown in Figure 43. If the damage region is deeper than simulated, as suggested by the measured IV scans, this would imply that the sub-surface cracks extend beyond the plasma-etched region, and are therefore not entirely removed by the plasma-etching process. The depth of the damage region causing the current increase observed in the IV scan therefore depends on the depth of sub-surface cracks from grinding. This depth can be determined through a study during plasma etching, as shown in [38], or by comparing simulations with different damage depths to the measured IV scan, for a sensor with known resistivity. This would help identify if the cause for the earlier current increase in the measured data is due to a higher resistivity, deeper damage region, or a different simulation variable.

9.1.5 Variations in the IV Yield

Figure 45 shows the IV scans performed after the improvement of the quality control tests. The evaluation result is indicated by the colour of the scan for each sensor.



(a) 70 µm

(b) 50 µm

Figure 45: The improved IV scans for 50 µm and 70 µm sensors.

Figure 45 shows that the IV criteria is successful in identifying sensors with functional outputs, and those with behaviours that are not suited for the Mu3e detector.

Figure 45b clearly shows the large current increase of the 50 µm sensors in comparison to the 70 µm sensors in Figure 45a. It is clear that the low pass rate is due to the behaviour of the sensors, not an error in the test. The evaluation successfully graded the sensors based on their performance. The sensors did not show the desired IV characteristics with increasing HV bias voltage. The current increases steeply in the damage region, and only two of forty-four sensors reach the end of the test at 65 V. Few sensors will be able to operate at full depletion, which is reached at approximately 15 V, and those that can will be consuming a current at −10 µA or more. In comparison, the 70 µm sensors almost all reach 65 V, and the operational sensors all show current of less than −5 µA at the operating voltage.

9.1.6 Light Dependency Study

The 50 µm wafer without back-side residue previously presented in Section 7.1 showed a better IV yield than wafer 382-9, shown in Figure 45b. The clear difference in the IV behaviour suggests influence of external effects in addition to the regular wafer-to-wafer yield fluctuation.

The improved tests were carried out in different lighting to the tests carried out before. The reduction of natural light due to a change in seasons meant that the ceiling light in the testing space was turned on, leading to light shining directly onto the probe card from above. The probe card has a single small open point in the lid of the mount, of about 2 mm diameter, through which light can directly hit the exposed silicon on the back-side of the sensor.

Figure 46 shows the IV scan for sensor 382-9-4, 50 µm, once with and once without exposure to light. The hole on the probe card was covered for the latter.

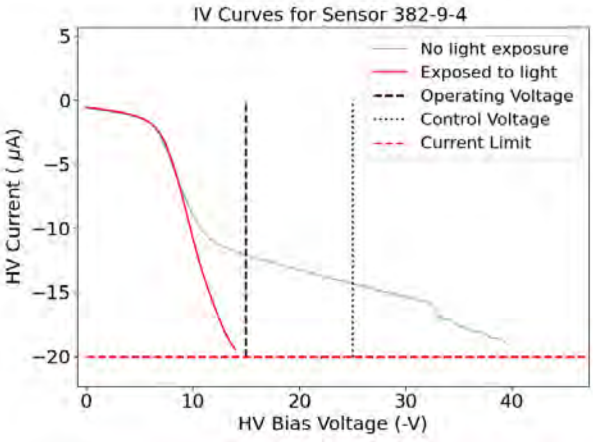


Figure 46: IV scans performed with and without light incidence on the same 50 µm sensor.

Figure 46 clearly demonstrates that the IV scan shows a much larger leakage current increase when light is incident, but only after the damage region is entered. The leakage current is so rapidly increased in the damage region that the current limit is reached, and the test ended before the current can stabilise. A high light dependency is inherent to the design of the 50 µm MuPix11 sensor. Incident photons can cause the ionisation of lattice atoms via the internal photoelectric effect [48]. If the released electrons are in the depletion region, or diffuse into it, the carriers will contribute to the leakage current. This effect is the working principle of silicon p-n photodiodes.

Therefore, despite the low sample size of this investigation of light dependency due to time constraints, it can be concluded that this effect is very likely to be the main reason for the low IV scan yield for 50 µm sensors. The light dependency causes the leakage current to increase rapidly in the damage region because the sensors reach full depletion in the damage region. At full depletion, all electrons generated by the internal photoelectric effect, which are not reabsorbed, contribute to the leakage current.

Future tests should always be carried out shielded from light, to understand the leakage current as it will be in the experiment, not artificially raised by light effects. The identification of this external influence on the testing process is a success, because it will improve the reliability and consistency of future quality control tests.

9.2 The Power-On Test

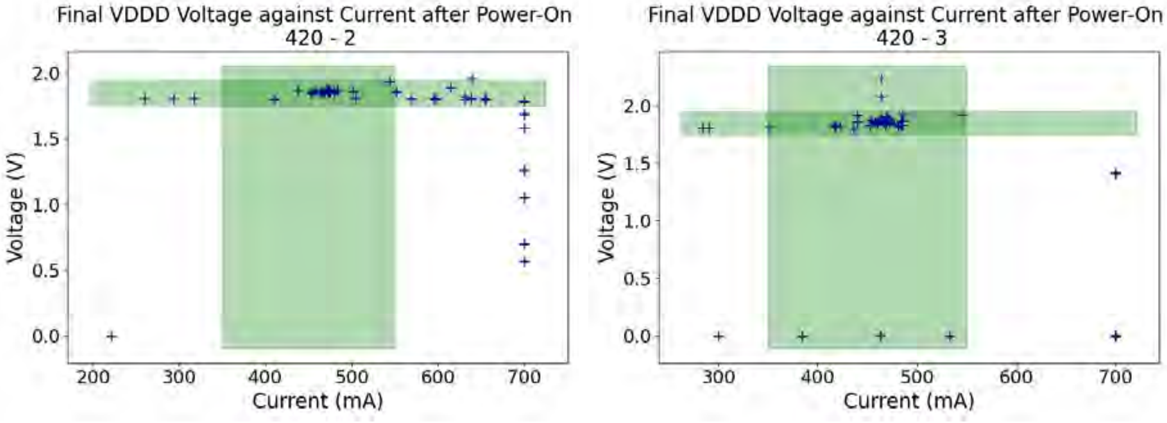
The power-on test was expanded to investigate which circuitry components were unable to be powered. The evaluation concept remains the same, but the investigation of failure modes was extended.

9.2.1 Current Limit Analysis

The power-on test is one of the most selective. It was investigated if the current limits defined in the LV power-on criteria exclude functional sensors.

Figure 47 shows the final voltage after voltage optimisation in the internal voltages test against the current after the power-on. It shows how the LV power-on test excludes sensors with a current slightly above or below the expected range, and that the on-chip circuitry for many of theses sensors is functional as they can set their internal voltages correctly.

The green bars show the regions in which strong pass criteria are fulfilled for the respective tests.



(a) Wafer 420-2: fixed contact strategy (b) Wafer 420-3: flexible contact strategy

Figure 47: Correlations of final VDDD voltages after voltage optimisation, against the default currents after power-on for a) wafer 420-2 and b) wafer 420-3

Sensors with high power-on currents and with functional voltage optimisation were only observed for wafer 420-2, which was tested using the fixed contact strategy Figure 47a. Too much pressure on the sensor can lead to low resistances between the sensor and the needles. This can lead to functional sensors drawing a large amount of current and wrongly failing the LV power-on test. The new contact strategies described in Section 8.1 should minimise the currents affected by bad contact, and therefore reduce yield loss due to contact issues in the LV power-on test. Remaining contact issues will be identified using the chip recovery scheme discussed in Section 8.2.

Low LV currents for on-chip circuitry which shows functionality during the internal voltages test are observed for both wafers. This could be caused by resistances between the voltage supply and the sensor's internal power grid, for example due to insufficient pressure on the sensors causing heightened resistances in the chip-needle contact. The voltage optimisation carried out in the internal voltages test compensates for such irregularities in resistance by raising the supply voltage. These resistance- induced failures can be separated from rightful failures caused by low current consumption, because if the failure was due to resistance, the internal voltages test will also recover the current consumption to within the limits set by the LV power-on test. The failure of these sensors despite their functionality is a limitation for the accuracy of the LV power-on test. Their recovery was discussed in Section 8.2.

Changing the current limits for the LV power-on criteria is not necessary as they evaluate the measured data accurately, and contact errors or failures due to an unoptimised supply voltage will be recovered by the chip recovery scheme. Furthermore, the limits defined in Section 7.2 ensure that the sensors receive the minimum current for operation, and if their LV current is low enough to conserve the uniformity of power consumption in the detector. Both of these conditions are important for sensor functionality and the limits will therefore remain unchanged for subsequent testing.

9.2.2 A Five-Step Power-On Test

The LV power-on test is designed to test the ability of the sensors to power their on-chip circuitry via the biasblocks. The test previously gave little information on the exact causes of failure. The procedure was therefore expanded to allow localisation of power-on failures to the responsible on-chip circuitry. The new power-on test switches on the circuitry components one after the other, whereas before they were all powered simultaneously. First, the sensor is configured with all on-chip circuitry turned off. The components are powered in the order given in Table 9.1, and the current measured at each step.

Step	Component	Location	Relevant DACs
1	Amplifier	Pixel	VNPix, VNFollPix, VSSA!(VDAC)
2	Line Driver	Pixel	VNOutPix
3	Comparator	Periphery	VNComp
4	Digital Circuits Clocking	Periphery	VN- and VPDCL
5	Digital Circuits Data Link	Periphery	VNLVDS, VNLVDSDel

Table 9.1: Order of On-Chip Circuitry Powering for the new Power-On Test

The successful turn on of each circuitry component leads to an increase in the LV current. When this is not the case, the component cannot be turned on. Figure 48 shows the mean LV current of all sensors in wafer 420-5, which passed the LV power-on test, at each step of the new LV power-on procedure. The power-up describes the initial LV current, before configuration of the sensor, and is different to the power-on, which describes the powering of all the circuitry components listed in Table 9.1. The LV current after the power up, and the LV current for all circuitry turned off are listed in order of greatest current to demonstrate the effect on the LV current for each component. The standard deviations of the LV currents show that the was a high variation in the measured currents after the powering of the amplifier and line driver.

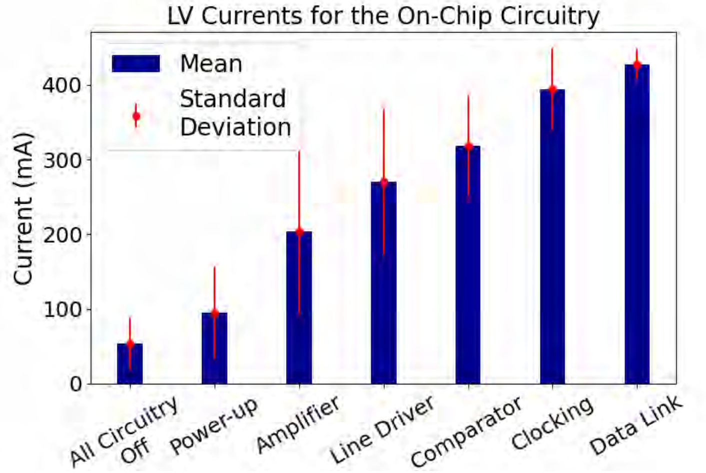


Figure 48: Mean LV current at each step of the new power-on procedure for functional sensors from wafer 420-5 (70 µm).

The failures of the individual circuitry components were investigated to find common failure modes for the LV power-on test. The average currents for the individual components shown in Figure 48 are listed in Table 9.2.

		70 µm			50 µm		
Step	Component	LV Current $\mu \pm \sigma$ (mA)	Lower Limit	# of Failures	LV Current $\mu \pm \sigma$ (mA)	Lower Limit	# of Failures
1	Amplifier	203.5 ± 110	80	7	202.1 ± 127.4	80	9
2	Line Driver	270.1 ± 98.2	100	6	269.7 ± 128.3	100	9
3	Comparator	318.3 ± 67.7	115	5	318.7 ± 106.6	115	9
4	Clocking	394.8 ± 53.4	235	5	408.9 ± 49.5	235	9
5	Data Link	427.5 ± 20.2	350	8	439.5 ± 26.2	350	10
Total Sensors:				44			44

Table 9.2: Average current jumps of circuitry components on functional sensors, the proposed lower limit, and the failure rate for 70 µm and 50 µm sensors.

Functional components were defined as those which showed a LV current above the lower limit. This was empirically set to fit the distribution of currents for sensors which showed a current increase for the components. The lower limit for Data Link was set by the minimum LV current all components, 350 mA. The LV current should also not surpass the upper limit of 550 mA. Components that did not show a suitable LV current according to this criteria were marked as failed.

The numbers of failures presented in Table 9.2 are not an accurate representation of the sensor behaviour, and no conclusions can be drawn from them. In addition to the failures for sensors which failed the LV power-on test, shown in Table 9.1, numerous sensors which passed also showed these individual component ”failures”. The amplifier and line driver are flagged as failed the most frequently and show very high standard deviations in Figure 48. This shows that the components are not sufficiently powered in the test, and therefore the LV current does not always increase.

A possible reason for this is that the optimisation of the internal voltages is necessary for the correct power supply to reach the circuitry components, and this optimisation is only carried out after the LV power-on test. As previously discussed, Figure 27 in Section 9.2 showed that some sensors showed low LV currents in the LV power-on test, but suitable LV currents after voltage optimisation. The evaluation performed by the LV power-on test is therefore limited by the unoptimised voltage supply, which artificially raises the LV power-on test’s selectivity. The test evaluates the measured data correctly, but the measured data is affected by resistances between voltage supply and the sensor’s internal power grid. and the chip recovery strategy described in Section 8.2 is necessary to reduce consequent yield loss. The accuracy of the LV power- on evaluation could also be improved by raising the initial voltage before optimisation to manually compensate for these voltage drops. The identification of this limitation is an important step towards a more accurate evaluation in future quality control tests.

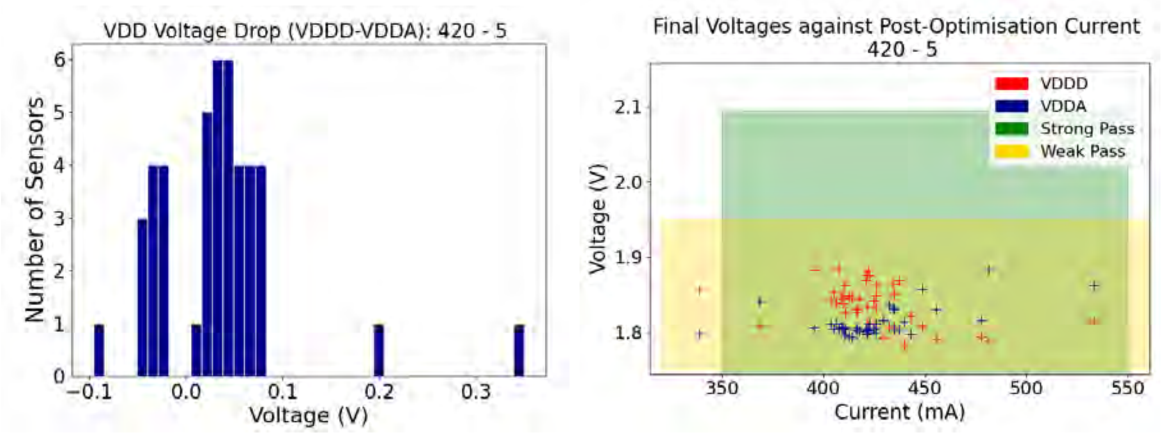
In future tests the LV power-on could be performed after a voltage optimisation to enable faster analysis of individual component failures. However, it is not strictly necessary, as time optimisation is not required at this stage, and all the individual components are investigated in later tests, and so the component failures which led to the failure of the LV power-on can be identified by cross-referencing the test results. The function of the Data Link, Clocking and Comparator is verified in the LVDS links test, and the Amplifier, Line Driver and Comparator are investigated in the VDAC scan.

9.3 The Internal Voltages Test

The criteria for the internal voltages test showed accurate evaluation of the voltage optimisation. The target voltages were reached well by functional sensors and the pass limits were well set, as they allowed for small fluctuations (-0.05,+0.15) in the final voltages, but excluded sensors which could not reach them. There was no extension of the internal voltages test but the failure modes were investigated in more detail, and testing parameters were changed to prevent possible testing errors.
The parameter for wait time between a change in the supply voltage, and the measurement of the effective voltage arriving on the sensor is referred to as the ADC wait time. This was increased from 1 s to 2 s, to make sure the sensor has enough time to settle in its new state before the effective voltage is measured.
As mentioned in Section 7.3, the target voltage for VSSA was changed to 1.1 V during the course of the previous tests. This value is kept as the target voltage for both sensor types for future tests because it ensures that the voltage optimisation is tested for a voltage comfortably above the minimum needed to bring the amplifier into its operational range.

9.4 Investigation of Voltage Drops

The evaluation for the internal voltages test was expanded to investigate the behaviour of VDDD and VDDA voltages. The difference between the final VDDD and VDDA voltages are shown in Figure 49.



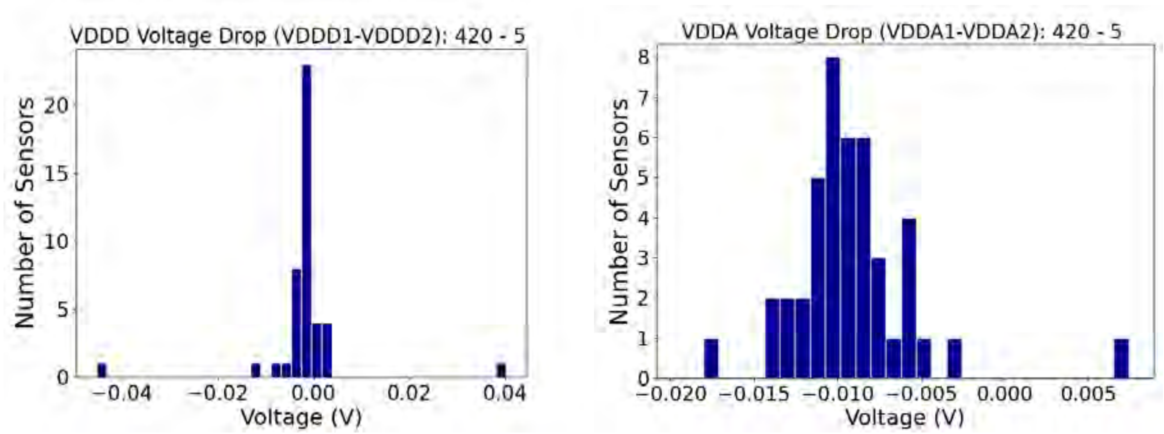
(a) Distribution of voltage differences.

(b) Scatter plot of final voltages against the post-optimisation current.

Figure 49: Visualisation of the voltage difference between VDDD and VDDA, in the form of a) a distribution, and b) a scatter plot of the voltages, for 70 µm sensors.

Most functional sensors showed a higher VDDD than VDDA voltage after optimisation, with a voltage drop between 0.0 V and 0.1 V. This was also observed for 50 μm sensors, and is due to VDDA voltage drops in the power grid. Figure 49b shows that almost all 70 µm sensors with greater VDDA than VDDD have LV currents above approximately 450 mA. This could show that the digital circuits show greater voltage drops at higher currents. This was not observed for the 50 µm sensors, which showed VDDD to be higher than VDDA in all cases.

Figure 50 shows the voltage differences between the two sensor partitions, for VDDA and VDDD. This allows the comparison of the voltage drops on the two sensor partitions.



(a) VDDD final voltages

(b) VDDA final voltages

Figure 50: Final VDDD and VDDA voltages for both sensor partitions, for 70 µm sensors

VSSA shows a very similar voltage offset between partitions as VDDA. Partition 1 consistently shows a lower final voltage than partition 2, although the difference is smaller for VDDD than for VDDA and VSSA. The mean voltage differences between partitions are −6.4 mV for VSSA, −9.7 mV for VDDA and −0.8 mV for VDDD, for 70 µm sensors. This shows that partition 1 sees more voltage drops than partition 2, and that this difference is larger for the analogue circuitry.

The voltage differences across the sensor partitions are small in comparison to the target voltages, and are not a common reason for failure.

9.5 Investigation of Failure Modes

The evaluation for the internal voltages test was expanded to investigate the cause of failures. Table 9.3 shows the percentage of failed voltage optimisations for each internal voltages, for the sensors tested with the improved VDAC scan.

A failed optimisation is clear evidence for issues with sensor operation, such as very high resistances on the internal power grid. It is important to investigate if the power grid shows high resistances frequently for a certain sensor partition, or internal voltage.

	Failures (%)	
VDAC	70 µm	50 µm
VSS1	11.4	18.2
VSS2	11.4	16.0
VDDD1	9.1	18.2
VDDD2	9.1	18.2
VDDA1	6.8	16.0
VDDA2	6.8	16.0

Table 9.3: Percentage of failed optimisations for each internal voltage for 50 µm and 70 µm.

The tested wafers show very little variation in failure frequency between the three internal voltages. The 50 µm sensors showed more failures than the 70 µm sensors, and there was one sensor which only failed for partition 2. However, most internal voltage failures show a failure for both partitions. The tested wafers do not show evidence of one partition systematically failing more than the other.

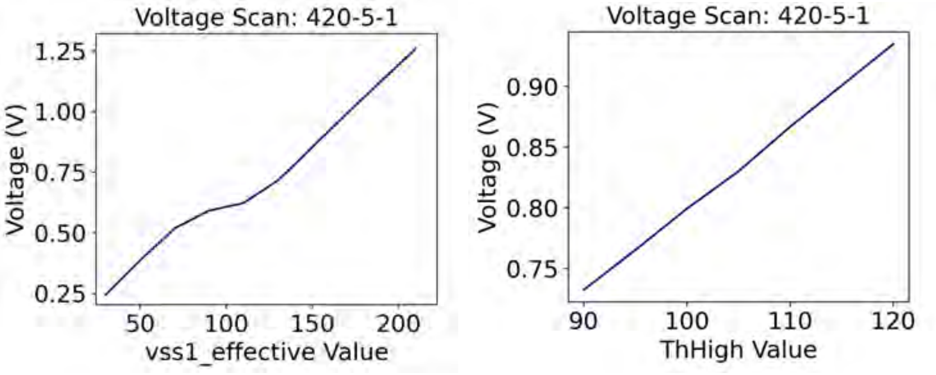
9.6 The VDAC scan

The previous VDAC scans discussed in Section 7.4 showed testing errors, which will be addressed in this chapter. Firstly, no data was taken for the ThLow VDAC, due to a faulty connection at the setup. This was fixed for the second round of tests, so that the VDAC scan now includes all VDAC variables intended for the final production quality control. In addition, small parameter changes were implemented. As mentioned in Section 9.3, the ADC wait time was increased from 1 to 2 seconds, to allow the sensor to settle in the new state after a settings change. This was done to ensure the measurement showed the effect of the voltage setting. The testing range also amended for BLPix and Ref_VSS (featured in VSS1 and VSS2), as the scan started midway through amplifier activation for previous tests. The new BLPix scan includes DAC values from 60 to 160, while the new Ref_VSS scan tests from 40 to 210.

The most important change made was the change from simultaneous VDAC testing to sequential tests. The analysis of the previous VDAC scans showed a very uncharacteristic output such as a decrease in current after amplifier activation, and an activation current jump in for every VDAC measurement (which should be limited to the VSS VDACs). The superposing effects of all the VDAC changes did not allow for effective analysis of the individual behaviours of the DACs. The VDAC scans were made sequential using a parameter in the VDAC sequencer script in order to observe the effect of each individual VDAC on the sensors.

9.6.1 The Sequential Voltage Scan

The sequential voltage scan shows that VSS1, VSS2 and BLPix do not cause a linear voltage increase. This was suggested by the results in Section 7.4, as the voltage scans for these DACs showed low gradients and a high deviations from linearity. Two exemplar voltage scans are shown in Figure 51.



(a) VSS1

(b) ThHigh

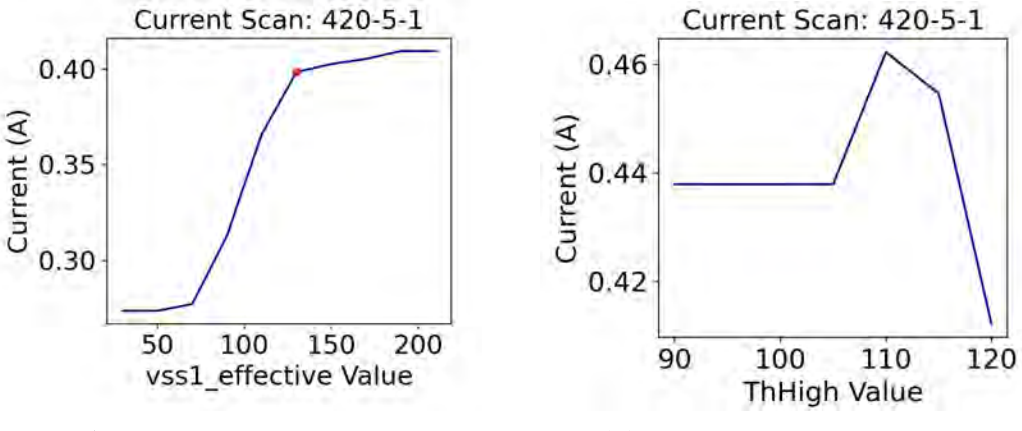
Figure 51: Sequential voltage scans for VSS1 and ThHigh for an exemplar 70 µm sensor

The voltage scans are shown for VSS1 and ThHigh. VSS1 can be considered representative of the voltage scans for VSS2 and BLPix, while ThHigh shows very similar behaviour to ThLow and Baseline. The voltage scan for VSS1 shows a linear increase for low and high ref_VSS values, and a region of non-linearity at a DAC value of ~ 100. This effect is well understood, since these DACs have a direct impact on the LV current. The activation of the amplifier (or line driver for BLPix) leads to an increase in the LV current, as discussed in Section 7.4. As the current increases, the voltage drop between input and internal voltage increases in response. This leads to a lower effective voltage, and therefore lower voltage scan linearity constant.

The voltage scans for ThHigh, ThLow and Baseline show the expected linear voltage relationship. It must be noted that Figure 51 shows a linear increase in the applied voltage, but that the voltage scan is in fact a step-function because the DAC values are discrete, not continuous.

9.6.2 The Sequential Current scan

The sequential current scan shows the S-curve characteristic of the amplifier activation for the VSS1 and VSS2 scans, as shown in Figure 52a. The current stabilises after amplification and there is no current drop as had been observed in the previous tests. This shows that the simultaneous testing was the cause for the uncharacteristic features in the previous current scans.



(a) Current scan for VSS1

(b) Current scan for ThHigh

Figure 52: Current scan for sequential testing for VSS1 and ThHigh, for an exemplar 70 µm sensor.

The current scan for ThHigh, ThLow and Baseline showed a constant behaviour, as expected, but only for low DAC values, as shown in 52b. The small increase in current is observed when the threshold reaches the baseline. This means that noise effects are now present, and the threshold is too low to remove them. The processing of the noise hits requires a high power consumption. The LV current then drops as the threshold is raised further, above the noise level.

Future tests will be adapted so that the baseline is lower than the thresholds throughout the VDAC scans, so that the current scans for ThHigh, ThLow and Baseline are not corrupted by noise. The range of the ThHigh and ThLow values could also be adapted to include higher threshold values, as it has been observed that the low thresholds are not sufficient to exclude noise. The behaviour of the sensor at high thresholds is therefore relevant for operation.

The red circle on the currents scan marks the point of component activation as it is identified by the analysis code. In the case of VSS1 and VSS2 this is the amplifier activation, and for BLPix it marks the line driver activation. There is no analysis of activation for ThHigh, ThLow and Baseline, as these VDACs do not correspond to components with activation. The current scan for BLPix is shown in Figure 53.

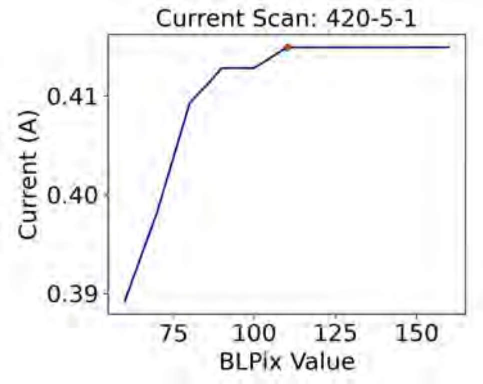


Figure 53: Current scan for sequential testing: BLPix, for 70 µm Sensor

The current scan for BLPix shows a clear current increase similar to the amplifier activation for VSS1/VSS2. As discussed in Chapter 5, BLPix controls the baseline voltage of the analogue circuitry. At low BLPix values, the voltage supply to the line driver circuitry is not within the line driver's operational range. It requires a minimum input voltage to reach a stable state in which the signal from the pixel can be driven down the long analogue signal lines of the pixel matrix, and in which the line driver will draw more current. The current increase seen for BLPix is due to the line driver reaching its operational range.

9.6.3 Evaluation using the Current Scan

The VDAC criteria must be changed to fit the new expectations for the VDAC scan. The criteria and grading parameters are summarised in Table 9.4, Table 9.6 and Table 9.5.

The linearity of the voltage scan is no longer a good evaluation parameter for VSS1, VSS2 and BLPix VDACs as the scan is not expected to be linear. These VDACs can be evaluated using the success of the amplifier activation, according to the parameters in Table 9.5. A successful activation is identified through a current increase between the

first and last measured values of the current scan, the minimum value for the criteria is set empirically through observation of functional sensors. The limits for the final current after activation correspond to those for the LV power on test: they ensure the chip is operating at the expected LV current after the activation.
The deviation is defined as the standard deviation of residuals about the least squares regression line, also known as the root mean square (RMS) deviation. The deviation is defined as the standard deviation of residuals about the least squares regression line, also known as the root mean square (RMS) deviation.

Result	Criteria
Strong Pass	ThLow, ThHigh and Baseline: 1. The voltage linearity deviation is less than the limit in Table 9.6. VSS1, VSS2 and BLPix: 2. The current after activation is within the limits in Table 9.5
Weak Pass	ThLow, ThHigh and Baseline: 1. The voltage scan linearity constant is within an error margin of ± 1.0 mV of the target gradient of 7.0 mV 2. The starting voltage exceeds the minimum at the DAC start value, both listed in Table 9.6. VSS1, VSS2 and BLPix: 3. The current scan shows a current increase above the minimum shown in Table 9.5.
Failure	1. The criteria for the weak pass are not fulfilled.

Table 9.4: Test criteria for the VDAC scan

VDAC	Minimum Current Increase (mA)	Minimum Final Current (mA)	Maximum Final Current (mA)
VSS1/VSS2	10	350	550
BLPix	10	350	550

Table 9.5: Evaluation parameters for the VDAC current scan

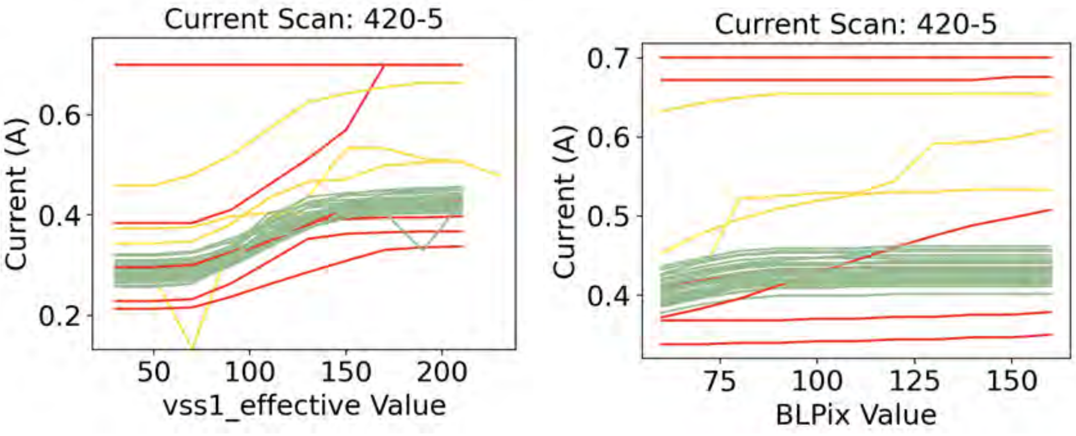
VDAC	Gradient Range (mV/DAC)	DAC Sample Value [dec]	Lower Voltage Limit (V)	Maximum Deviation (mV)
ThHigh, ThLow, Baseline	6 - 8	100	0.5	7

Table 9.6: Evaluation parameters for the VDAC voltage scan

The current scans for ThHigh, ThLow and Baseline have a constant relationship between VDAC value and LV current. This means that all VDACs can be evaluated using the

current scan in future tests. ThHigh, ThLow and Baseline can be evaluated using the linearity constant and deviation of the scans to make sure they show a constant current. However, the tests for ThHigh, ThLow and Baseline presented in this section only showed a constant relationship between current and the VDAC values at low DAC values. At higher DAC values, the noise level passed the threshold and the LV current increased. To prevent this from happening in future tests, the testing parameters must be changed so that the Baseline is always sufficiently below the ThHigh and ThLow thresholds.
For the present tests, the old criteria, based on the voltage scan, will be used for ThHigh, ThLow and Baseline, and the new current-based criteria will be used for VSS1, VSS2 and BLPix. The allowed gradient range has been reduced from the values presented in Section 7.4, because the generous allowance of ± 2 mV was introduced to accommodate for the high gradient variation of VSS1 and VSS2 DACs and is unnecessary for ThLow, ThHigh and Baseline, which were shown to adhere to linearity with less deviation. Therefore an error margin of ± 1 mV is sufficient. VSS1,VSS2 and BLPix are evaluated according to the success of the amplifier activation.
Future quality control procedures will evaluate these DACs by their linearity in the current scan. This is also beneficial for the development of ladder quality control procedures, which will only be able to read out the LV current of the individual sensors and therefore require criteria based on the current scan.

The effectiveness of the evaluation of the sequential VDAC scans can be verified by plotting the current scans with each individual scan highlighted according to the overall result of the VDAC scan for the sensor. Figure 54 shows the current scans for VSS1 and BLPix for wafer 420-5, of 50 µm sensors.



(a) Current scan VSS1

(b) Current scan BLPix

Figure 54: Current scans with test results for a) VSS1 and b) BLPix for 70 µm sensors.

The scans show the importance of testing all VDACs: a sensor which passes one VDAC scan is not guaranteed to pass the others. This can lead to some sensors with desirable output in one VDAC scan being marked as failed in the scan, due to them failing another. This is not due to a failure of the evaluation scheme, but of the sensor itself. The scans clearly show the success of the evaluation scheme at identifying sensors which show the desired behaviour.

9.6.4 Linearity of the Voltage Scans

The linearity constants of the VDAC voltage scans were calculated for ThHigh, ThLow and Baseline and listed in Table 9.7. The table also contains the target and measured averages for the RMS deviation from the least squares regression line for the voltage scans.

VDAC	Gradient Target ($\frac{\text{mV}}{\text{DAC}}$)	Deviat. Limit (mV)	70 µm Gradient (mV/DAC)	70 µm Deviation (mV)	50 µm Gradient (mV/DAC)	50 µm Deviation (mV)
Baseline	7	7	6.82 ± 0.25	2.00 ± 4.51	6.76 ± 0.05	0.65 ± 0.42
ThHigh	7	7	6.74 ± 0.28	3.43 ± 7.52	6.69 ± 0.17	2.47 ± 6.51
ThLow	7	7	6.79 ± 0.37	3.20 ± 5.87	6.75 ± 0.06	1.20 ± 0.73

Table 9.7: Mean values for the gradients and RMS deviations for the VDAC Voltage Scan, for each DAC value, for functional 50 µm and 70 µm sensors.

The mean values of the linearity constants of functional sensors, are lower than the target value of 7 mV. The target value is within one standard deviation of the mean for 70 µm sensors. The 50 µm sensors have lower standard deviations for the mean. Both Baseline and ThLow have an average linearity constant that deviates more than three standard deviations from the target voltage for 50 µm sensors. This could be explained by a small voltage drop and should not affect their functionality.

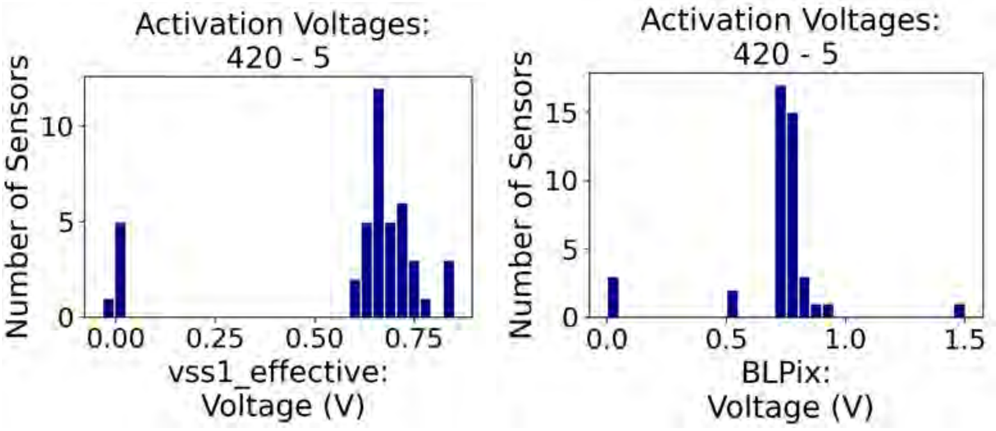
The mean deviations for the VDAC scan appear quite high in relation to the mean gradients, but this is due to the inherent resolution of the VDAC scan. The DAC values can only be increased in steps of one DAC, which leads to a voltage increase of 7 mV. This means that the DAC scan is a step-function, and therefore has an inherent deviation from linearity. If the RMS deviation is below 7 mV, this means that all DAC values can be set correctly. This is the case for all observed deviations. The standard deviations of the RMS deviations are quite large. This shows that individual functional sensors showed a one or more wrongly set DAC values.

ThHigh shows the highest standard deviation of the RMS deviation, for both 50 µm and 70 µmsensors, showing that it has the most wrongly set DAC values. However, the fact that the standard deviation is very close to 7 mV for ThHigh shows that even this VDAC does not show a large amount of wrongly set DAC values. Therefore, the voltage scans show a good linearity when analysed in the context of the inherent VDAC scan resolution.

9.6.5 Activation Voltages

When a component is reaches its operational range, the LV current will increase sharply. In the analysis of the current scan, the activation voltage is defined as the voltage at which the LV current stabilises after a component reaches its operational range. Figure 52 shows how the DAC value at activation is identified on the current scan. The voltage supplied at this DAC value is the activation voltage.

The distributions of activation voltages for VSS1 and BLPix for all 70 µm sensors (not just functional sensors) are shown in Figure 55. Table 9.8 shows the means and standard deviations of the activation voltages for the amplifier and line driver. These are derived from sensors which passed the VDAC scan, in order to describe the activation process in functional sensors.



(a) VSS1 (b) BLPix

Figure 55: Distributions of the activation voltages for a) VSS1 and b) BLPix for 70 µm sensors

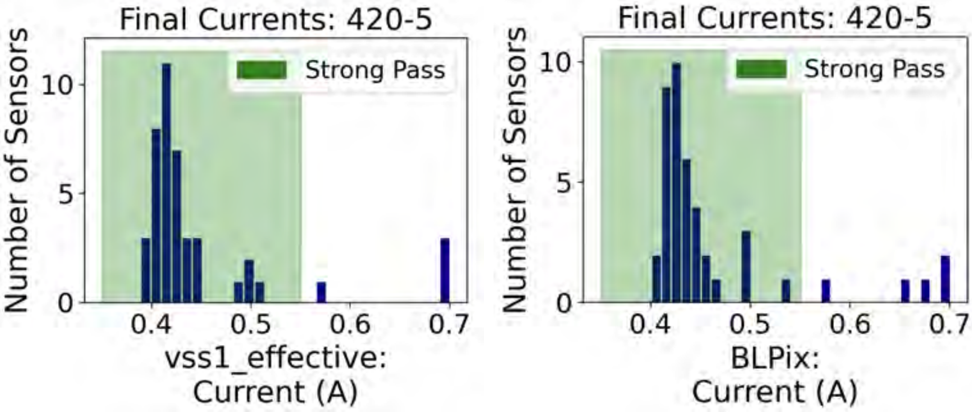
		Activation Voltage $\mu \pm \sigma$ (V)	
VDAC	Component	70 µm	50 µm
VSS1	Amplifier (Partition 1)	0.69 ± 0.06	0.70 ± 0.05
VSS2	Amplifier (Partition 2)	0.70 ± 0.07	0.70 ± 0.05
Ref _VSS Average	Amplifier (All)	0.70 ± 0.09	0.69 ± 0.07
BLPix	Line Driver	0.79 ± 0.13	0.80 ± 0.13

Table 9.8: Activation voltages for the amplifier and line driver, for functional 50 µm and 70 µm sensors

There is no significant deviation between the activation voltages identified for VSS1 and VSS2. This shows that the amplifier activation consistently occurs at the same voltage for both sensor partitions. There is no significant deviation between sensors of 70 µm and

50 µm thickness. The line driver is activated at higher voltages than the amplifier.
There no sensors which passed the VDAC scan and show an amplifier activation at voltages higher than 0.8 mV, or line driver activation past 1.0 V. This means that the the target voltage of 1.1 V set for the VSSA internal voltages test was suitably high. The test successfully evaluated the voltage optimisation for operation with active amplifiers and line drivers for all functional sensors.

The distributions of post-activation currents for VSS1 and BLPix are shown in Figure 56. The limit of 550 mA is set by the requirement of uniformity for power consumption in the detector, and Figure 56 shows it to generously include the majority of tested sensors. This shows good functionality of the amplifier and line driver because they should not reach the LV current limit when operated alone.



(a) Final currents for VSS1

(b) Final currents for BLPix

Figure 56: Distributions of the final LV current after amplifier activation for a) VSS1 and b) BLPix for 70 µm sensors.

The lowering of the maximum LV current could be considered for subsequent tests. The individual components should not draw the maximum LV current for operation individually. However, this amendment is not strictly necessary, as the evaluation of the combined LV current of the on-chip circuitry components is not an aim of the VDAC scan, and already performed in the LV power-on test.

9.6.6 VDAC performance

The number of failures of the individual VDACs were investigated and listed in Table 9.9. The VDACs which show the most errors, and therefore limit the VDAC yield, are BLPix and ref_VSS (VSS1/VSS2). This is a clear example of the analogue pixel circuitry being more error-prone than the digital circuity in the periphery, which is expected as the analogue circuitry is tightly routed and therefore production errors as dust particles in the production space can lead to shorts very quickly.

		Number of Failures	
VDAC	Location	70 µm	50 µm
VSS1	Pixel	4	10
VSS2	Pixel	4	10
BLPix	Pixel	6	10
Baseline	Periphery	3	7
ThHigh	Periphery	2	7
ThLow	Periphery	2	7
Total sensors:		44	44

Table 9.9: Number of failures according to the new VDAC criteria, for each VDAC, for each 50 µm and 70 µm sensors.

The small sample size limits the conclusiveness of these statistics, but the functionality on-pixel circuitry does appear to limit the VDAC scan yield for both sensor thicknesses.

9.7 LVDS Links

The LVDS links test was adapted for efficiency, and to remove testing errors. Section 7.5 showed that the default thresholds of ThHigh=118 and ThLow=117 are too low to transmit data without errors. Therefore, only results the from the LVDS links test at the raised thresholds of ThHigh=138 and ThLow=137 are considered in the evaluation.

In future, the default threshold should be removed to reduce the time taken by the LVDS links test during production testing. The aim of the LVDS links test is to evaluate if data can be transmitted without 8b/10b errors, and not the investigation of the pixel noise level. Therefore, the default threshold is therefore not necessary for the evaluation performed by the test. The information that would be gained from the definition of a new default threshold would be minimal. The noise level can be analysed with much more efficiency through a separate, designated investigation.

9.7.1 Clock Re-Synchronisation

The previous evaluation scheme presented in Section 7.5 did not consider the possibility to recover the data read-out through re-synchronisation of the internal and external clocks using the reset of the PLL. The measurement of the LVDS errors after re-synchronisation was previously implemented in the testing procedure, but not considered in the evaluation. The analysis code was therefore extended to read and evaluate the LVDS errors after the reset of the PLL, which improved the LVDS yield. For example, this led to the recovery of two sensors of wafer 420-5.

The improved LVDS links evaluation failed every sensor which did not show error-free readout for all links at at least one VPVCO (VNVCO) setting. It passed every sensor which could successfully send data without 8b/10b errors. Therefore the improved LVDS links evaluation accurately tests of the ability of a sensor to send out error-free data.

9.7.2 Amendments for Production Testing

The LVDS links test should be shortened for more time efficient production testing. This can be done by changing the test procedure.

The number of sensors with errors in their read-out varies strongly between VPVCO (VNVCO) values. This was previously discussed in Section 7.5. Table 9.10 shows the number of passes at the VPVCO (VNVCO) values for all six tested wafers. Differences in the functionality of VNVCO values between two sensor thicknesses were observed in the previous tests, but not for the improved LVDS test. This could be due to a reduction of contact errors, which could have affected the LVDS error rate for the 70 µm sensors in the previous tests.

VPVCO (VNVCO) Value	Number (%) of Passes for 70 µm	Number (%) of Passes for 50 µm
12 (13)	78 (59%)	55 (45%)
17 (18)	90 (68%)	78 (63%)
22 (23)	96 (73%)	81 (66%)
27 (28)	95 (72%)	81 (66%)
32 (33)	79 (60%)	75 (61%)
37 (38)	21 (16%)	11 (9%)
Total Sensors:	132	123

Table 9.10: Number of sensors which showed error-free readout, for each VPVCO (VNVCO) value, across all tested wafers.

The efficiency of the test could be increased by scanning the VPVCO (VNVCO) values following the highest success probability, as shown in Table 9.11, instead of going from smallest to largest as was done previously. The test can then be ended after a sufficient number of VPVCOs (VNVCOs) pass. Even though only one pass is needed for the sensor to be functional, it would be beneficial to always test the three best performing VPVCO (VNVCO) values to ease ladder construction. Even though individual setting of VPVCO (VNVCO) values is possible in ladder operation, it is useful if each sensor has multiple working values to reduce the necessary individual sensor configuration. The order of the three best performing VPVCOs (VNVCOs) is irrelevant because they will all be tested. This new testing strategy can be implemented through changes to the relevant sequencer files for the LVDS links quality control procedure.

Step	VPVCO (VNVCO) value	End Test if Failed?
1	17 (18)	×
2	22 (23)	×
3	27 (28)	×
4	32 (33)	✓
5	12 (13)	✓
6	37 (38)	✓

Table 9.11: Performance of VPVCO (VNVCO) values across all tested wafers.

Section 9.7.2 shows the frequency of a VPVCO (VNVCO) value being the only one which allows error-free read-out for a sensor. Only about $\sim 1.6\%$ of the tested sensors only worked for one VPVCO (VNVCO). This is beneficial for the proposed testing strategy, because there is a low probability of having to test all VPVCOs (VNVCOs) before a functional one is found. The new testing scheme will therefore accelerate the testing for almost every sensor.

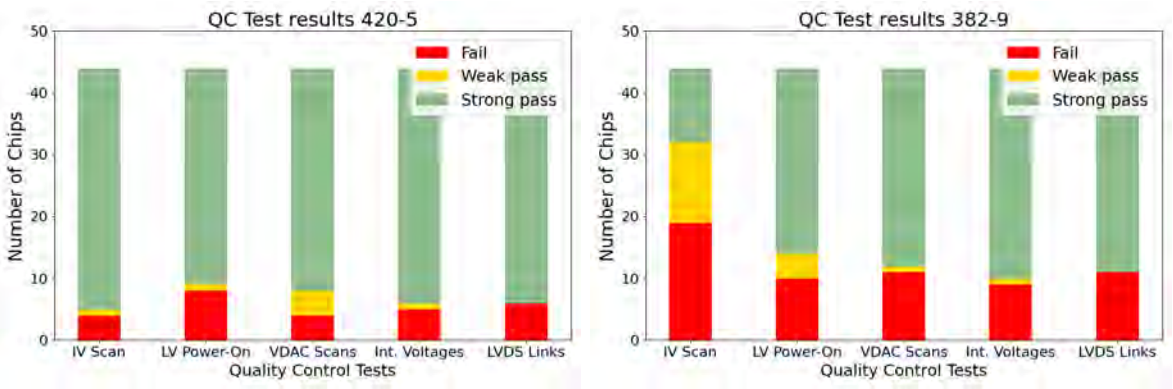
	# of ocurrences	
Single Passed VPVCO (VNVCO)	70 µm	50 µm
12 (13)	1	0
17 (18)	3	1
22 (23)	0	0
27 (28)	0	0
32 (33)	0	0
37 (38)	0	0
Total Sensors:	132	123

Table 9.12: Frequencies of sensors with only one VPVCO (VNVCO) with error-free readout, for all tested wafers.

The most important benefit of this testing strategy is that it will decrease the duration of the LVDS test without reducing the yield.

9.8 The Total Yield

The new testing scheme is able to improve the yield for the individual wafers by reducing errors in the testing and evaluation procedures. Large wafer-to-wafer fluctuations can occur, but the yield for a given wafer is clearly improved by the reduction of false negative results. The 50 µm wafer showed an artificially lowered yield due to the external influence of light, but errors during testing were reduced, and all tests but the IV scan showed improved yields. The total yields of the individual tests are visualised in Figure 57, and listed in Table 9.13.



(a) Yield for 70 µm sensors.

(b) Yield for 50 µm sensors.

Figure 57: Visualisation of the yields for the individual improved quality control tests, for 50 µm and 70 µm sensors.

Test	70 µm Yield (%)		50 µm Yield (%)	
	Strong	Weak	Strong	Weak
IV Scan	88.6	90.9	25.0	54.5
LV Power-On	79.5	81.8	70.5	77.3
Internal Voltages	86.4	88.6	77.3	79.5
VDAC Scan	79.5	81.8	72.7	75.0
LVDS Links	81.6	81.6	75.0	75.0

Table 9.13: Yields for each improved quality control test, for 50 µm and 70 µm sensors.

The yield for 70 µm sensors was limited by the VDAC scan and LV power-on test. Sequential testing improved the yield for the VDAC scan, which was a limiting factor for the previous quality control yield, see Section 7.6. The VDAC scan is still a limiting test for the 70 µm wafer, but this is now an accurate representation of sensor behaviour. The high selectivity of the VDAC scan is not an inherent issue of the test, but a consequence of the failure profile of the sensors. The malfunction of analogue circuitry components is the most common failure of the VDAC scan, and limits the quality control yield.

The LV power-on test has remained as a limiting factor. The inability to power the

on-chip circuitry is a common failure mode. The attempt to analyse the individual component failures was unsuccessful because the supply voltage is not optimised before the LV power-on test is carried out. The fact that some components cannot be successfully switched on before the supply voltage optimisation is an interesting conclusion, as it could be an explanation for why some sensors fail the LV power-on due to low LV currents, and then show good functionality in later tests. Recovery of such sensors could improve the LV power-on yield. The incidence of underpowered sensors can be reduced by increasing the initial input voltage used in the LV power-on test.
The 50 µm sensors consistently show lower yields for the quality control tests than the 70 µm sensors. This could be due to the post-processing procedure, because the design and production is inherently the same for both thicknesses. The grinding process causes sub-surface cracks and sensor warping. The 50 µm sensors are thinner than the 70 µm sensors, and the on-chip circuitry is less protected against stress and warping.
The 50 µm sensors had a low yield for the IV scan, but otherwise showed a similar failure profile to the 70 µm sensors. The LV power-on and VDAC tests are the most limiting, then the LVDS links test, and then the internal voltages. The yield for the IV scan was artificially lowered by the effect of light incident on the testing setup. If the IV yield without light influence for 50 µm sensors is comparable to that of 70 µm will be investigated in future tests. Nevertheless, the sensors of both thicknesses show limitations in the same functions: powering, and configuration with VDACs, in particular of the analogue circuitry components.

Further investigation of wafer damages could reduce production errors and increase the yield in the long term, but is not necessary for the development of the quality control procedure itself. Systematic damage scans of sensors at inner and outer locations on a wafer could provide insights on the production process. The investigation into the location of shorts using heat sensors could also help to locate common failure points in the analogue circuitry. This could guide identification of high risk areas and to adapt routing patterns for future designs, but would need a separate investigation with a different experimental setup. A detailed noise study could provide more information on the noise levels of the two sensor types, which is necessary for the setting of efficient thresholds.

The total yields for all tested wafers are shown in Table 9.14. Wafers 420-5 and 382-9, highlighted in yellow, show the yield for the improved quality control procedure. The total weak pass yield includes sensors that passed the quality control with grades A-E, so which did not fail any individual quality control test. These show functionality and can be considered for installation. The total strong pass yield only includes sensors which passed the quality control with a grade A, so only showed strong passes. Sensors with higher grades should be prioritised for installation.

Sensor Type	Wafer	Strong Pass Yield (%)	Weak Pass Yield (%)
70 µm	420-2	16	18
	420-3	36	43
	420-5	61	66
	Total	38	42
50 µm	382-5	11	17
	382-6	30	36
	382-9	16	36
	Total	21	32

Table 9.14: Total yields of the quality control testing for all wafers presented in this thesis.

The total yield for 70 µm sensors was significantly improved by the amendments to the quality control tests and procedures. The total yield for the 50 µm sensors was reduced in comparison to the previous tests. This is due to light incidence on the setup, and is not an indication of flaws in the testing scheme or the quality of the sensors themselves. Future tests without light incidence are expected to significantly improve the total yield of the 50 µm sensors. If the IV yield relative to the other single test yields, and the total 50 µm yield relative to the single test yields, are comparable to the past 50 µm wafers, the corrected 50 µm strong pass yield can be estimated to lie at about 50%.

Chapter 10
Conclusion and Outlook

10.1 Summary and Conclusion

The aim of this thesis is the development of a quality control concept for MuPix11 pixel sensors. Quality control testing is necessary for the selection of functional sensors for the Mu3e detector. The quality control must therefore not only test the functionality of the sensors, but also verify that they fulfil certain operational requirements of the experiment. The quality control procedure was carried out and analysed for sensors of 50 µm and 70 µm thickness, as both are candidates for the Mu3e detector. The analysis of the quality control procedure not only provides information on the testing scheme, but also evaluates the performance of critical components. The acquired information on the failure profile of the sensors and limits of the quality control procedure is used to guide improvements to the testing strategy and procedures. The aim of the improvements is to reduce testing errors and expand the tests to investigate failures in detail.

The IV scan tests the ability of the sensors to operate at the HV bias voltage necessary for the sensors to reach the efficiency and time resolution requirements of the experiment. First, a suitable operational HV bias voltage is identified to guide the evaluation. This is identified through analysis of the leakage current at different HV bias voltages, which is indicative of the operational stability and noise of the sensor. Test beam data and the time resolution requirements for the Mu3e experiment are also taken into account. The proposed values for the operating bias voltages are $-30\,\mathrm{V}$ for 70 µm sensors and $-15\,\mathrm{V}$ for 50 µm sensors.

The sensors have a region with a high defect concentration on the back-side, which is caused by damage to the crystal lattice during grinding. Due to the 50 µm sensors only having a very thin layer of silicon substrate, the pixels must operate at a HV bias voltage at which this damage region is depleted, in order to fulfil the efficiency and time resolution requirements of the detector. This can reduce the yield due to the leakage current increase when this damage region is depleted. The possibility of operation at lower bias voltages for 50 µm sensors should be investigated, as efficiency measurements were only available for one sensor at the time of writing.

Investigations into the depletion process showed two separate stages of current increase due to the depletion zone reaching the damage region in two phases. This helped to understand the operational state of the sensor at different bias voltages.
The total yield of the improved IV scan is 25.0 % for 50 µm sensors and 88.6 % for 70 µm sensors. The low 50 µm yield is not reflective of the sensor's functionality or a flawed evaluation scheme, but the consequence of a systematic external effect on the 50 µm tests. An investigation into the light dependency of the 50 µm sensors showed that light incidence significantly raised the leakage current, causing functional sensors to fail the IV scan. The identification of light dependency as a source of false failures in the quality control procedure has considerable significance, as the correction of this effect will improve the accuracy of the evaluation performed by future IV scans. The IV yield for 50 µm is estimated to lie at around 70% when the effect of light incidence is removed. This estimate assumes that the relative pass rates between individual tests are comparable between the previous and improved testing schemes.

The LV power-on test evaluates a sensor's ability to power key elements of the on-chip circuitry. It must ensure that the upper limits on individual sensor power consumption before and after the powering of the circuitry are not exceeded, in order to preserve uniformity of power consumption and heat dissipation in the Mu3e detector. The yield for the improved LV power-on test is 70.5 % for 50 µm sensors and 79.5 % for 70 µm sensors. The LV power-on test is one of the most selective tests for both sensor thicknesses, the 50 µm IV result aside, and a limiting factor for the total quality control yield for 70 µm sensors.
The evaluation performed by the LV power-on test is limited because the supply voltage is not optimised before the test. While most sensors are evaluated accurately, a small number wrongly fail the LV power-on because they are insufficiently powered due to voltage drops between the voltage supply and the sensor's internal power grid. These would be corrected for during operation in the detector by voltage optimisation. The evaluation of powering before voltage optimisation in the quality control procedure therefore slightly reduces the yield. Sensors which show functionality after the voltage optimisation should be recovered to reduce this yield loss. The LV power-on should also be carried out at a higher initial input voltage to reduce these failures due to underpowering.
The high selectivity of the LV power-on test is in part due to the testing procedure. Therefore, the identification of this failure mode is a key step towards a more accurate evaluation of sensor powering in future quality control tests.

The internal voltages test evaluates a sensor's ability to optimise the supplied voltage. The optimisation procedure adjusts the supply voltage to correct for variations in the resistance between the voltage supply and sensor's internal power grid, to ensure that every sensor receives the same supply voltages. The test is successful in evaluating the voltage

optimisation, and in ensuring that the current consumption is still within the constraints of the experiment after the optimisation. The optimisation failures where investigated to see if the optimisation was limited by a particular supply voltage. The failure rate of the voltage optimisation did not show significant deviation between the supply voltages, or between the sensor partitions. No specific limitation was identified.
The yield of the improved internal voltages test is 77.3 % for 50 µm sensors, and 86.4 % for 70 µm sensors. The internal voltages test was one of the least selective tests, showing that the voltage optimisation had a high success rate and was not a limiting factor for sensor functionality.

The VDAC scan tests a sensor's behaviour in response to the changing of key VDAC values. The changes in the applied voltage and LV current are measured and plotted against the VDAC value. VSS1 and VSS2 show the effect of the ref_VSS VDAC in the two sensor partitions. Their current scans show the increase in LV current when the amplifier reaches its operational range. The current scan for BLPix shows the increase in LV current when the line driver reaches its operational range. Both the amplifier and line driver are analogue circuitry components. There is no significant deviation in the operational ranges for the amplifier between the two sensor thicknesses, nor between the two sensor partitions.
ThHigh and ThLow change the comparator setting, while Baseline sets the baseline voltage for the digital circuits. ThHigh, ThLow and Baseline show a linear voltage increase and a constant LV current with increasing DAC value, as expected.
The yield of the VDAC scan was limited by the performance of the sensors in response to VSS1, VSS2 and, in particular, BLPix. The analogue components show a higher failure rate than the digital components, which is expected for the sensor design, which features long analogue readout lines which are prone to shorting due to production errors. The VDACs showed a higher failure rate for 50 µm sensors than for 70 µm sensors. This implies that the thinning process may cause more damage to the analogue components for the 50 µm sensors. The grinding process can cause damage in the form of sub-surface cracks, or breakage in the metal layers due to warping. The warping may be stronger for the thinner 50 µm sensors, and therefore cause more damage to the on-chip circuitry, especially to the long analogue readout lines. However, the conclusiveness of this evaluation is limited by the sample size of observed sensors.
The execution of the VDAC scan was changed in response to the results of the first quality control tests. The simultaneous testing of the VDACs led to superposition of many separate effects, and made it difficult to disentangle the effects of the individual VDAC changes. The analysis of the sensors' response to the individual VDACs was made possible by testing the VDACs sequentially. The evaluation scheme was adapted to the new VDAC scans, and to evaluate the current scan, instead of the voltage scan. This improves

the precision of the evaluation, as it explicitly looks for the turn on of individual components.
The yield of the improved VDAC scan is 72.7 % for 50 µm sensors and 79.5 % for 70 µm sensors. The VDAC scan was a limiting factor for the 70 mum yield, and one of the most selective tests for both sensor thicknesses.

The LVDS links test evaluates a sensor's ability to send out data without 8b/10b errors at different VPVCO (VNVCO) settings. The test showed success in evaluating the quality of the output data. At a Baseline level of 112, the noise level prevented error-free readout at the lower effective threshold of 118 (ThHigh) and 117 (ThLow), but the raised threshold of 138 (ThHigh) and 137 (ThLow) was not affected by noise.
Links C and D consistently showed more errors than links A and B. This is caused by a voltage drop across the links, which is inherent to the link powering concept. Almost all sensors which could transmit data without errors could do so at multiple VPVCO (VNVCO) values. The best performing VPVCO (VNVCO) values are the same for both sensor thicknesses: 18, 23 and 28. This can be used to guide the VPVCO values used in the Mu3e detector. The yield of the LVDS links test was 75.0 % for 50 µm sensors and 81.6 % for 70 µm sensors. The test was not highly selective, so the performance of the LVDS links was not a limiting factor for sensor functionality.

Improvements were also made to the general testing strategy. The LVDS links test shows that the noise level is above the default threshold of 118, and therefore close to the safety threshold previously set for all tests, 123. This safety threshold was therefore was raised to 153 to avoid noise effects influencing the test results. As described in Section 8.1, the contact strategy was also changed from a fixed to a flexible contact strategy to ensure that each sensor is well-connected during the test, and to reduce excess pressure on the sensors beyond the point of contact. The thin sensors are fragile, and easily damaged by excess or uneven pressure. A chip recovery strategy was introduced to reduce yield loss due to errors in testing, and efforts were undertaken to understand the nature of production damage and make systematic production errors easier to identify.

The total yields of the improved testing procedure are shown in Table 10.1. The grading scheme is applied as discussed in Table 6.2 in Chapter 6.

	Total Quality Control Yield (%)	
	Strong (Grade A)	Weak (Grades A-E)
50 µm	16	36
70 µm	61	66

Table 10.1: Total yield of the improved quality control procedure for MuPix11.

Sensors with grades A-E should be considered for installation at the Mu3e detector, but those with higher grades should be prioritised. The total quality control yield for 70 µm sensors was improved by the amendments to the quality control procedure. The yield for 50 µm sensors was reduced in comparison to the previous tests, but this was due to the effect of light incidence, not the changes made to the testing procedure or the functionality of the sensors.
Future tests without light incidence will show a more accurate failure profile, which may reveal a different limiting factor for the 50 µm sensors. For example, the 50 µm yield is likely be limited by the VDAC scan, due to the similarity of the failure profile to that of the 70 µm sensors. The total quality control yield for 50 µm sensors is estimated to increase to about 50% when the effect of light incidence is removed.

The quality control procedure developed in the context of this thesis has proven to be accurate in the evaluation of a sensor's functionality and ability to fulfil key operational requirements of the Mu3e detector. Within this thesis frequent failure modes are investigated in detail, and the information used to evaluate the accuracy of the test results and suggest improvements for handling and testing strategies. The artificial reduction of the yield for 50 µm is a consequence of an external influence on the testing setup, not of errors the individual testing procedures. Furthermore, the identification of the light dependence of 50 µm sensors was a key step to the success of future quality control procedures. The ability of the quality control tests to identify and recover false failures is exemplified by the recovery of sensors with powering issues through voltage optimisation.
Therefore, the improvements and investigations presented in this thesis enabled the development of an effective quality control procedure for MuPix11 HV-MAPS, in the context of vertex detector pre-production for the Mu3e experiment.

10.2 Outlook

The quality control tests presented in this thesis were performed in the context of vertex pre-production testing. However, the MuPix11 sensor will not only be used for the vertex detector, but also for the outer layers of the Mu3e detector, which will require a large number of sensors. To speed the testing process for the outer layers, a high-precision needle contact system guided by pattern recognition will be used. The only differences to the setup described in this thesis concern sensor handling, but not the powering or data readout strategies. The quality control procedure presented in this thesis is therefore directly transferable to the quality control for outer layer pre-production testing.

The quality control procedure will require targeted optimisation for the production testing phase. To accelerate the quality control for the 2844 sensors required for the pixel detectors, the extra measurements taken to investigate failure modes will be removed from the tests and the testing procedure limited to the data needed for evaluation. This will require further research and development.

The quality control yield must be considered in the planning for detector production. The 50 µm sensors carry a clear advantage for the accuracy of track reconstruction in the Mu3e detector. However, the possibility of using the higher yield 70 µm sensors for some detector sections should be explored as a way of accelerating the quality control and the subsequent assembly of the pixel detector. Since a good yield is critical for the production of the Mu3e tracking detector, this study has provided a significant contribution to the decision on the thickness of the outer layers.

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Declaration of Authorship

I hereby declare that I have written this thesis independently, and that none other than the referenced sources and resources were used.

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