Thomas Rudzki - 4th Mighty Tracker Workshop - Liverpool 2024
4.7.2024

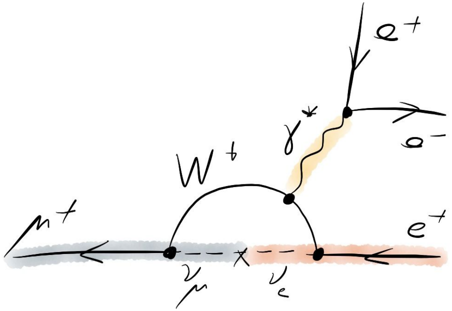
Lessons from Mu3e

Handling, assembly and testing of HV-CMOS pixel chips

Physics motivation

Charged lepton flavor violation (CLFV)

- LFV observed in neutrino mixing
- **Charged** LFV not yet observed
- μ decays are clean searches
  (only decay products ν, e, γ)

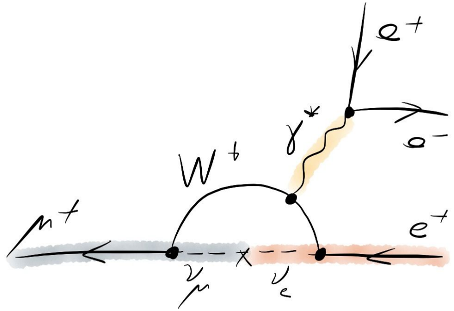


Standard Model $\mu \rightarrow eee$ decay, BR < 10^{-54}

Physics motivation

Charged lepton flavor violation (CLFV)

- LFV observed in neutrino mixing
- **Charged** LFV not yet observed
- μ decays are clean searches
  (only decay products ν, e, γ)
- Sensitive to **beyond SM** loop & contact interactions
- Current Limit of $\mathbf{\mu^+ \rightarrow e^+ e^- e^+}$:
  SINDRUM: BR < 1×10^{-12}



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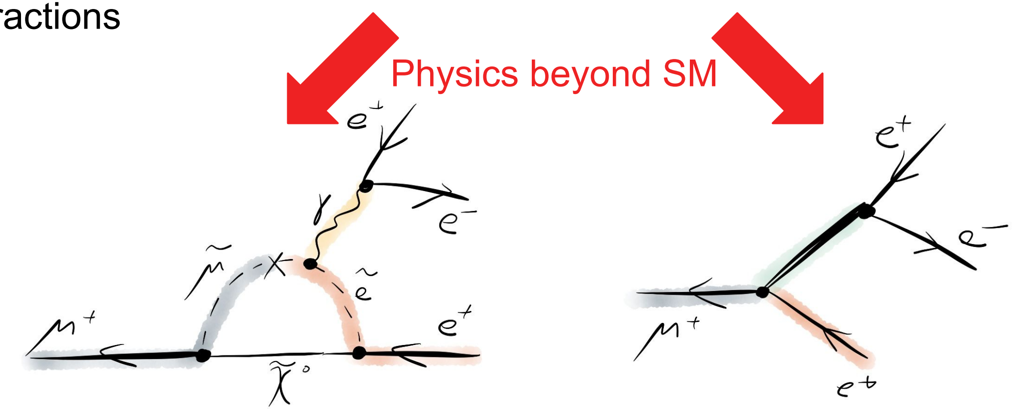

Goal of Mu3e: Improve single event sensitivity by 3 to 4 orders to $< 2 \cdot 10^{-15}$ ($< 10^{-16}$ in Phase II)

The Mu3e experiment

- **High muon rate** needed → 10^8 μ decays/s
- DC surface muon beam at PSI (πE5 beam line)
    - Low momentum, 28 MeV/c
    - Muons stopped on target
    - **Decay at rest**

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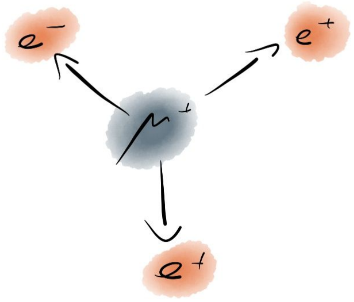
- **Signal decay: μ→eee**
  - Three prompt $e^{+/-}$
  - Common vertex
  - $\Sigma E = m_\mu$
  - $\Sigma \mathbf{p} = 0$



Signal decay

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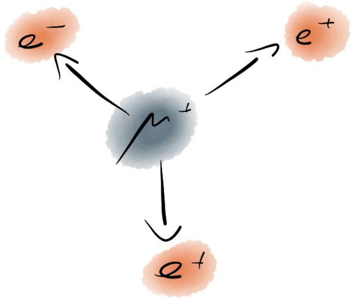
- **Main backgrounds:**
  - Internal conversion

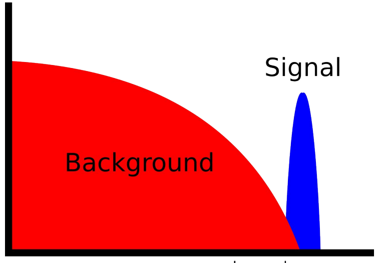


Signal decay

vs.

Internal conversion

Excellent momentum resolution needed
Max. momentum: 53 MeV/c
➡ resolution is **multiple Coulomb scattering limited**



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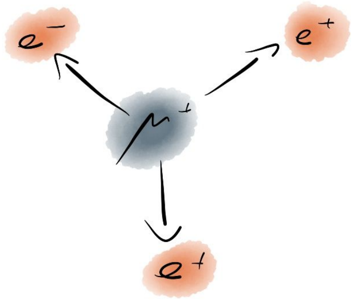
- **Main backgrounds:**
  - Internal conversion
  - Accidental background



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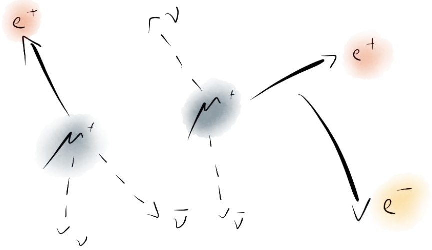


Michel e^+ & e^- from Bhabha or γ conversion

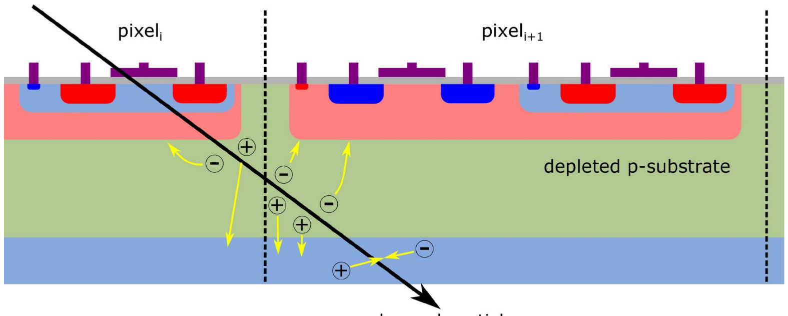
Time and vertex resolution
- Fast detectors
- High granularity

High rate capability

MuPix sensor

High-Voltage monolithic active pixel sensors (HV-MAPS)

- Monolithic: Detection and readout on the same chip
- In-pixel electronics
- Deep n-well diode
- Charge collection via drift (high voltage)
- Can be thinned to ≤ 50 μm



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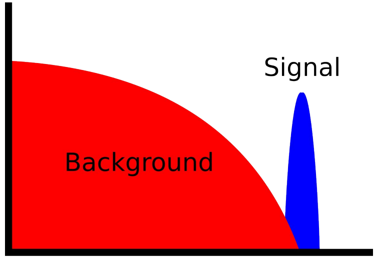

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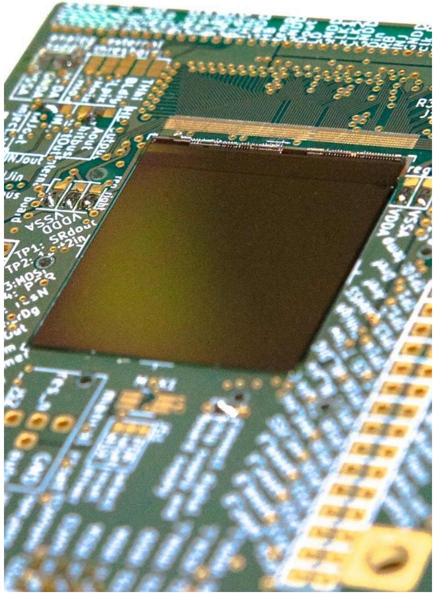
MuPix11

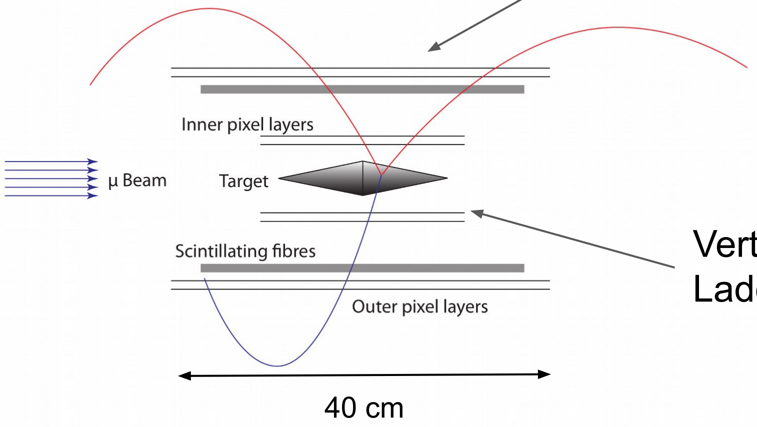
- Chip size: ~ 20 x 23 mm²
- Pixel size: 80 x 80 μm²
- time resolution < 20 ns
- Hit efficiency > 99 %



Detector design

- 4x **pixel** tracking layers only ➡ minimize material
- 1T magnetic field

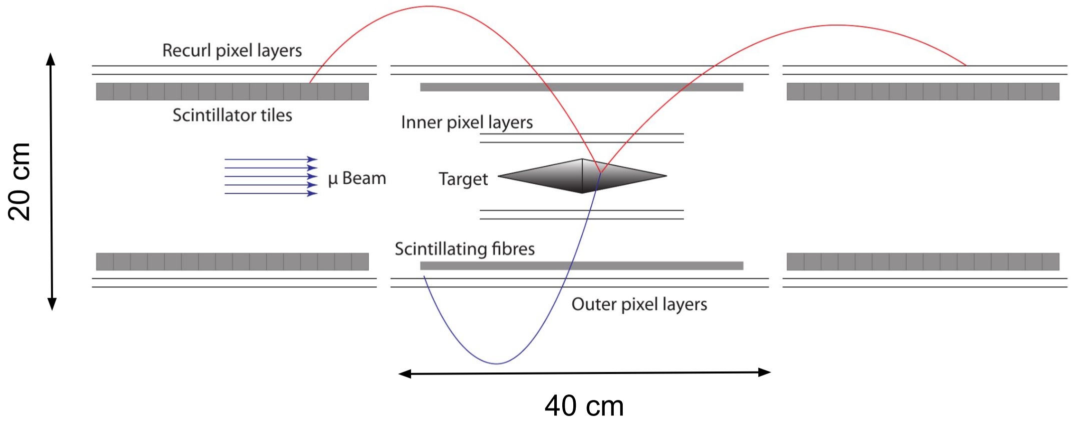
Outer pixel layer:
Ladders with 17/18 chips



Vertex Detector:
Ladder with 6 chips

Detector design

- 4x **pixel** tracking layers only ➡ minimize material
- 1T magnetic field
- Recurl pixel station to get **optimal momentum resolution**
- **Fast scintillating fiber and tile detectors** for optimal timing resolution



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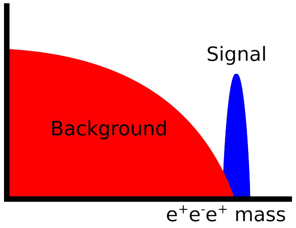


Time and vertex resolution
- Fast detectors
- High granularity

High rate capability

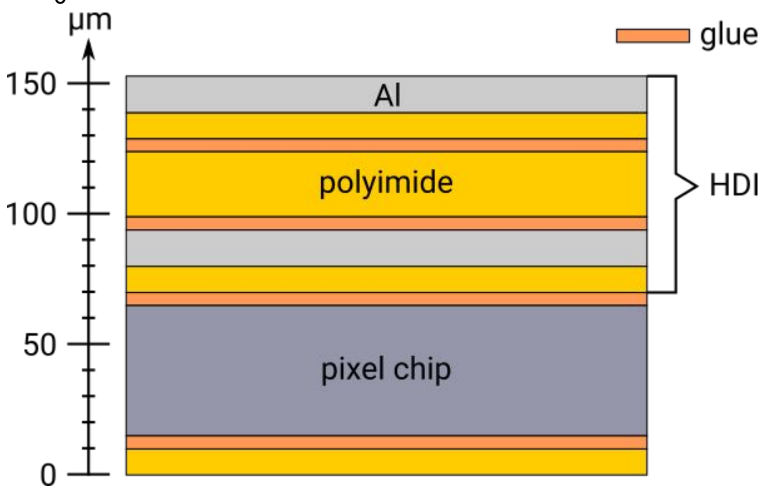
Low mass pixel detector

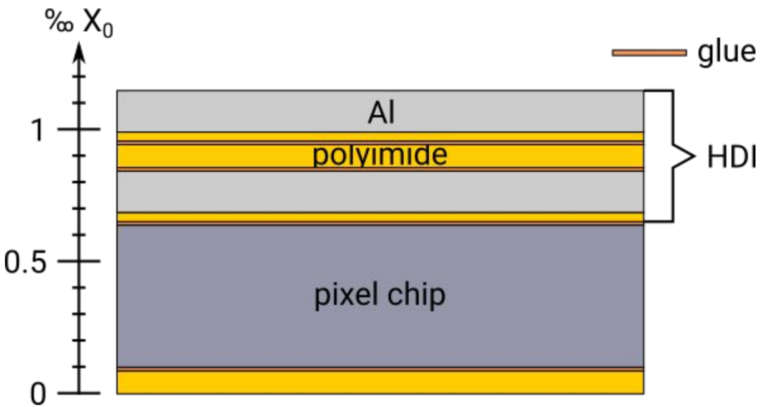
Detector composition:

- High-density interconnect (HDI) + HV-MAPS (50 µm thin)
- HDI = Aluminium-based flexprints
- $X/X_0 \approx 1.15$ ‰ per tracking layer

Aluminium vs. Copper

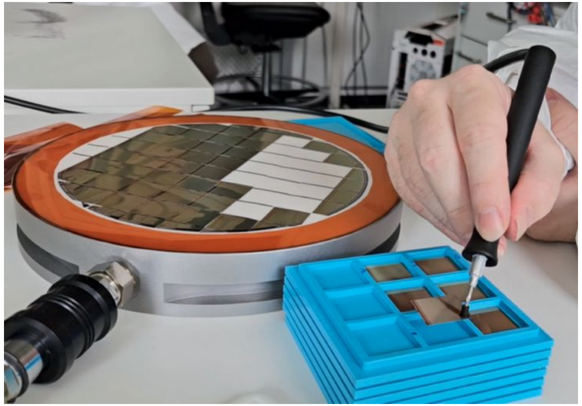
Radiation lengths
$X_0(Cu) = 12.86\ g/cm^2 \rightarrow 1.436\ cm$
$X_0(Al) = 24.01\ g/cm^2 \rightarrow 8.897\ cm$

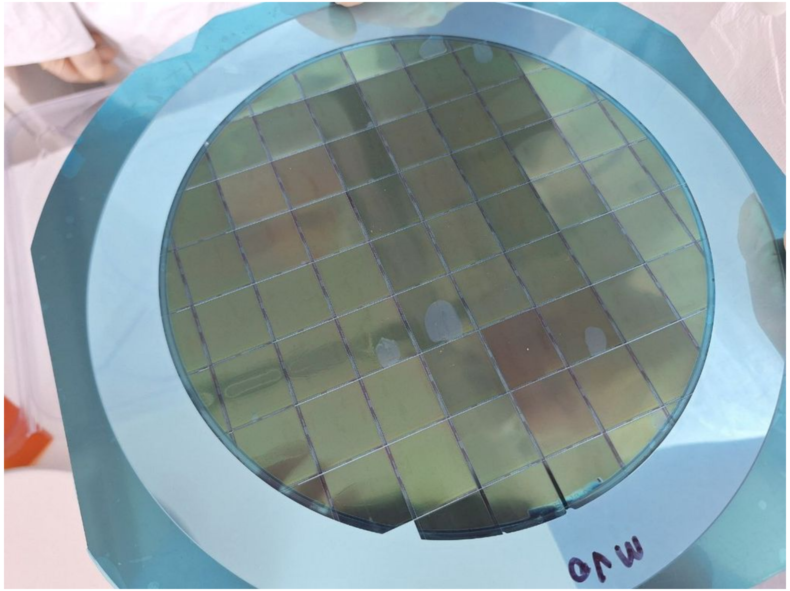




From chips to a detector

1. Receive **thinned** and **diced** wafers after **plasma etching** from OPTIM (France) on **blue tape**
   a. Place wafer on ceramic chuck
   b. UV curing
   c. **Manual peeling and picking**





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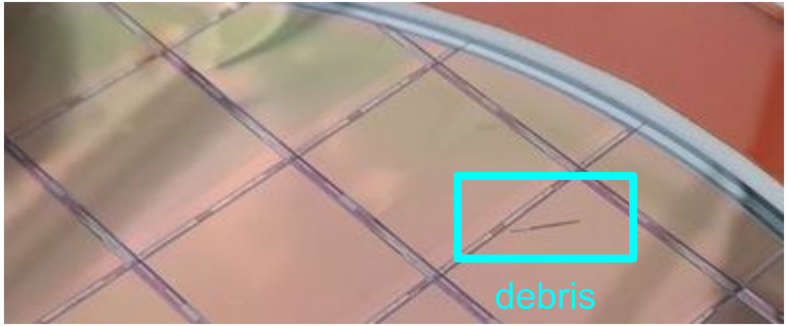
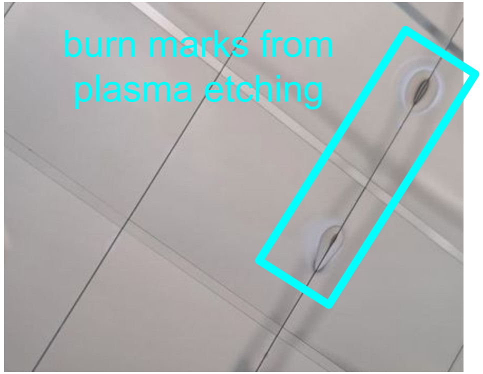
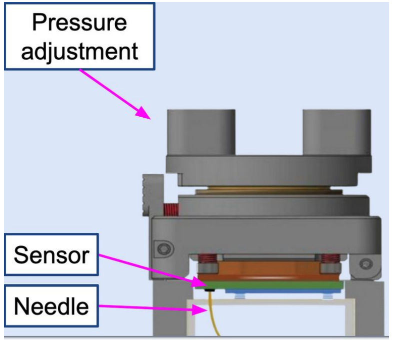




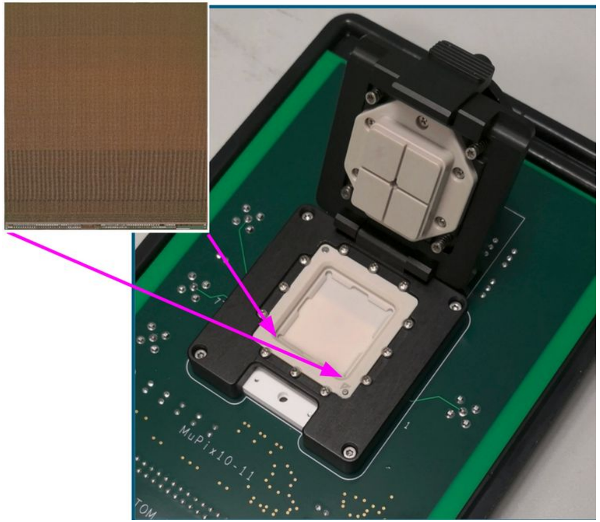
- **Time on blue tape** varies due to transport time (needs to be < 2 weeks)
- **Debris** from area between chips can slip below chips
- Observed yield increase over time
  - Better peeling with experience?
  - Thin chips appear to be **very sensitive to the peeling procedure**
- **Burn marks** from plasma etching visible
  - No impact on yield observed so far

From chips to a detector

2. **Chip QC**
   a. **Manual chip test card** at PSI and Heidelberg for the vertex detector
   b. **Automatized** testing with **probe station** in Oxford for outer layers (not yet fully ready)
   c. Chip QC implemented in [MIDAS]



Manual MuPix probe card
from PTSL

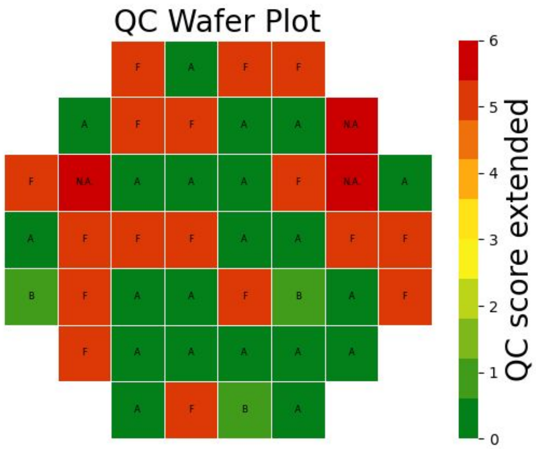


From chips to a detector

2. **Chip QC**
   d. **Check contact**
   Chip in contact with needle, power consumption within specs
   e. **IV scan**
   Necessary depletion voltage can be reached
   f. **On-chip voltages**
   Supply voltage adjustment, amplifier voltage (VSSA) correctly generated on chip
   g. **VDAC tests**
   Test of adjustment of thresholds etc.
   h. **Data transmission**
   Test integrity of high-speed LVDS links (1.25 GBit/s)
   i. **Noise scan**
   Record noise and mask noisy pixels

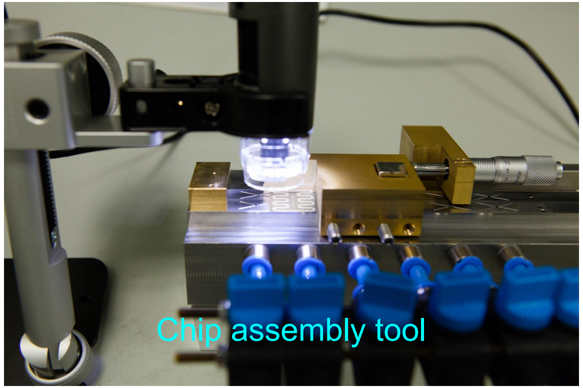
From chips to a detector

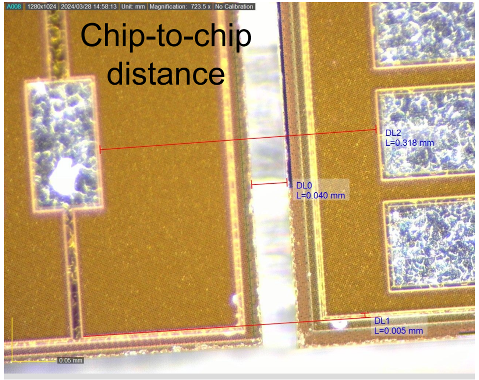
2. **Chip QC**
   j. **Test duration** ~ 30 to 40 min per chip
      Being optimized for automatized testing: Goal 1 wafer per day (44 chips)
   k. **Yield:** ~ 50 % for 50 µm; ~60 % for 70 µm **(very preliminary)**
      Main issues:
      i. Mechanical damage
      ii. IV problems (HV short)

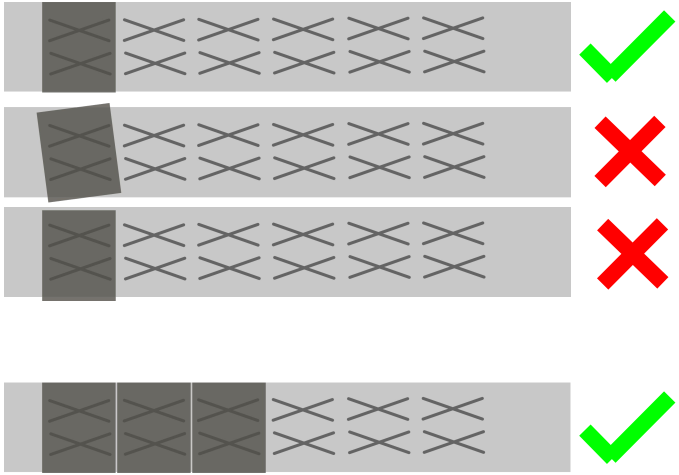


From chips to a detector

3. **Ladder assembly**
   a. **Manual procedure** for vertex detector
   b. Chip placement on assembly chuck using a slider (confined two dimensions)
   c. Check chip pitch with microscope

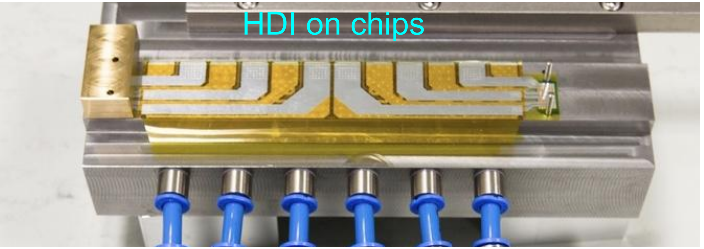


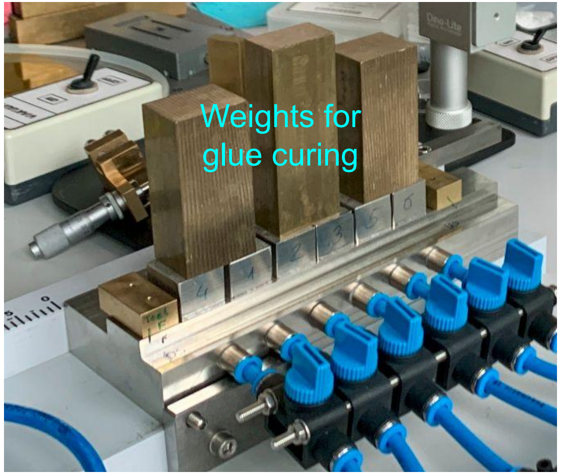




From chips to a detector

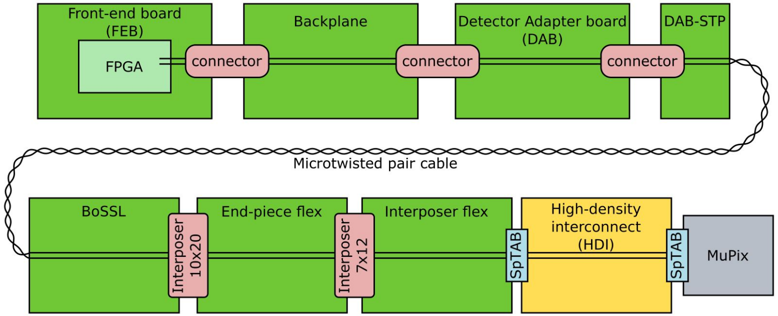
3. **Ladder assembly**
   a. **Manual procedure** for vertex detector
   b. Chip placement on assembly chuck using a slider (confined two dimensions)
   c. Check chip pitch with microscope
   d. Apply glue in quincunx pattern on chip
   e. Put on HDI
   f. Align by hand under microscope
   g. Apply weights + glue curing





From chips to a detector

4. **Ladder QC**
   a. Basically repetition of chip QC protocols
      i. Plus detailed signal transmission scan and recording a hit map using a ^{90}Sr source
   b. Performed with **complex vertical slice** (also during pre-production), not on a simplified readout chain ➡ Due to missing personpower
   c. Lost a lot of time on debugging
   d. Gained a lot of experience on the final hardware
   e. Main problem:
      i. **Data readout via μ-twisted pair cable (a MUST due to limited space for services)**
         ➡ Hardware problems, worse data transmission with first batch
      ii. LVDS-related DAC settings needed to be optimized
         ➡ Longer signal lines compared to chip QC
         ➡ Large parameter space



Vertical slice of Mu3e pixel readout inside magnet

From chips to a detector

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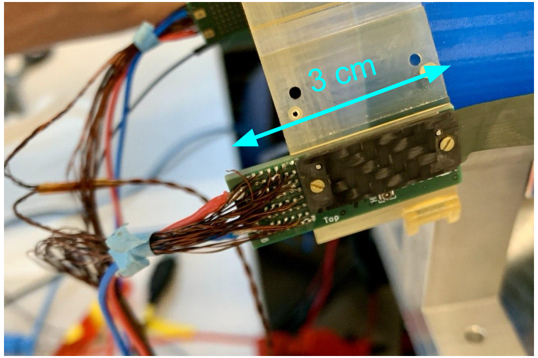
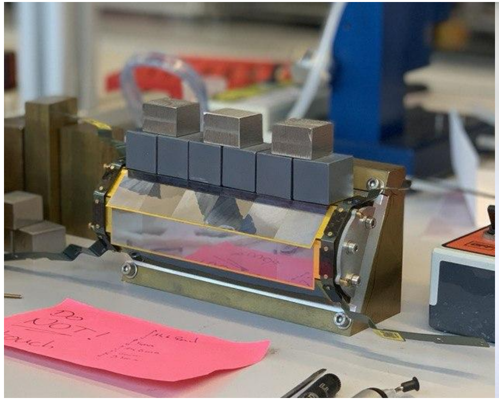
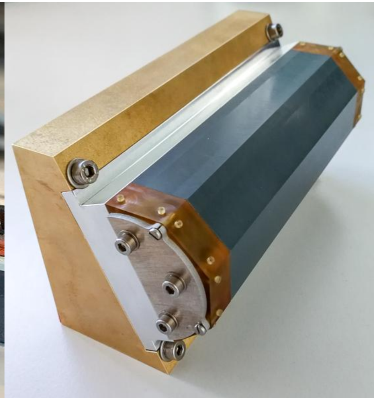


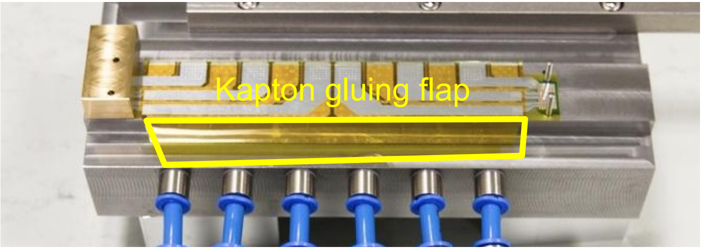
BoSSL PCB connecting µ-twisted pair cables (22 pairs) with the end-piece flexprint of the vertex detector

From chips to a detector

5. **Module assembly**
   a. **Manual procedure**
   b. Ladders glued together via Kapton flap
   c. Electrical connections via interposer pin connector to end-piece flexprint
   d. **Self-supporting** half-shell structure
   e. Handling of modules is surprisingly easy

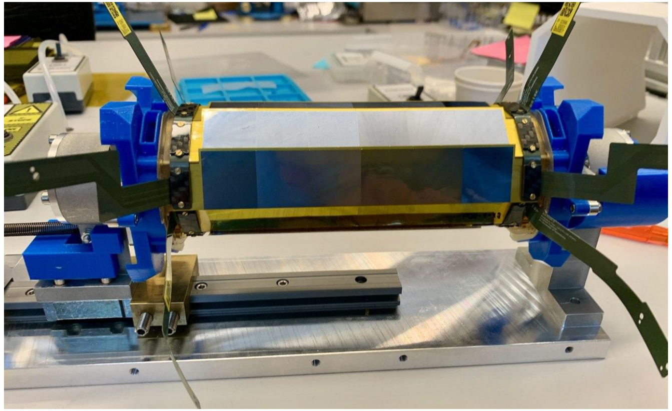


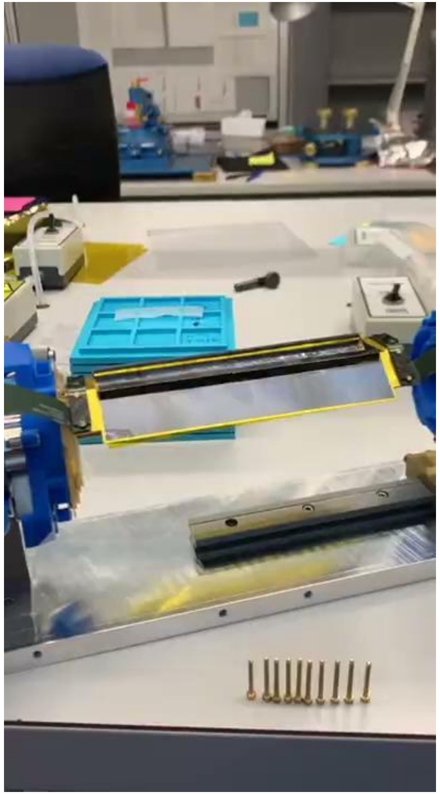




From chips to a detector

6. **Barrel assembly**
   a. Modules are **mounted on a specific tool** to the full vertex detector outside the experiment
   b. Vertex detector is **inserted between the beampipes as one unit**

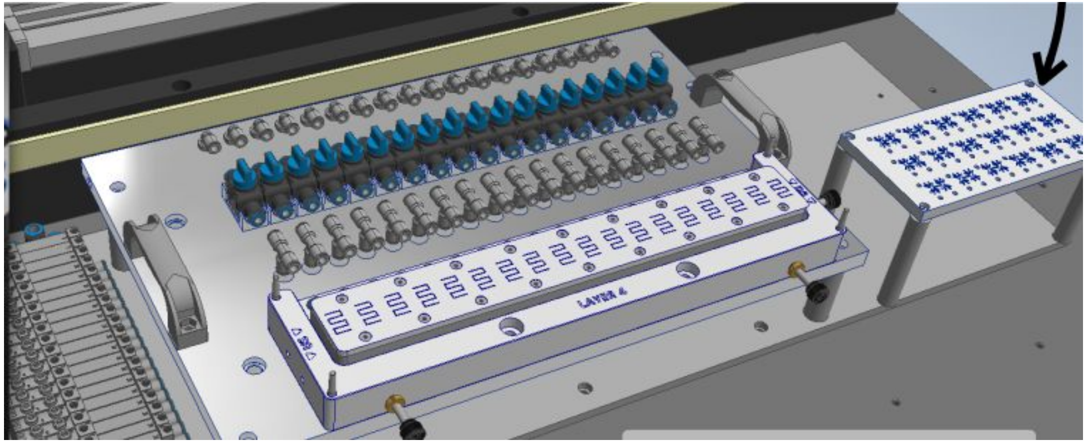




Layer 1 module mounted only on one side

The outer pixel layers

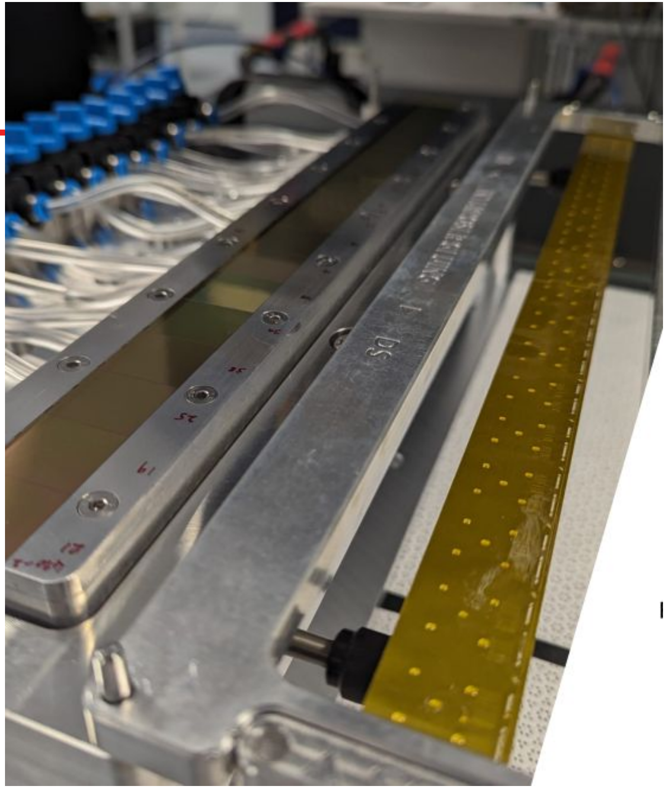
- **Automated** chip placement on gantry



Automated chip placement tooling on the Oxford gantry.
18 chips are placed with a chip gap of 40 µm.

The outer pixel layers

- **Automated** chip placement on gantry
- Alignment of components via **precise tooling** (not fully by hand as for vertex detector)

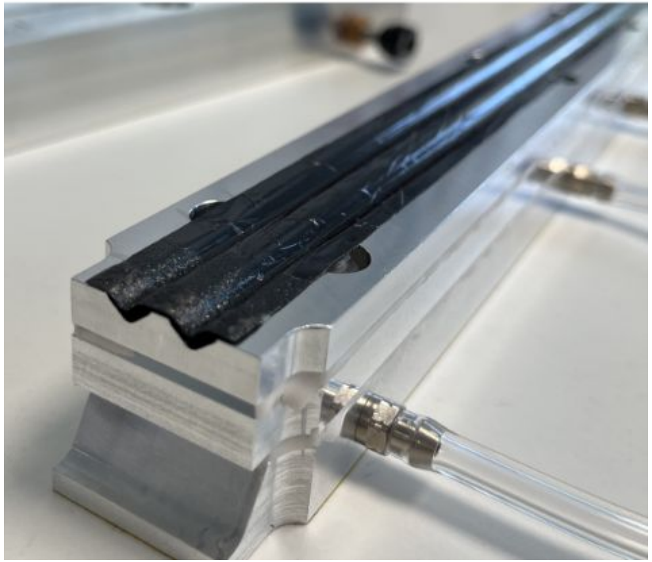


Positioned chips on chuck (left).
HDI in ring frame (pre-aligned) with glue deposited in quincunx pattern.

The outer pixel layers

- **Automated** chip placement on gantry
- Alignment of components via **precise tooling** (not fully by hand as for vertex detector)
- Additional mechanical support using v-folds
  - Past baseline: Kapton-based v-fold
  - Current baseline: **Carbon stiffener** (25 µm) + 8 µm co-cured Kapton layer (el. isolation)

    ➡ **Low material budget with maximum stability**



Carbon stiffener for a Mu3e outer pixel ladder.
You can look at a real prototype after the talk.

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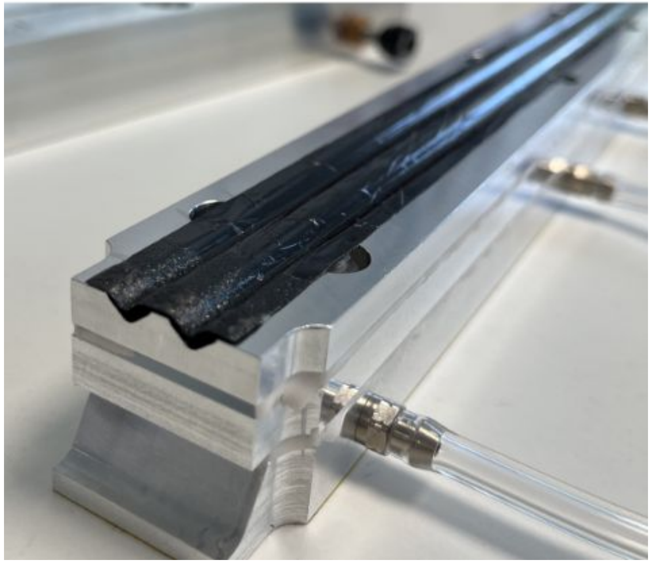
- **Chip and ladder QC:**
  - Chip QC on probe station in Oxford (automated)
  - Ladder QC in thermal test box (using simplified readout board, not full QC)
  - All processes to be verified within this year



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Lessons learned (an incomplete list)

- Thin monolithic silicon chips require careful/trained handling
  - Clean work (gloves, dust free environment or proper cleaning)
  - Clearly defined working steps ➡ **production protocols/checklist** (also for experienced colleagues)
- Benefits from **early stage prototyping** (even if geometry is not fully finalized)
  - Many smart design improvements can be triggered early enough
  - Go through every working step (even the ones which appear to be simple)
- **Transfer knowledge** between production sites
- **Modular design** in as **little flavours** as possible
  - Think about yield and spares
  - Design ladders/modules in a smart way ➡ Goal: No multiple flavours of interfaces
- Verify functionality of **all non-standard components** already way before (pre-)production

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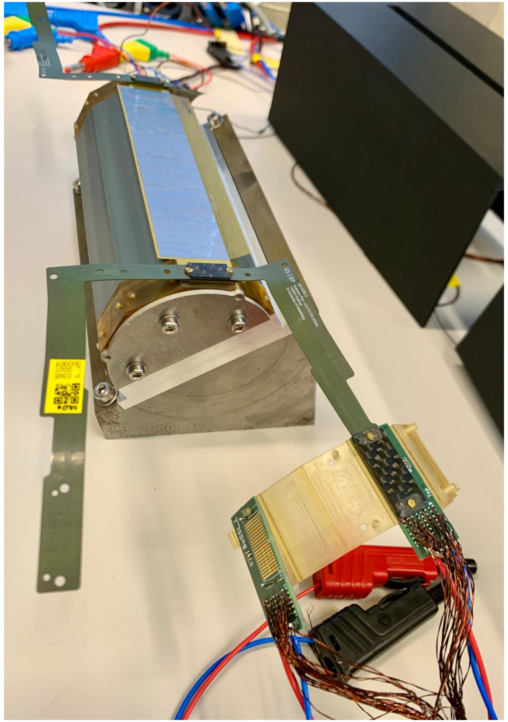
We did not adequately follow these guidelines

Summary

- After **four years of serious prototyping** Mu3e went into **production phase this year**
- Vertex detector production ongoing
  - Full vertical slice proved functionality
  - Getting ready for cosmic run in autumn 2024
- Outer layer pre-production prepared
  - Currently establishing chip and ladder QC procedures
- Building my own Mu3e-like detector?
  - Current detector ladder **design transferable** to different detector geometries **(modularity)**
  - Cu-based HDIs with wire bonds can replace our Al-based ones when material budget is not that crucial (≥ 0.15 % X_0) **(standard components wherever possible)**
  - Less compact design (e.g. for services) avoids most problems we had
  - Currently no chip vendor for MuPix sensors anymore
  - But: Our ambitious detector design is viable. **Don’t be afraid of crazy ideas!**



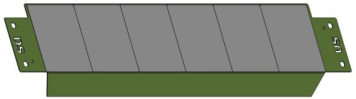
QC stand of 1st final vertex detector ladder

Back up

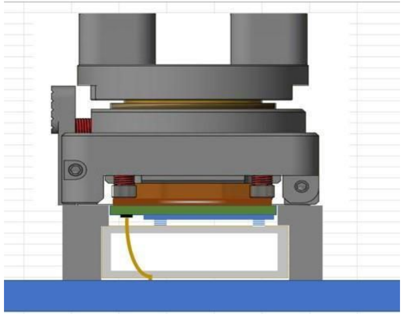
Low mass pixel detector

From HDIs and sensor chips to a detector

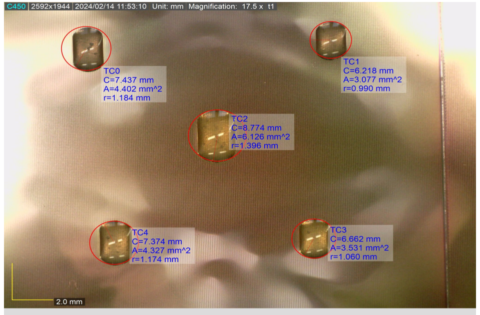
1. MuPix chips are **qualified** in probe card
2. MuPix chips are **aligned** on assembly tool
3. MuPix chips are **glued** on the HDI and **bonded** to a **ladder**



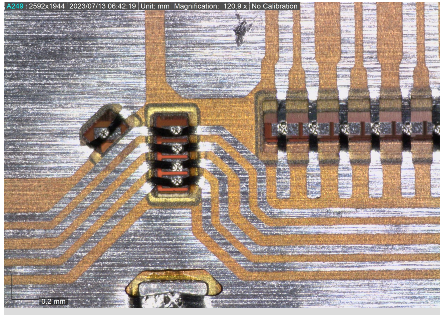
Ladder



Manual MuPix probe card



Glue dots on a MuPix chip

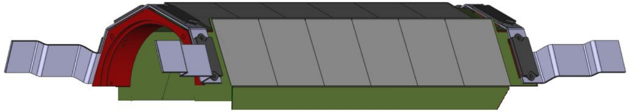


spTAB connections from HDI to the MuPix chips

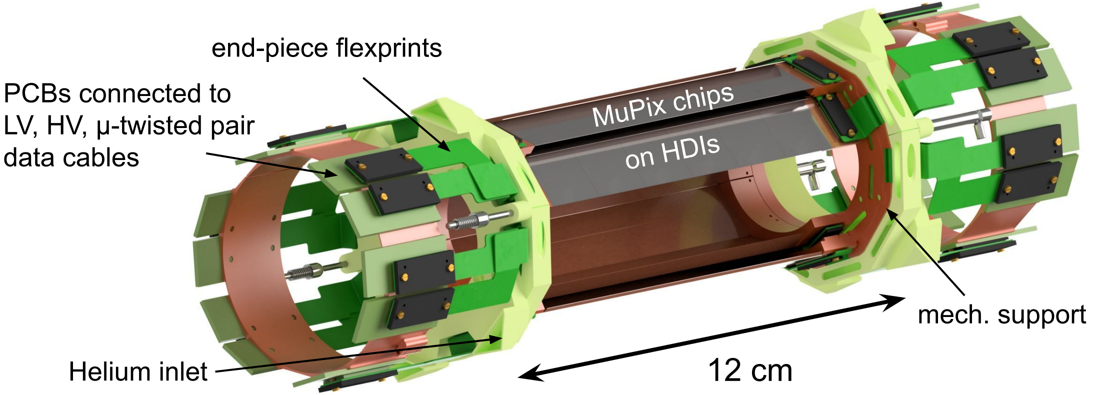
Low mass pixel detector

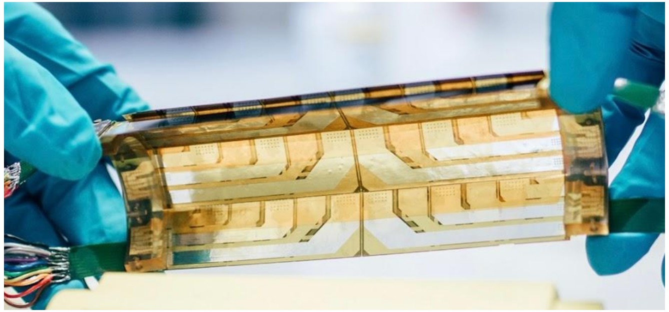
From HDIs and sensor chips to a detector

1. MuPix chips are **qualified** in probe card
2. MuPix chips are **aligned** on assembly tool
3. MuPix chips are **glued** on the HDI and **bonded** to a **ladder**
4. Ladders are glued to each other forming half-shell **modules**
5. 4 modules mounted as two barrel layers forming the **vertex detector**



Module





Silicon heater mock-up module