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THE MU3E VERTEX DETECTOR -

CONSTRUCTION, COOLING,

AND FIRST PROTOTYPE OPERATION

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źródła mojej pasji do przyrody i nauki

Abstract

The Mu3e experiment searches for the charged lepton flavor violating decay $\mu^+ \to e^+e^-e^+$ with an aimed single event sensitivity of $2 \cdot 10^{-15}$ in phase I. To achieve this goal, the highest momentum resolution possible is approached, which is mainly affected by multiple Coulomb scattering. This results in extremely tight constraints on the material budget to the level of 0.1 % radiation length per layer for the tracking detector.

The Mu3e pixel detector is based on High-Voltage Monolithic Active Pixel Sensors (HV-MAPS) developed for this project, the MuPix, which can be thinned to 50 µm. The electrical services and the support are realized by ultra-thin (≈ 80 µm) structured aluminum-polyimide laminates. Furthermore, the detector is cooled by gaseous helium, a novelty for particle detectors.

This thesis covers the construction of detector mock-ups in preparation for the final production of the Mu3e vertex detector, the studies of the helium cooling system, and the operation of a first functional prototype of the Mu3e vertex detector.

The mock-up construction demonstrated that an excellent longitudinal chip placement precision of $\sigma = 4$ µm and a lateral precision of $\sigma = 3$ µm is achieved with a manual approach. An average glue thickness of only (5.3 ± 1.7) µm for the joint between chips and laminates is realized.

The helium cooling system is verified to be sufficient to cool the Mu3e vertex detector. To prove this, the thermal-mechanical mock-ups were heated actively and cooled by the helium cooling system. For a heat dissipation of $350\,\mathrm{mW/cm^2}$, all chip temperatures are found to be below 70 °C for an inlet helium temperature of 0 °C. The temperature change during heating up and cooling down can be described by a time constant of about 2 s to 3 s.

A first functional vertex detector prototype has been operated under Mu3e-like conditions. The communication with the vertex detector and the readout of its hits is performed by the Mu3e DAQ, which is proven to be functional. The hits from different portions of the detector are correlated, and the results are in agreement with the expectation for all the target geometries that have been used. The conceptual detector design and the functionality of the novel detector cooling system are validated, which paves the way for the detector production in 2022.

Kurzzusammenfassung

Das Mu3e-Experiment sucht, mit einer angestrebten Sensitivität von einem Signalzerfall in $2 \cdot 10^{-15}$ Zerfällen in Phase I, nach dem Leptonfamilienzahl-verletzenden Zerfall $\mu^+ \rightarrow e^+e^-e^+$. Um dieses Ziel zu erreichen, wird die bestmögliche Impulsauflösung angestrebt, die hauptsächlich von Coulomb-Vielfachstreuung limitiert wird. Das führt zu einer starken Begrenzung der erlaubten Materialdicke von nur 0.1 % einer Strahlenlänge pro Detektor-Lage.
Der Mu3e-Pixel-Detektor baut auf Hochspannungsgetriebenen monolithischen aktiven Pixelsensoren (kurz: HV-MAPS) auf, die speziell für dieses Projekt entwickelt wurden. Diese sog. MuPix-Sensoren können auf eine Dicke von nur 50 µm gedünnt werden. Die elektrischen Leitungen sowie die Halterung des Detektors werden durch sehr dünne Aluminium-Polyimid-Folien (80 µm) realisiert. Gekühlt wird der Detektor durch ein Kühlsystem, das auf gasförmigem Helium beruht, einer Neuheit im Feld der Teilchenphysik.
Diese Arbeit umfasst, neben der Konstruktion von Detektormodellen, welche die finale Produktion des Mu3e-Vertex-Detektors vorbereiten, Studien der Helium-Kühlung und den Betrieb eines ersten funktionellen Prototypen des Mu3e-Vertex-Detektors.
Die manuelle Konstruktion von Detektormodellen hat eine ausgezeichnete Präzision bei der Positionierung von Sensoren von $\sigma = 4$ µm in longitudinaler und $\sigma = 3$ µm in lateraler Richtung vorgeführt. Bei der Klebung von Sensoren und Leiter-Folie wurde eine durchschnittliche Klebedicke von nur (5.3 ± 1.7) µm erreicht.
Es konnte gezeigt werden, dass das Helium-Kühlsystem den gesetzten Anforderungen genügt. Bei Messungen mit beheizbaren Detektormodellen mit einer Heizdichte von 350 mW/cm^2 war die Temperatur aller Chips bei unter 70 °C für eine Eingangstemperatur von 0 °C des Gases. Der Temperaturänderung der Chips kann durch eine Zeitkonstante von ungefähr 2 s bis 3 s beschrieben werden.
Ein erster funktionsfähiger Vertex-Detektor-Prototyp konnte unter Mu3e-nahen Bedingungen betrieben werden. Die Kommunikation mit dem Detektor und die Auslese von Daten durch die Mu3e-DAQ konnte deren Funktionsfähigkeit verifizieren. Die aufgenommen Teilchentreffer in verschieden Teilen des Detektors waren miteinander korreliert. Die gemessenen Korrelationsdaten entsprechen den Erwartungen für die verwendeten Targetgeometrien.
Sowohl die Realisierbarkeit des Detektordesigns als auch die Funktionalität des neuartigen Kühlkonzepts konnten erfolgreich bestätigt werden. Beides ebnet den Weg für den Start der Detektorkonstruktion im Jahr 2022.

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Acronyms

ADC analog-to-digital converter

ASIC application-specific integrated circuit

CAD computer-aided design

CFD computational fluid dynamics

CFK carbon-fiber-reinforced polymer

chip DAC chip digital-to-analog converter value

CLFV charged lepton flavor violation

CMBL Compact Muon Beam Line

DAB detector adapter board

DAQ data acquisition

DS downstream

FEB front-end board

FHNW Fachhochschule Nordwestschweiz

flex circuit flexible circuit board

FPGA field-programmable gate array

HDI high-density interconnect

HV high voltage

HV-MAPS high-voltage monolithic active pixel sensors

KF Klein Flansch - ISO standard

L0 Layer 0

L1 Layer 1

L2 Layer 2

L3 Layer 3

LHC Large Hadron Collider

LV low voltage

MAPS monolithic active Pixel sensors

MOSFET metal-oxide-semiconductor field-effect transistor

NMOS n-channel metal-oxide-semiconductor

PCB printed circuit board

PEI polyetherimide

PMOS p-channel metal-oxide-semiconductor

PSI Paul Scherrer Institut

PVC polyvinyl chloride

QC quality control

SciFi Scintillating Fiber

SciTile Scintillating Tile

SES single event sensitivity

SiPM silicon photomultiplier

SM Standard Model

SPI serial peripheral interface

spTAB single point tape-automated bonding

ToT time over threshold

US upstream

Outline of the thesis

The Mu3e vertex detector will be the first particle-physics detector that uses high-voltage monolithic active pixel sensors (HV-MAPS). It is an ultra-thin silicon pixel detector, with a radiation length of only 0.115 % per layer, optimized to reduce scattering of low-energetic electrons and positrons emerging from the muon stopping target. The quoted number accounts for the sensor, the support structures, and the electrical services. With such tight constraints, any cooling system based on liquids or on integrated cooling channels would add a significant amount of material, spoiling the achieved material minimization. Due to the long path length of the particles, even an air-based cooling system would add an equivalent of three tracking layers to the total radiation length. The solution for Mu3e is to use a gaseous helium cooling system, a novelty in particle physics. The corresponding flow channels are confined by the tracking layers themselves, which brings the overall material budget of the Mu3e pixel detector to an unprecedented minimum.

After an introduction to the motivations from theory in chapter 1 and to silicon pixel sensors in chapter 2, the Mu3e experiment is described in chapters 3 and 4.

In the context of this thesis, a detailed characterization is performed for the helium cooling system of the Mu3e vertex detector. For this purpose, detailed mock-ups of the Mu3e vertex detector were constructed, as described in chapter 5. They can be actively heated and are equipped with resistive thermometers. The performance analysis of the helium cooling system is presented in chapter 6.

Furthermore, a first functional vertex detector prototype was constructed and operated under Mu3e-like conditions, including cooling by gaseous helium. The detector construction and its integration into the experiment are both described in chapter 7. In the measurement campaign, called integration run, parts of the Mu3e data acquisition (DAQ) were operated for the first time under realistic conditions. The collected correlation data from the vertex detector is presented and compared to simulation studies in chapter 8.

Contributions from the author

The work presented in this thesis is based on the work of a big collaboration. The contributions from the author to the covered topics are summarized here:

Mock-up construction

The mock-up components and concepts for module construction have been designed prior to the start of this work. The author helped to develop the ladder assembly tool described in appendix A in close collaboration with the mechanical workshop of the Physics Institute in Heidelberg. The construction of both the tape heater and silicon heater mock-ups described in chapter 5, and the associated development of the quality control procedure, were solely done by the author.

Helium cooling studies

The helium cooling plant prototype was designed by Marin Deflorin from Fachhochschule Nordwestschweiz (FHNW). The control software was developed by Frank Meier Aeschbacher from Paul Scherrer Institut (PSI). The author assisted in the construction of the plant. The long-term operation and the measurements exploiting the silicon heater mock-up were all conducted solely by the author. The same applies to the associated data analysis. The presented tape heater cooling studies were performed by Marin Deflorin at the FHNW.

Vertex detector prototype

The author assisted Frank Meier Aeschbacher and Luigi Vigani in the conceptual design of the vertex detector prototype. The testing of detector components was a combined effort of Luigi Vigani and the author. Beside chip bonding, the construction of the detector was conducted solely by the author. The data taking in the integration run measurement campaign was carried out in a collaborative effort with colleagues from the Mu3e collaboration. The data processing was performed by two colleagues from Mainz and the author. The latter analyzed the presented recorded data and conducted simulations.

Part I

Introduction

Muon decays in the Standard Model of particle physics 1

1.1 The Standard Model of particle physics

The Standard Model (SM) of particle physics describes all known elementary particles of our universe and their interactions. It is one of the biggest success stories of modern physics since it provides a detailed description of all current experimental data [1]. It was developed in the 1960's and 70's by unifying electromagnetism and the weak interaction and combining it with the strong interaction and the Higgs mechanism. The establishment of the SM culminated in the discovery of the predicted but until then unobserved Higgs boson in 2012 at the Large Hadron Collider (LHC) [2, 3]. Its discovery was crucial to validate the associated Higgs mechanism, which has been the missing puzzle piece of the SM describing the origin of particle masses.

The building blocks of the SM are quarks, leptons, and bosons (Figure 1.1). Quarks and leptons are spin-1/2 fermions. They are subdivided into three generations. In each generation, there is a quark with an electric charge +2/3 and another one with a charge -1/3. In the leptonic sector, there is a charged lepton with an electric charge -1 and a neutral lepton, the neutrino. The fundamental charged particles of the 1st generation, the up and down quark, and the electron form all known matter surrounding us. The particles of the 2nd and 3rd generations are copies of the 1st generation, differing only in their masses. The mass increases moving to the next generations. All fermions introduced are associated with an antiparticle with opposite quantum numbers.

There are three fundamental forces described by the SM: the electromagnetic, the weak, and the strong force. All of them are mediated by spin-1 gauge bosons. The electromagnetic force is mediated by the massless photon γ, which couples to electric charges. The weak interaction is mediated by massive gauge bosons. The charged $W^{\pm}$ bosons mediate weak charged-current interactions. The electrically neutral Z boson mediates weak neutral-current interactions. Weak interactions couple to the weak isospin, a charge that is carried by all fermions. The last fundamental force, the strong force, is mediated by the massless gluon g. It couples to color charge which is only carried by quarks and gluons.

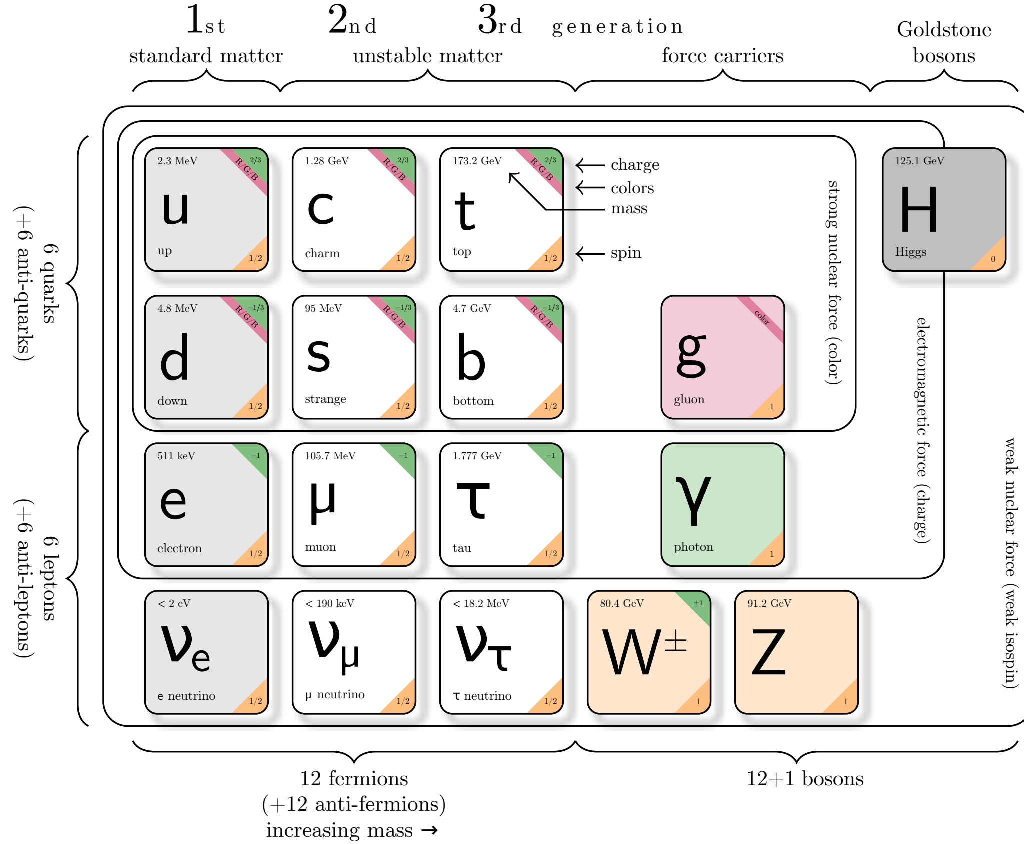


Figure 1.1: The Standard Model of particle physics. Taken from [4]. Based on [5].

In addition, there is the Higgs boson, a spin-0 scalar particle. It is a Goldstone boson that can be regarded as an excitation of the Higgs field, which has a non-zero vacuum expectation value. The interaction of the fermions with this field provides their masses.

1.2 Muon decay

The predictions of the SM regarding interactions and particle properties are tested by a variety of experiments around the world. The Mu3e experiment discussed in this thesis is designed to probe the interactions of the muon to an unprecedented precision. The muon is the charged lepton of the 2nd generation. It has a mass of $(105.658\,374\,5 \pm 0.000\,002\,4)\,\mathrm{MeV}/c^2$ and a lifetime of $(2.196\,981\,1 \pm 0.000\,002\,2)\,\mu\mathrm{s}$ [6]. As a lepton from the 2nd generation, it is assigned with the lepton family number $L_\mu = 1$ (or -1 for μ^+). The lepton family number as well as the lepton number $L = \sum_i L_i = L_e + L_\mu + L_\tau$ are conserved quantities in the SM. The comparably low mass has the consequence that the unstable muon can decay exclusively in electrons, neutrinos, and/or photons. Its main decay channel, referred to as the Michel

decay, is $\mu \to e\bar{\nu}_e\nu_\mu$ with a branching ratio close to 1. The momentum and angular distribution of the positron emerging from a Michel decay is given by the SM to be:

$$\frac{d^2\Gamma}{dx\ d\cos\vartheta} \propto x^2\left((3-2x) - P_\mu \cos\vartheta\,(1-2x)\right) \tag{1.1}$$

with $x = \frac{2E_e}{m_\mu}$ the electron energy fraction to the highest allowed value ($x = 1$ corresponds to $E_e \approx 52.8\,\mathrm{MeV}/c^2$), P_μ the muon polarization, and ϑ the angle between electron momentum and muon spin [6]. The most dominant radiative channel of the muon decay is $\mu \to e\gamma\bar{\nu}_e\nu_\mu$ with a branching ratio of $(1.4 \pm 0.4) \times 10^{-2}$ for $E_\gamma > 10\,\mathrm{MeV}/c^2$ [7]. Another important decay channel is $\mu \to eee\bar{\nu}_e\nu_\mu$ with a branching ratio of $(3.4 \pm 0.4) \times 10^{-5}$ [6]. In all three common muon decay channels, the lepton number L as well as the lepton family number L_μ are conserved.

1.3 Charged lepton flavor violation

An open question in modern particle physics is the presence of so-called charged lepton flavor violation (CLFV). The observation of neutrino mixing [8–10] revealed the existence of lepton flavor violation in the neutrino sector such that the lepton family number is no longer a conserved quantity. CLFV is possible beyond tree-level within the SM when considering neutrino mixing. A corresponding Feynman diagram is depicted in Figure 1.2.

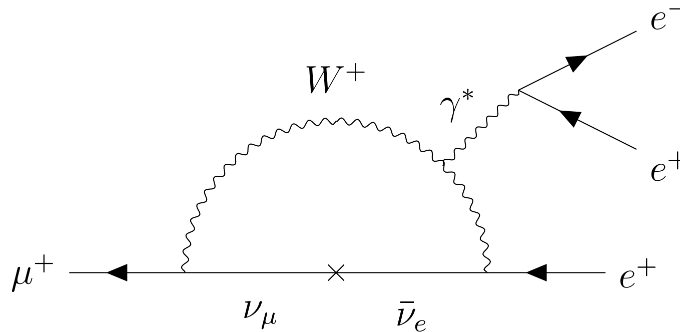


Figure 1.2: The lepton flavor violating muon decay $\mu^+ \to e^+e^-e^+$. This decay is allowed by the SM once the neutrino mixing is taken into account.

The theoretical SM branching ratio for this process, however, is only of the order of 10^{-55} for both, normal and inverted neutrino mass orderings [11, 12]. The current experimental limit for the branching ratio is 1×10^{-12}, set by the SINDRUM collaboration in 1988 [13].

Experimental data suggests that the description of the SM for the leptonic sector is not complete. Recent hints come from b meson decays [14–17] and from deviations of the measured and theoretical value of the anomalous magnetic moment of the muon, as confirmed recently by the g-2 collaboration [18]. This opens the door for

Decay	current limit	future experiment	projected SES
$\mu \to eee$	1.0×10^{-12} [13]	Mu3e (phase I) [22]	2×10^{-15}
		Mu3e (phase II) [22]	$\leq 1 \times 10^{-16}$
$\mu \to e\gamma$	4.2×10^{-13} [23]	MEG-II [19]	6×10^{-14}
$\mu N \to eN$	7.0×10^{-13} [24]	COMET (phase II) [20]	2.6×10^{-17}
		Mu2e [21]	3×10^{-17}

Table 1.1: Current limits and projected SES for future lepton flavor violation experiments with muon decays.

potential physics beyond the SM, and makes precision measurements of rare muon decays highly relevant in particle physics.

The Mu3e experiment aims to exploit branching ratios for $\mu^+ \to e^+e^-e^+$ down to a single event sensitivity (SES) of 1×10^{-16} in the final phase, improving the current limit by four orders of magnitude. Complementary searches like MEG-II [19], COMET [20], and Mu2e [21] are expected to lower limits for the decay $\mu \to e\gamma$ or the conversion of muonic atoms $\mu N \to eN$ to similar levels in the next decade, as summarized in Table 1.1. Any observation of one of these decays would be a clear indication for physics beyond the SM. No observation of any decay, however, will put large constraints on the allowed phase space for theories beyond the SM.

Silicon tracking detectors 2

Tracking is nowadays a standard technique to reconstruct particle trajectories in high-energy experiments. The trajectory of a particle is reconstructed by measuring several points in space. This way, the track parameters can be extracted, which provide information about the origin and the path of the particle. Within a magnetic field, the particle momentum is accessible by measuring the curvature of the particle track. Using a granulated detector, the points of a track are precisely identified. Silicon detectors can be micro-structured and offer spatial resolutions of a few micrometers. Combined with fast readout electronics, they represent one of the most widely-used detector technologies.

Tracking the charged decay products of muon decays is the basis of the Mu3e experiment as outlined in chapter 3. The focus of this chapter is to introduce the concept of particle detection with silicon detectors and the relevant physics processes to understand the design and technological choices made for the experiment described in part II.

The signal generation in silicon detectors is described, starting with the interaction of charged particles in matter and magnetic fields, followed by the main working principles of signal detection in semiconductors, based on [6, 25]. There are many types of silicon detectors optimized for specific applications. This work focuses on pixelated sensors, which offer the highest granularity and thus enhanced precision. The conventional approach of hybrid pixel sensors is discussed, where sensors and readout chips are separated. Later, monolithic sensor technologies are introduced, which combine sensor and readout in one entity. The chapter concludes with the HV-MAPS technology that will be used in the Mu3e experiment.

2.1 Particle interaction with matter

The basis of particle detection is the interaction of particles with the detector material. In the search for $\mu^+ \to e^+e^-e^+$ low-energetic positrons and electrons are to measure. Thus, this section covers the energy deposition caused by charged particles and the associated scattering, which defines the tracking resolution at low momenta.

Charged particles traversing matter deposit energy in the medium primarily by four effects: ionization, bremsstrahlung, Cherenkov radiation, and transition radi-

ation. The amount of energy deposited in the medium is mainly determined by ionization and bremsstrahlung. Thus, they are the relevant phenomena for particle detection with silicon detectors. Cherenkov and transition radiation deposit only a small fraction compared to the former. In general, they are used primarily for particle identification and not for tracking applications.

The interaction of particles with the medium opens the possibility to detect them. The downside is that it is accompanied by scattering, which distorts the trajectory of the particle tracks. Both the energy deposition and scattering are described in the following sections.

2.1.1 Energy deposition

The energy deposition of a particle is a stochastic process. Along the path x through a medium, the number of interactions and their strength can vary in a wide range. The average energy loss for heavy charged particles is described by the Bethe formula [26]. For the energy deposition by electrons and positrons, one has to consider the low mass of the particles and the indistinguishability of incident particles and the electrons of the medium. The corrections applied result in the Berger-Seltzer formula [27]:

$$-\left\langle \frac{dE}{dx} \right\rangle = \rho \, \frac{0.153536}{\beta^2} \, \frac{Z}{A} \cdot \left(B_0(T) - 2 \ln \frac{I}{m_e c^2} - \delta \right) \tag{2.1}$$

with ρ the material density, Z and A the atomic and mass numbers, I the mean excitation energy, and δ the density-effect corrections of the material. $\beta(= v/c)$ describes the particle velocity, m_e its mass. $B_0(T)$ is the stopping power for a specific kinetic energy T given in [27] for positrons and electrons separately. The mean energy loss in silicon is displayed in Figure 2.1.

The Berger-Seltzer formula in equation 2.1 overestimates the energy deposition for thin detectors [6]. More precisely, the energy loss-probability function is described by the highly-skewed Landau distribution. It has a long tail toward high-energy transfer. The most probable energy deposition, which corresponds to the peak of the distribution, depends then on the thickness of the detection layer, as shown in Figure 2.2a.

The contributions of ionization and bremsstrahlung to the energy loss depend on the particle velocity and the medium. In Figure 2.3, the fractional energy loss for different processes is shown for lead. The crossing point of ionization and bremsstrahlung is referred to as the critical energy E_c. For particle energies higher than the critical energy, bremsstrahlung dominates the average energy loss. In silicon, $E_c \approx 40\,\mathrm{MeV}/c^2$ for electrons and positrons [29]. Thus, with a maximum energy of around $53\,\mathrm{MeV}/c^2$, the decay products from muons decaying at rest are in the regime where ionization has a significant contribution.

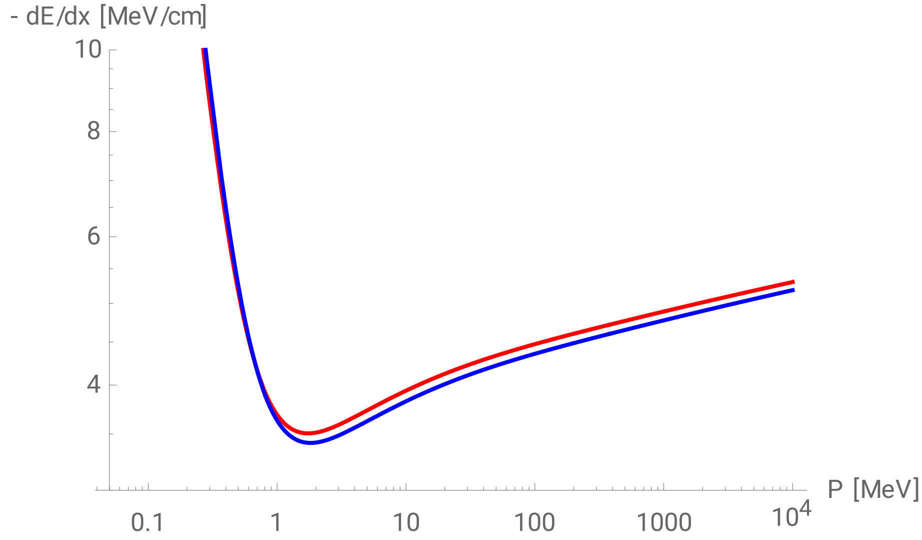
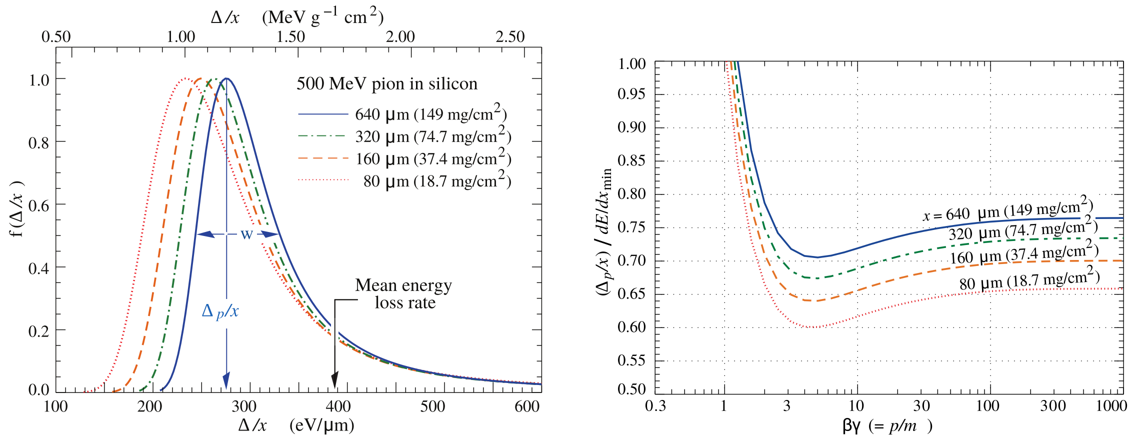


Figure 2.1: Mean energy loss of electrons (red) and positrons (blue) in silicon. From [28] based on values from [27].



(a) Straggling functions normalized to unity at the most probable value [6].

(b) Most probable energy loss, scaled to the mean loss of a minimum ionizing particle [6].

Figure 2.2: The energy loss of 500 MeV pions in thin silicon detectors.

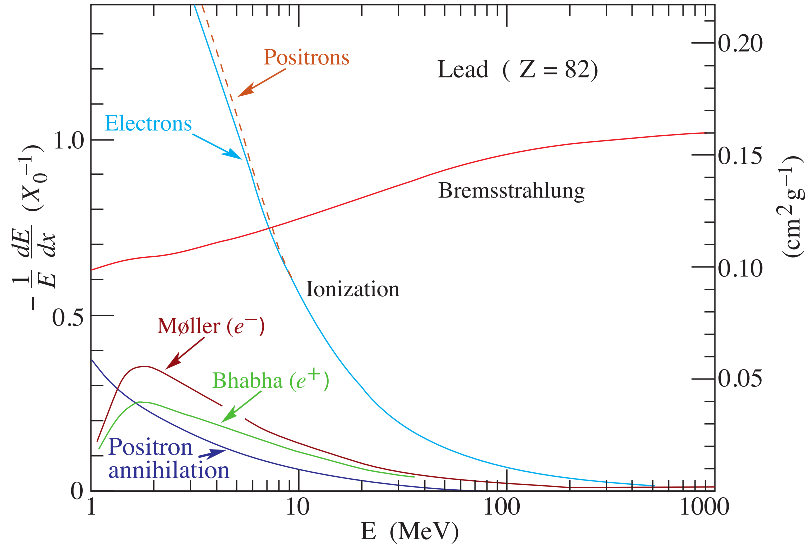


Figure 2.3: Fractional energy loss per radiation length X_0 for electrons in positrons in lead [6].

In high-energy physics, it is conventional to quantify material budget[1] by the radiation length X_0. It is defined by the average distance an electron travels in the medium before it is left with a fraction of its initial energy corresponding to 1/e because of bremsstrahlung. In more formal terms:

$$-\frac{dE}{dx} = -\frac{E}{X_0} \tag{2.2}$$

The radiation length can be numerically calculated by the approximation given in [25]:

$$\rho X_0 = \frac{716.408\,[\mathrm{g/cm^2}] \cdot A}{Z(Z+1)\ln\dfrac{287}{\sqrt{Z}}} \tag{2.3}$$

A high radiation length is required, when the influence of the detector on the particle energy and momentum needs to be minimized. This is obtained for materials with a low density ρ and a low atomic number Z.

2.1.2 Scattering

While traversing a medium, a particle is scattered multiple times under small angles. These interactions, resulting from Coulomb scattering with the nuclei of the medium, sum up to an average net scattering angle. This process is illustrated in

[1]Material budget refers to a weighted quantity that describes the detector thickness in units of the radiation length.

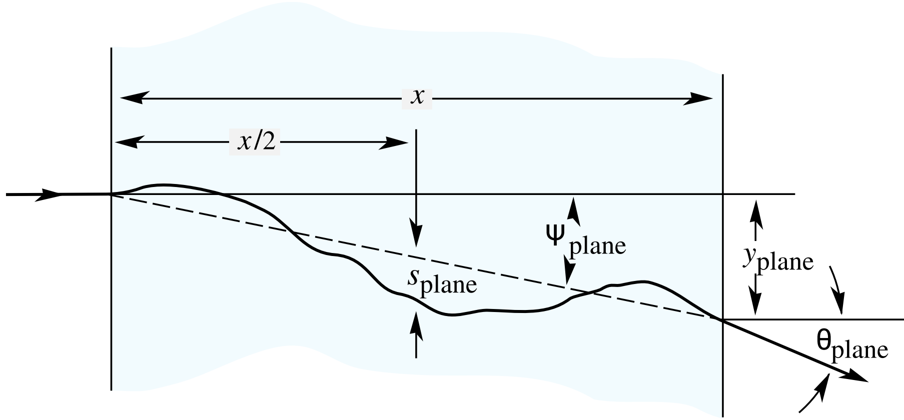


Figure 2.4: Sketch of the distortion of a particle track due to multiple-Coulomb scattering [6].

Figure 2.4. The rms width θ of the net angle is quantitatively described by the Molière theory [30]:

$$\theta = \frac{13.6\,\mathrm{MeV}}{\beta c p}\, z \sqrt{\frac{x}{X_0}} \left(1 + 0.038 \ln \frac{x z^2}{X_0 \beta^2}\right) \tag{2.4}$$

with β, p, and z the particle velocity, momentum, and charge number. x describes the path length through the medium and X_0 the previously introduced radiation length of the medium. The effect of scattering decreases for high-momentum particles and light materials with large radiation lengths. To minimize the distortion of particle tracks, thin detectors with large X_0 are favorable.

2.2 Particle tracks in magnetic fields

In the presence of a magnetic field, the Lorentz force acts on the moving charged particles. When the tracking detectors are placed inside a magnetic field, the bending radius of the particle trajectory can be measured. As an example, the bending of two positively and one negatively charged particle tracks is sketched in Figure 2.5. The bending radius in the plane transverse to the magnetic field is given by:

$$R = \frac{p_T}{0.3\ z\ B} \tag{2.5}$$

with B the magnetic field in Tesla, p_T the transverse momentum in GeV/c, z the charge number of the particle, and R the radius in meter [25]. The particle momentum p is obtained by measuring the bending radius and the inclination angle ϑ in the longitudinal plane (Figure 2.5):

$$p = \frac{p_T}{\sin \vartheta} \tag{2.6}$$

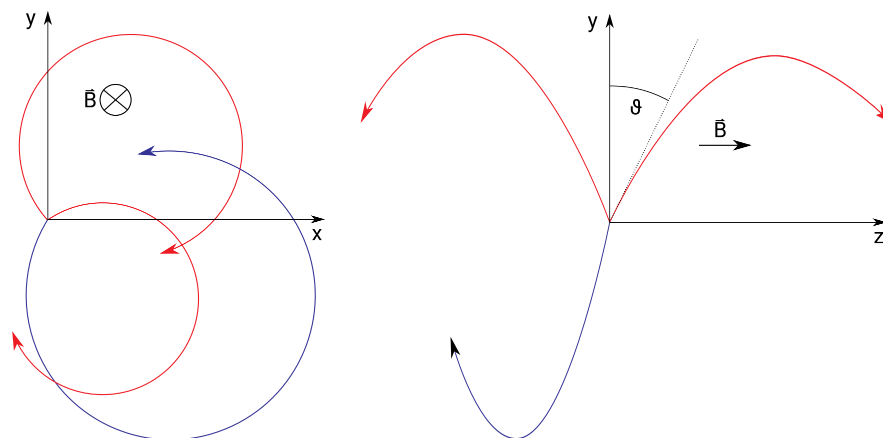


Figure 2.5: Particle tracks in a magnetic field in the transverse and longitudinal plane. Red tracks illustrate positively charged particles and the blue track the negative one. The inclination angle ϑ is shown for one particle.

For a known particle species, the energy can be determined directly from its momentum. This enables to study the kinematics of a decay since energy and momentum are conserved in every physics process.

2.3 Semiconductors as particle detectors

This section describes the basic working principles of semiconductors used as particle detectors. The pn-junction is introduced, which forms the basis of silicon detectors. The detection of the deposited energy by a traversing particle is outlined and the implementation of electrical circuitry using transistors is briefly described.

2.3.1 PN-junction

All materials are classified on the basis of their electrical properties as conductors, semiconductors, and insulators. Semiconductors have a small band gap between their valence and conduction band, the two bands closest to the Fermi level. This band gap is small enough for thermal excitations to lift electrons into the conduction band, filling the valence band with holes. The most common semiconductor in most applications, including particle physics, is silicon.

Solid silicon forms a crystalline structure. As an element of the carbon group, it comes with four valence electrons. For particle detection, a silicon substrate is doped to generate a pn-junction. Atoms of the boron group are implanted for p-doping. They are incorporated into the crystalline structure and create an additional hole in the valence band because atoms of the boron group come naturally only with three valence electrons. Similarly, atoms of the nitrogen family are implanted for

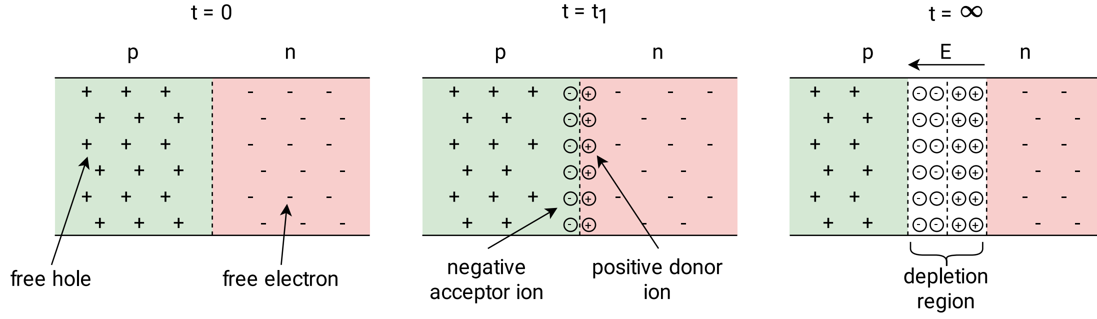


Figure 2.6: Sketch of a pn-junction. Free-charge carriers move toward the interface at $t = t_1$, where they recombine creating a depletion zone. The immobile ionized atoms create an electric field E. At $t = \infty$, the pn-junction is in equilibrium. Taken from [31]. Based on [32].

n-doping. With five valence electrons, only four are bound to the surrounding silicon atoms in the crystal bond structure, leaving a free electron.

A pn-junction is formed by bringing a p-doped and an n-doped substrate into contact. Such a junction is also referred to as a diode. The free electrons diffuse from n-doped to the p-doped material, while holes diffuse into the n-doped material. The charge carriers recombine at the interface, leaving behind an area without free-charge carriers, the *depletion zone*, as illustrated in Figure 2.6. The resulting charge displacement creates an electric field within the substrate.

The width of the depletion zone d and the intrinsic potential U_{bi} between the n-doped and p-doped sides of the diode are given by the doping concentrations N_A and N_D and the resulting charge carrier density n_i. The potential U_{bi} for silicon is typically given by:

$$U_{bi} = \frac{k_B T}{e} \ln \frac{N_A N_D}{n_i^2} \approx 0.6 - 0.8\,\mathrm{V} \tag{2.7}$$

with k_B the Boltzmann constant, e the elementary charge, and T the temperature [25]. In particle detectors, usually, a pn-junction is formed by either a p- or n-doped substrate and a thin n- or p-doped layer, which forms the charge-collection electrode. The substrate is typically used as the depleted volume having a lower doping concentration. The depletion width is then given as:

$$d \approx \sqrt{\frac{2\epsilon\epsilon_0}{e}\, U_{bi}\, \frac{1}{N_{substrate}}} \tag{2.8}$$

with ϵ and ϵ_0 the dielectric constant of silicon and vacuum [25]. By applying an additional external voltage U_{ext}, the width of the depletion zone can be changed. Applying the higher potential to the n-doped part, reverse bias, expands the depletion zone as sketched in Figure 2.7.

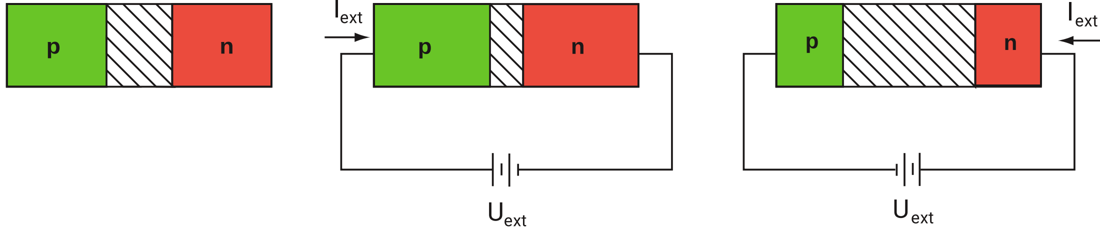


Figure 2.7: The depletion zone of a pn-junction changing under an externally applied voltage U_{ext}. Left: no bias, middle: forward bias, and right: reverse bias. Based on [25].

2.3.2 Charge detection and readout

The energy deposited along its path by traversing particles excites electrons and lifts them into the valence band. This creates electron-hole pairs in the silicon. When generated in the depletion zone, electrons and holes drift in opposite directions in the electric field. If generated outside the depletion zone, they thermally diffuse until they recombine or eventually reach the depletion zone. Moving charges induce mirror charges at the electrodes. The resulting signal pulse at the electrode is amplified and read out.

The amplifier and the readout are realized by transistor logic. It is commonly realized as metal-oxide-semiconductor field-effect transistor (MOSFET). There are two basic implementations, the p-channel metal-oxide-semiconductor (PMOS) and the n-channel metal-oxide-semiconductor (NMOS) transistors, which are sketched in Figure 2.8. A PMOS transistor is realized with p-doped implants on an n-doped substrate, and NMOS transistors with n-doped implants on a p-doped substrate. Each transistor comes with four connections: source, gate, drain, and bulk (or just S, G, D, and B). The S and D are the implants, B is an implant directly connected to the substrate, and G is a metal-oxide connector between S and D.

The operation of a MOSFET is determined by the voltage applied between the different connections. The voltage U_{GS} between G and S controls if current can flow through the transistor between D and S (drain-source current). The voltage U_{DS} between D and S defines if the transistor is operated in linear or in saturation mode. In linear mode, the drain-source current increases linearly with U_{DS}. In saturation mode, the transistor can be considered as a current source that depends on U_{GS}.

The amplification and readout of the signal is either implemented in a separate readout chip that is connected to the sensor chip, or it is integrated in the same substrate, where the particles are detected. Both realizations are described for silicon pixel sensors in the next section.

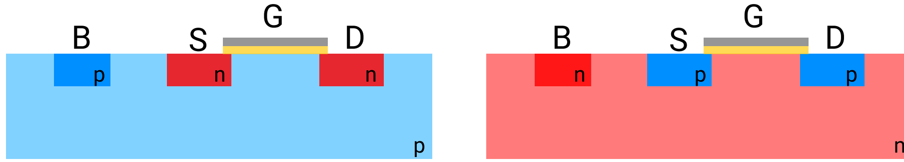


Figure 2.8: MOSFET transistors. Left: NMOS, right: PMOS [28].

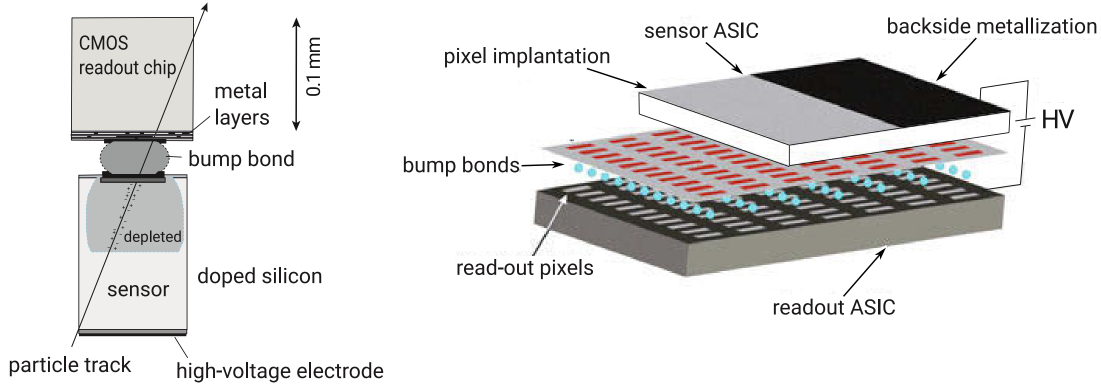


Figure 2.9: Sketch of hybrid pixel detectors. Left: structure of an individual pixel cell. Right: hybrid pixel matrix made of a sensor and a readout ASIC. Based on [25].

2.4 Pixel detectors

One of the advantages of silicon detectors is that they can be etched in small independent units. Pixel detectors are structured in 2D pixel arrays and allow to associate each detected particle with a confined position information. Only microstrip detectors can compete in terms of spatial resolution [33, 34] but they are more prone to ambiguities. Typical pixel sizes of $100\,\mu\text{m} \times 100\,\mu\text{m}$ and less are possible [35]. In high-rate experiments like Mu3e or at the LHC, a low occupancy per readout channel is required, which is realized by such a high granularity.

In the following sections, hybrid and monolithic pixel sensors are introduced. Their applicability in high-rate environments, which in addition have strong constraints on the radiation length, is discussed. It is concluded by presenting HV-MAPS that combine low material budget with fast readout electronics.

2.4.1 Hybrid pixel sensors

Hybrid pixel sensors are composed of two application-specific integrated circuits (ASICs). The sensor ASIC is detecting the traversing particles and generates the associated signals. Each pixel cell is electrically connected via bump bonds (Figure 2.9) to an associated cell in the readout ASIC. The amplification and readout of the data is fully realized on this chip.

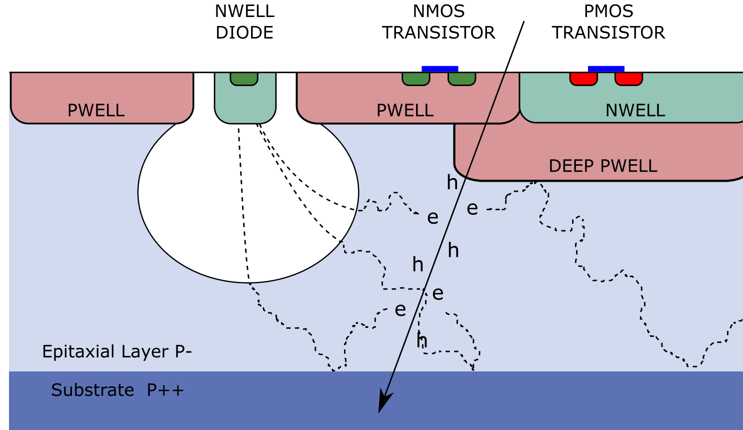


Figure 2.10: Schematic cross section of the ALICE ALPIDE MAPS [39].

The upside of such a modular design is that both ASICs can be developed separately. The downside is that the fabrication is highly complex. This includes the bump bonding and that the sensor ASIC has to be usually processed on both sides.

For an experimental design, where multiple-Coulomb scattering is the main contribution to the track resolution, hybrid sensors are disfavored because of their high material budget. Hybrid designs in the ATLAS and the CMS experiments, typically contribute to around 3 % X_0 per detector layer including all services. The share of silicon is around 0.5 % X_0 [35, 36]. Considering that a single 100 µm thin silicon substrate has only ~ 0.1 % X_0 [29], a monolithic sensor with integrated readout circuitry inside the sensitive bulk is favorable when material minimization is required.

2.4.2 Monolithic Pixel sensors

In the recent past, monolithic active Pixel sensors (MAPS) entered high-energy physics as tracking devices in the STAR and the ALICE experiments [37, 38]. MAPS integrate particle detection, signal processing, and readout in one entity. They are based on commercial CMOS processes, which makes them a low-cost alternative.

In Figure 2.10, a schematic cross section of the ALPIDE design used in ALICE is shown [38]. The on-chip circuitry is realized by a deep p-well in a p-doped epitaxial layer. The p-well allows to integrate NMOS transistors while the epitaxial layer serves as detection volume. Charges generated in this layer diffuse until they eventually reach the depleted area at the diode.

The sensors can be thinned to $\leq$50 µm, an unsurpassed material budget for pixel detectors in high-energy physics. The downside of conventional MAPS is the slow charge collection via diffusion. High-rate applications like the Mu3e experiment require a time resolution in the order of $\mathcal{O}(10\,\text{ns})$ or less, which can only be realized with charge collection by drift. A MAPS-based design with superior time resolution is described in the next section.

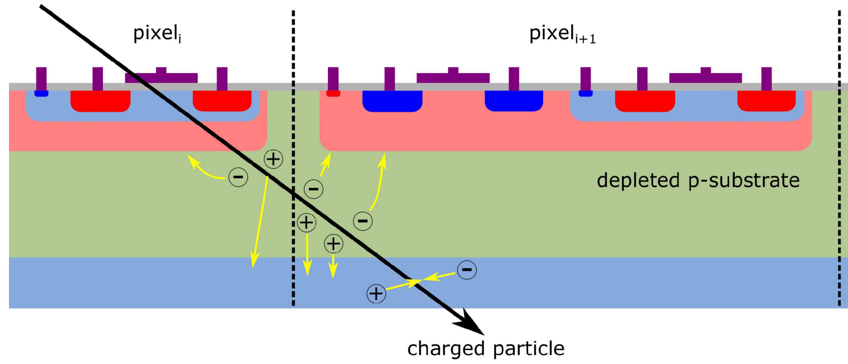


Figure 2.11: Schematic cross section of an HV-MAPS. The electrons are collected by the collecting electrode, the deep n-well (pink-colored) [42].

2.4.3 High-voltage monolithic pixel sensors (HV-MAPS)

HV-MAPS [40] is a monolithic sensor technology with an optimized time resolution. It is based on a deep n-well in a p-substrate (Figure 2.11). This way, the embedded PMOS logic in the pixel cell is shielded against the substrate potential. The deep n-well itself is used as a diode. A high voltage is applied to the substrate such that a depletion zone is formed around the whole n-well. This increases the depleted volume compared to conventional MAPS and enables fast charge collection via drift [41].

The HV-MAPS used in the course of this thesis are realized in the commercial 180 nm HV-CMOS process in comparably low ohmic substrates (20-200 Ω cm). This provides a depletion zone of a few tens of micrometers, which combines efficient charge detection with a good time resolution. Like for MAPS, the thickness can be reduced to $\leq$50 µm, which allows minimal material budget [43].

It is the technology of choice for the Mu3e tracking detectors, since it combines a good time resolution of a few nanoseconds with minimal material budget [44]. This is crucial for the design of Mu3e, as outlined in the next chapter. The concrete sensor realization for Mu3e is presented in chapter 4.

Part II

The Mu3e experiment

The conceptual experimental design 3

Mu3e [44] is an experiment that aims to measure the rare muon decay $\mu^+ \to e^+e^-e^+$ down to a SES of 2×10^{-15} in phase I. To reach such a high sensitivity, background processes mimicking the signal have to be suppressed below the signal level. This can only be achieved by a clever detector design and the use of novel detector technologies. Mu3e strikes several new paths that all aim to minimize material in the acceptance region.

In this chapter, the experimental challenges like low material budget and background sources of concern are outlined. The concepts for background suppression are discussed. Finally, the technological solutions regarding the detector design are presented focusing on the silicon tracking detectors with an emphasis on the cooling system. The resulting structure and realization of the Mu3e detectors is then described in chapter 4.

3.1 Experimental challenges

The experimental challenges to address in Mu3e are manifold. There are low-energetic particles to detect at high rates. Background processes have to be taken into account to not spoil the sensitivity of the experiment. The key challenges are listed and discussed in the following.

3.1.1 Low-energetic particles

Mu3e is an experiment at the high-intensity frontier. It requires a high-rate muon beam to reach the aimed sensitivity. Currently, the most intense continuous muon beam is provided at PSI with muon rates of the order of $10^8\,\mu^+/\mathrm{s}$ [45, 46]. These high rates are accessible by impinging a powerful proton beam on a target. A certain fraction of the resulting pions decay at the target surface at rest. This produces a mono-energetic continuous muon beam with a momentum of 28 MeV/c. The muon beam is directed by a beam line toward a stopping target, where the muons decay at rest. Thus, the decay products have a maximum energy of only $m_\mu/2 \approx 53\,\mathrm{MeV}/c^2$. This poses a natural challenge for tracking, since the interaction

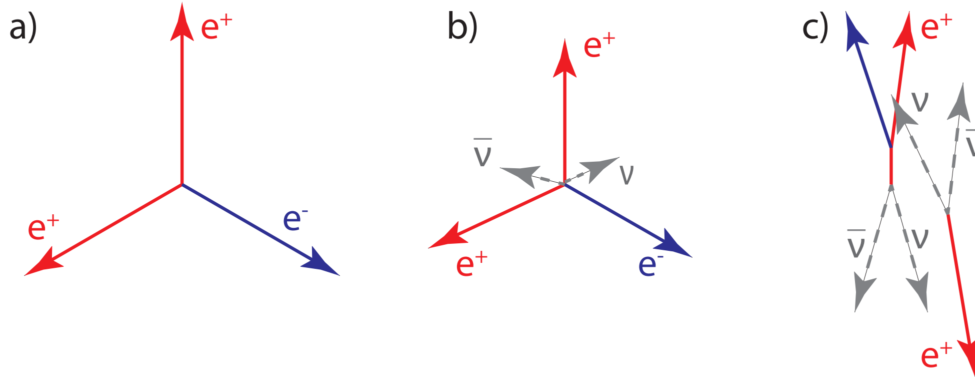


Figure 3.1: Topologies for a) the signal decay $\mu^+ \rightarrow e^+e^-e^+$, b) the internal conversion decay and c) combinatorial background from two Michel decays with a Bhabha scattering [22].

with material distorts the measurement, particularly for low-energetic particles such as the positrons and electrons emerging from the muon decays.

3.1.2 Signal to background discrimination

The reconstruction of the $\mu^+ \rightarrow e^+e^-e^+$ decay is in principle straight-forward. One needs to find three charged particle tracks originating from a single vertex in time coincidence. The reconstructed energy has to match the rest mass of the muon. The particle tracks are detected by silicon pixel detectors. The momentum of the particles is measured by the curvature of the track within a homogeneous magnetic field.

Background processes, however, can mimic the signal topology as illustrated in Figure 3.1. In Mu3e, one distinguishes between combinatorial and irreducible background. In a high-rate environment, ambiguities can be created by the sheer mass of particles emerging from the stopping target, causing combinatorial background. Rare muon decays with three charged particles in the final state cause irreducible background that has to be discriminated by kinematics.

Combinatorial background

The combinatorial background is mainly caused by the presence of electrons. One example is illustrated in Figure 3.1 (c). Two Michel decays close in time and space generate two positrons. When one positron undergoes Bhabha scattering within the target, the decay topology is recreated. Similar topologies can be obtained for pair production from photons. Another background is the misinterpretation of the particle charge for full-circle positron tracks.

The combinatorial background is tightly constrained for superior vertex and time resolution and for a high resolution on the reconstructed muon mass. The vertex

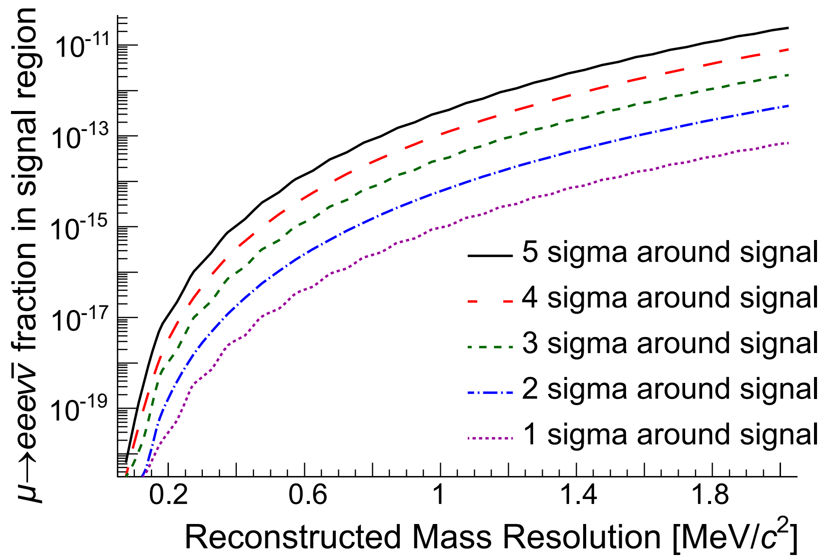


Figure 3.2: Contamination of the signal region with internal conversion events as a function of momentum sum resolution [22].

resolution is limited by multiple-Coulomb scattering, particularly for the target and the first tracking layer. The time resolution has to be sufficient to suppress ambiguities and to ensure a proper time-of-flight measurement for charge identification. This means that the material for the tracking layers and the target have to be at the possible minimum. The required time resolution is $<$500 ps to distinguish the charge of the decay products by time-of-flight, and $<$100 ps to eliminate ambiguities from non-synchronous muon decays [22].

Irreducible background

The radiative muon decay with internal conversion of the photon to an electron-positron pair, $\mu \rightarrow eee\bar{\nu}_e\nu_\mu$, produces the same decay signature as $\mu^+ \rightarrow e^+e^-e^+$ (Figure 3.1 (b)). It is considered as the most critical background source for the experiment. The neutrinos carry away a fraction of the energy, which means the background can be discriminated by kinematics. For this, a superior momentum resolution is necessary. In Figure 3.2, the contamination of the signal region with internal conversion decays is shown. For the aimed SES of 2×10^{-15}, the resolution of the reconstructed mass has to be better than $1\,\mathrm{MeV}/c^2$. This can be only achieved by sufficient momentum resolution of the charged particle tracks. In the low-energy regime, the momentum resolution is dominated by multiple-Coulomb scattering (Figure 3.4a). Thus, the material has to be at a minimum not only for the active detector, but also for the passive components.

3.2 Tracking

The tracking detector of Mu3e has to combine low material budget with excellent timing performance and a high efficiency. The sensors require to fulfill a time resolution of ≤20 ns, a spatial resolution of ≤30 µm, a detection efficiency of ≥99 %, and a thickness of ≤50 µm to reduce the background described above. In addition, the sensor has to be capable of processing hit rates of around 5 MHz. [22]

The thickness restricts the sensor design to monolithic technologies. The severe performance requirements concerning bandwidth and time resolution rule out current MAPS like the ALPIDE chip [38]. For Mu3e, a dedicated sensor R&D led to the development of a specific HV-MAPS sensor, the MuPix, which is described in chapter 4.3.1.

The minimization of material is reflected also in the number of tracking layers. Only four pixel layers surround the target region. A conceptual sketch of the experimental design is shown in Figure 3.3. A pair of two inner layers at small radii forms the vertex detector. Another pair at larger radii forms the outer layers. The momentum resolution is increased by detecting the particles twice with the outer layers. The charged particle tracks bend in the magnetic field such that they recurl and hit the outer layers again. This way, the lever arm for the momentum measurement increases and six hits (or more for the most central region) are accessible for track reconstruction. To increase the acceptance for recurlers, two stations are added upstream (US) and downstream (DS).

This design further reduces the effect of multiple-Coulomb scattering in the outer layers as sketched in Figure 3.4b. For a half-turn made by recurling tracks, the effect of scattering cancels to a first order . This statement only holds when scattering can be neglected within the half-turn, which requires either a low density gas or vacuum. The required time resolution to eliminate combinatorial background is reached by a pair of timing detectors. In the central station, there is the low-material Scintillating Fiber (SciFi) detector placed between the tracking layers. Inside the outer layers in the recurl stations, there is the Scintillating Tile (SciTile) detector.

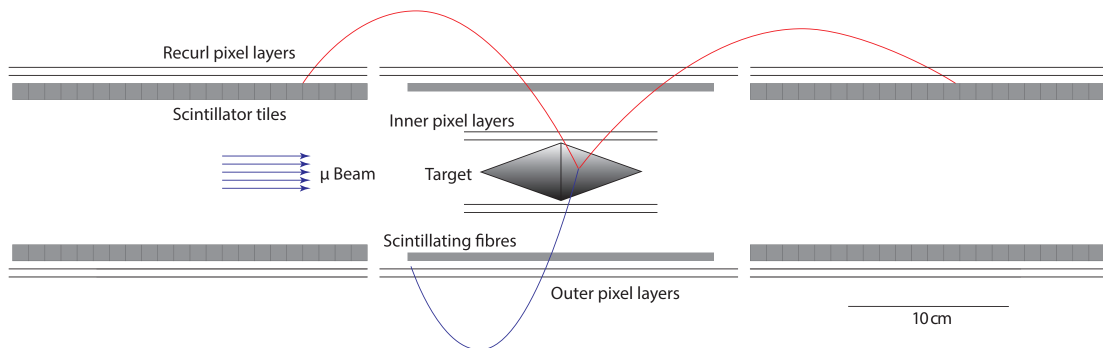
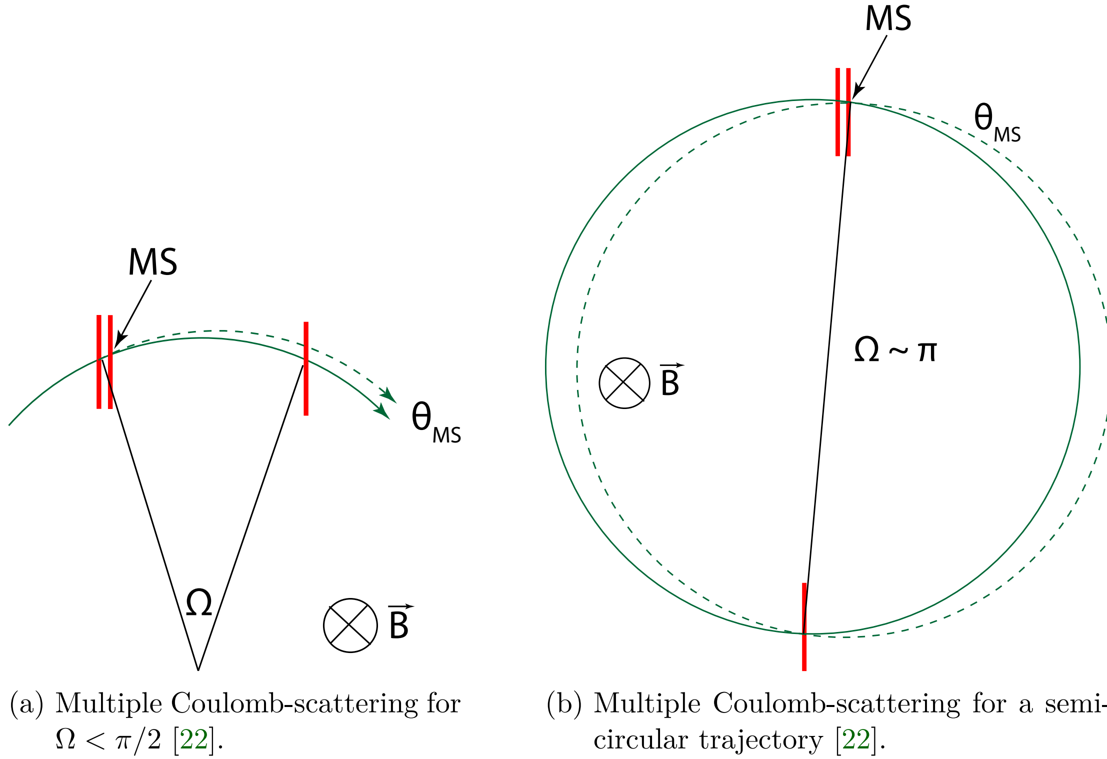


Figure 3.3: Schematic view of the Mu3e experiment, cut along the beam axis in the phase I configuration [22].



(a) Multiple Coulomb-scattering for $\Omega < \pi/2$ [22].

(b) Multiple Coulomb-scattering for a semi-circular trajectory [22].

Figure 3.4: Multiple Coulomb-scattering as seen in the plane transverse to the magnetic field direction. Comparison of a given angle $\Omega < \pi/2$ and a semi-circular trajectory. The red lines indicate the measurement planes.

The design for the powering and readout of the pixel sensors is also driven by the minimization of the material budget. Flexible circuit boards (flex circuits) providing both power and readout lines are realized as multi-layered aluminum-polyimide laminates. An aluminum circuit is preferred against conventional copper because of its higher radiation length. The technology was established e.g. in the ALICE silicon strip detector [47]. The aluminum traces are directly connected via single point tape-automated bonding (spTAB), which does not require any additional material to establish the connection. The soft aluminum traces are ultrasonically bonded to the bond pads through cutouts in the polyimide layers.

The flex circuits serve as intrinsic support structure of the tracking layers such that no additional material is added. Such a pixel ladder, consisting of chips, power and readout circuitry, and adhesives, has a resulting material budget of only $0.115\,\%\ X_0$ [22] with no cooling structure implemented.

3.3 Detector cooling

Every active detector technology dissipates a certain amount of heat. To keep the detector at a temperature where stable operation can be assured, the pixel sensors of

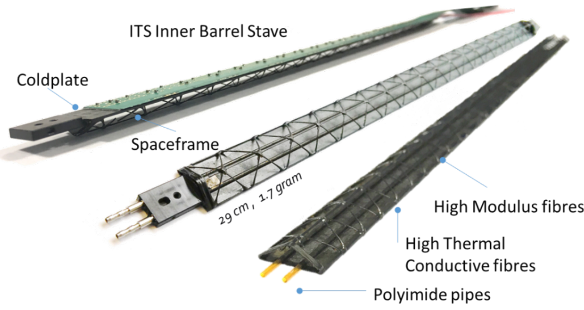
the tracking detector have to be cooled. The conventional approach is a pipe system providing a liquid coolant to the readout electronics. The cooling circuit is thermally coupled to the heat source and carries the heat away. Additional material inside the acceptance region, e.g. in form of a cooling plate to thermally couple the sensors to a cooling circuit, would counteract the material minimization. The same holds for an integrated cooling circuit on the sensor or its support. A massless cooling concept relying on heat radiation only, however, leads to chip temperatures of >140 °C, without considering any surrounding material.[1] This underlines the necessity of active detector cooling. State-of-the-art pixel cooling systems like microchannel CO_2 cooling, ultra-thin water cooling, and gaseous cooling are described and their applicability for Mu3e is evaluated. It is followed by the description of the cooling concept of Mu3e.

Evaporative CO_2 and water cooling

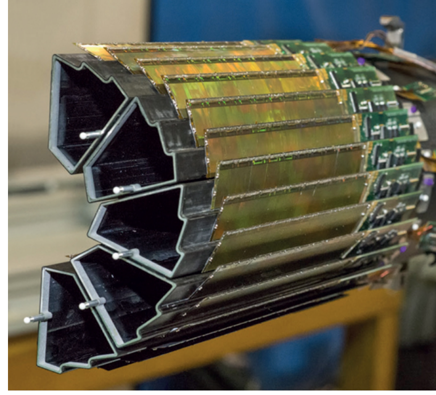
Evaporative CO_2 cooling has been a game changer in recent particle physics experiments. It was first realized for the LHCb VELO detector [49] and the AMS TTCS [50], and combines excellent cooling power with a radiation hard and non-toxic coolant. In the first application, the cooling pipes have been thermally coupled to the readout chip by cooling plates. The sensor chip itself has no integrated readout circuitry and is only conductively cooled being bonded to the readout chip. Recent developments, like the LHCb VELO upgrade, use microchannels to provide the CO_2 directly to the silicon substrate [51]. The coolant channels are etched into a silicon wafer, which is soldered to the readout chip. The downside of such a scheme is that the required silicon thickness is a few 100 µm. This would at least double the material budget of the sensors in Mu3e without yet considering the pressurized CO_2.

An alternative approach is the ultra-thin water cooling system used by the ALICE ITS upgrade [39]. As for Mu3e, monolithic chips are used but with a heat dissipation of only around 40 mW/cm^2 [38]. The 50 µm thin sensors are also electrically connected with aluminum-polyimide flex circuits. The cooling circuit is integrated into the sensor staves (Figure 3.5a). It is made of polyimide tubes with a diameter of 1 mm and a wall thickness of 25 µm filled with water. The thermal coupling is provided by carbon foam, which partially serves as a support structure as well. The average radiation length added by the cooling structure is only 0.1 % X_0 for the inner barrel staves. It is not distributed uniformly and peaks at the water tubes at around 0.5 % X_0. Despite being aggressive in material reduction, it would still double the material budget of a MuPix ladder.

[1] Stefan-Boltzmann law: $T = \sqrt[4]{P/A\sigma}$ with P = 350 mW/cm^2, A $\approx 2 \cdot (20.66 \times 23.18\,\mathrm{mm}^2)$ the chip surface and σ the Stefan–Boltzmann constant [48].



(a) Inner stave of the ALICE ITS [52].



(b) 2nd layer of STAR PXL on carbon fiber support [53].

Figure 3.5: Pixel detector cooling concepts with reduced material budget. (a) Water cooling system of ALICE ITS, (b) gaseous cooling system of STAR PXL.

Gaseous cooling

The most radical approach to minimize material is to use gaseous cooling. This concept has been successfully demonstrated by the STAR PXL detector [54]. The monolithic sensors, with a heat dissipation of around 150 mW/cm^2, are cooled by an airstream. The air is guided through carbon channels that serve also as support and as thermal coupling to the sensors (Figure 3.5b). The velocity of the air is around 10 m/s to provide sufficient cooling power. In this implementation, the carbon fiber supports add 0.193 %/X_0 of material which is even more than for the water cooling system described above. In turn, the material is distributed uniformly and the question arises if structured channels are needed at all. In case of a global air flow without additional support, the material budget of the cooling system would be entirely negligible.

Mu3e helium cooling

Gaseous cooling without supported channels is the approach that is followed by Mu3e. A gas flow between the tracking layers of the vertex detector and the outer layers is foreseen. In addition, a global flow around the outer layers is implemented. Comparing the radiation length of air to the detector material, scattering with the gas inside the detector volume can be neglected. The picture changes, however, if going to the recurling tracks. With an approximate track length of 1 m, the resulting radiation length of air is 0.33 % X_0, an equivalent to three additional tracking layers. Thus, the cancellation of multiple scattering described above for recurling tracks does not hold for air. The aimed sensitivity can not be reached. Therefore, the tracking concept for Mu3e can only be realized with gases lighter than air. An overview of the radiation lengths and relevant parameters regarding cooling is given for a selection of such gases. Both hydrogen and helium combine

	Air	N_2	Ne	He	H_2	unit
ρ	1.29	1.25	0.90	0.18	0.09	kg/m^3
X_0	3.0×10^4	3.3×10^4	3.5×10^4	5.7×10^5	7.5×10^5	cm
X/X_0	0.33	0.30	0.29	0.018	0.013	% (for X = 1 m)
λ	0.241	0.24	0.46	1.43	1.71	mW/(cm·K)
C_p	1.01	1.04	1.03	5.23	14.32	kJ/(kg·K)
s	1.30	1.30	0.93	0.94	1.29	$kJ/(m^3 \cdot K)$

Table 3.1: Radiation length X_0 and thermal properties of selected gases lighter than air [55, 56]. ρ is the gas density at 0 °C at ambient pressure. λ is the thermal conductivity given at 0 °C. C_p is the specific heat capacity at 20 °C. $s = \rho \cdot C_p$ is the volumetric heat capacity.

extremely low material budget with excellent cooling capabilities. Helium has the additional advantage of being inert and safe to operate.

The cooling concept of Mu3e is planned to be a novel gaseous helium system that provides several local flows to cool the tracking layers. The flows are confined by the detector layers themselves. This brings material minimization for the cooling of a pixel detector to an unprecedented optimum. A more technical description follows in the next chapter. In chapter 6, results are presented for a realistic thermal-mechanical mock-up of the vertex detector, which is cooled by such a helium cooling system.

The Mu3e detector setup 4

The basic experimental concept of Mu3e is to stop a high-intensity muon beam with a rate of up to 10^8 Hz on a stopping target in phase I of the experiment. The charged decay products (electrons and positrons) are detected by an HV-MAPS-based tracking detector determining the particle momenta. The experiment is located inside a 1 T solenoidal magnetic field, which results in helical particle trajectories. Precise timing of the tracks is measured by additional detectors based on organic scintillators, which determine the decay time and the charge of the decay products.

The requirements and the general concept of Mu3e were outlined in the previous chapter. A computer-aided design (CAD) visualization of the overall detector is shown in Figure 4.1. This chapter describes the technical realization of the experiment. The focus is on the vertex detector and its helium cooling system. The remaining sub-detectors and services are briefly described.

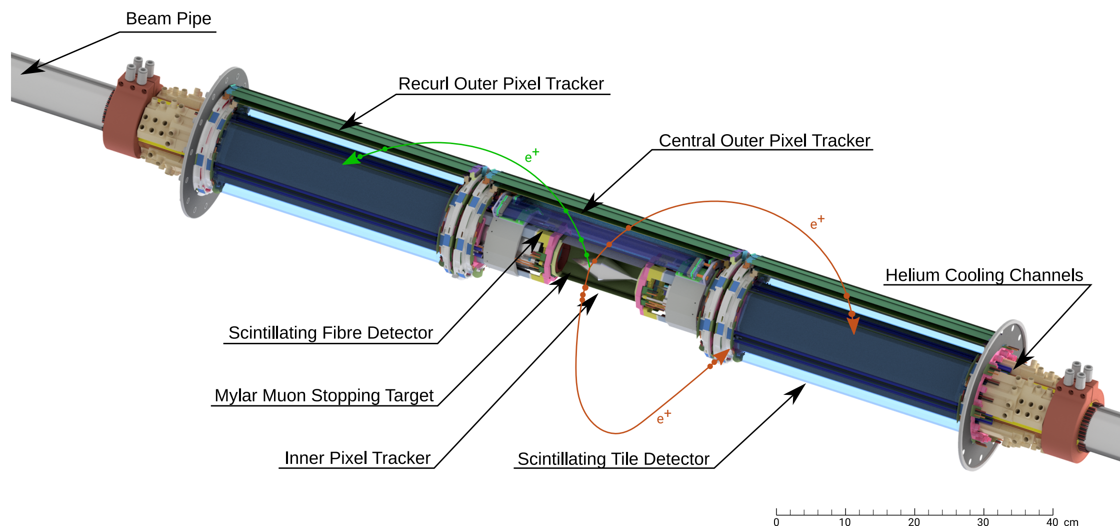


Figure 4.1: The active part of the Mu3e detector, with a central tracker surrounding the stopping target, and US and DS outer pixel tracking stations. Taken from [57]. Based on [22].

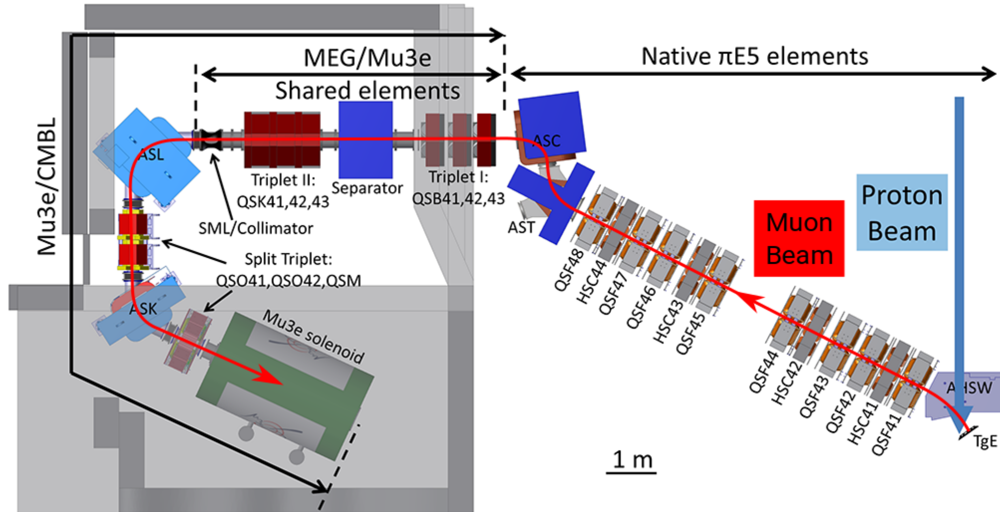


Figure 4.2: CAD model of the entire πE5 channel & CMBL. Based on [22].

4.1 Muon beam, stopping target, and magnet

4.1.1 Muon beam and beam pipes

The Mu3e experiment will be conducted at the πE5 beam line located at PSI, Switzerland. Surface muon rates in the order of $10^8\,\mu^+/\mathrm{s}$ are accessible. The beam of the πE5 channel is guided via the Compact Muon Beam Line (CMBL) to the Mu3e solenoid as displayed in Figure 4.2.

Two dipole magnets (ASL & ASK) direct the beam from the shared πE5 channel to the Mu3e solenoid. Focusing magnets (QSK41-43, QSO41/42 & QSM) ensure that the beam is focused on the stopping target.

The muons enter the helium atmosphere inside the magnet via the US beam pipe. Inside the pipe, there is a degrader to slow down the muons and a collimator to inhibit muons not hitting the stopping target. The beam pipe extends as close as possible to the target. It serves as support structure for detectors and services. On the DS side, the beam pipe serves as an identical support. Inside the DS beam pipe, the mounts for the stopping target are integrated. Power lines, helium channels and support rings are all mounted directly on the beam pipes, as shown in Figure 4.1. The beam pipes themselves are mounted in an experimental cage that is slided into the Mu3e magnet. The experimental cage, in turn, hosts the power boards for low voltage (LV) and high voltage (HV), and the front-end boards (FEBs) for data readout and slow control.

4.1.2 Stopping target

The stopping target is a hollow-double cone made of aluminized Mylar foil. The shape is optimized for a homogeneous distribution of stopped muons, and for a

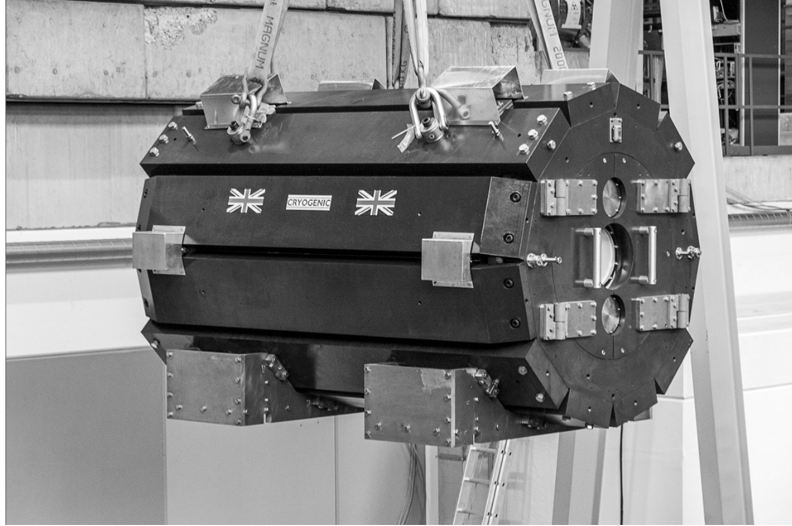


Figure 4.3: Mu3e solenoid [22].

large area to spread the decays vertices, which reduces accidental coincidences. The target dimensions are 19 mm radius and a length of 100 mm. The Mylar thickness is 70 µm at the US side and 80 µm at the DS side for an optimized stopping rate. [22]

The physical stopping target used in the integration run described in chapter 8 is shown in Figure 8.1b.

4.1.3 Mu3e solenoid

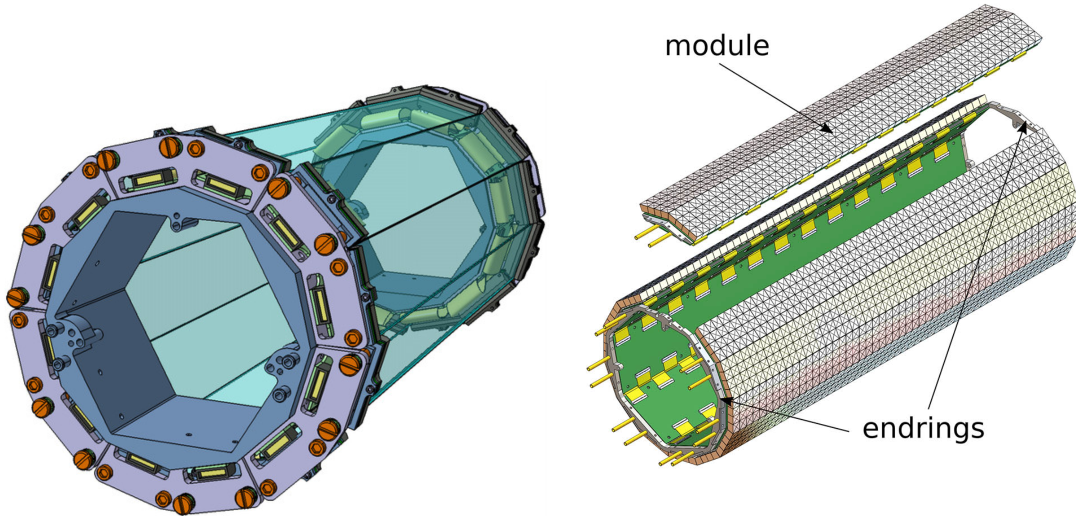
The Mu3e solenoid (Figure 4.3) is a superconducting magnet that provides a magnetic field of 1 T. The required homogeneity is $\Delta B/B < 10^{-4}$. The warm bore has a diameter of 1 m and a length of 2.7 m. It is equipped with a rail system such that the experimental cage can be inserted into the magnet. The warm bore is required to be helium tight during operation which is realized by removable flanges. [22]

4.2 Timing detectors

There are two different types of timing detectors integrated in the Mu3e experiment. The barrel-shaped low-material scintillating fiber detector is located around the vertex detector in the central station. In the recurl stations, US and DS of the stopping target, the scintillating tile detector is placed, which is purely optimized for precise timing.

4.2.1 Fiber detector

The fiber detector (or SciFi) is optimized for low material budget, perpetuating a high efficiency for the suppression of combinatorial background. Figure 4.4a shows a



(a) Structure of the SciFi detector [22]. (b) Structure of the SciTile detector [58].

Figure 4.4: Mu3e timing detectors.

CAD drawing of the detector. It consists of 12 × 3-layered fiber ribbons of 300 mm length on a minimal radius of 61 mm around the stopping target. The fibers are read out by 128-channel silicon photomultipliers (SiPMs) obtaining a timing resolution of around 250 ps. It is located beneath the central outer pixel layers to not add material after the last tracking layer. Its material budget is ∼0.2 % X_0. [22]

4.2.2 Tile detector

The tile detector (or SciTile) is the only sub-detector with no limitations on material budget. Thus, it is mainly optimized for superior time resolution. Its size is determined by the space between services and the outer pixel layers. Figure 4.4b shows a CAD drawing of the detector. Each tile station is made of 7 modules equipped with 8 × 52 plastic tiles wrapped in reflective foils. Each tile is glued to an individual SiPM. The purpose of the detector is to identify three coincident electrons/positrons and to suppress combinatorial background. The detector reaches a detection efficiency of >99 % and a time resolution of <50 ps. [58]

4.3 Tracking detectors

This section describes the tracking detector of the Mu3e experiment, its basis, the MuPix sensor, and its DAQ. The tracking detector is subdivided into the vertex detector, which describes the two innermost layers, and the outer layers. The outer layers consist of three stations, a central one around the stopping target, and two recurl stations US and DS. Since this work describes the construction and studies

sensor size	$20.66 \times 23.18\,\mathrm{mm}^2$
pixel matrix	256×250
pixel size	$80 \times 80\,\mu\mathrm{m}^2$
thickness	$50\,\mu\mathrm{m}$
time resolution	$\leq$20 ns
hit efficiency	$\geq$99 %
power density	$\leq$350 mW/cm^2

Table 4.1: MuPix10 characteristics and requirements [22].

of mock-ups of the vertex detector and its first functional prototype, it is described in more detail compared to the outer layers.

4.3.1 MuPix sensor

The MuPix sensors are HV-MAPS specifically designed to be operated in Mu3e. MuPix10 is the first full-scale prototype of the MuPix series of pixel chips that is designed to be fully compatible to be operated in the Mu3e tracking detectors [43]. It is used in the vertex detector prototype described in chapter 7. Detailed studies of MuPix10 are summarized in [59–61].

MuPix10 is manufactured in a 180 nm HV-CMOS process at TSI semiconductors[1]. The main geometrical characteristics and the performance requirements of the chip are summarized in Table 4.1. The chip is divided into an active matrix and a periphery containing the readout structure (Figure 4.5). The active pixels have an integrated charge-sensitive amplifier. The analog signal is driven via a long-line connection by an NMOS source follower to the periphery. In the periphery, each pixel has a digital partner cell. There, the input signal is discriminated by two individual thresholds. The low threshold enables precise timestamping, while the high threshold validates a hit and suppresses noise. The arrival time of the pulse is assigned to an 11-bit timestamp (TS). The time when the signal is below the threshold again is assigned to a 5-bit timestamp (TS2). The typical bin sizes used for MuPix10 are 8 ns for TS, and 128 ns for TS2. The time over threshold (ToT) is given by:

$$ToT = TS2 - TS, \tag{4.1}$$

which can be used as a tool to discriminate background and for offline time-walk correction as described in detail in [60]. The hits are read out by a column-drain procedure, where columns with hits to read out are flagged. This way, a continuous readout with zero suppression is realized. The chip is divided into three sub-matrices

[1] TSI Semiconductors, USA, http://www.tsisemi.com.

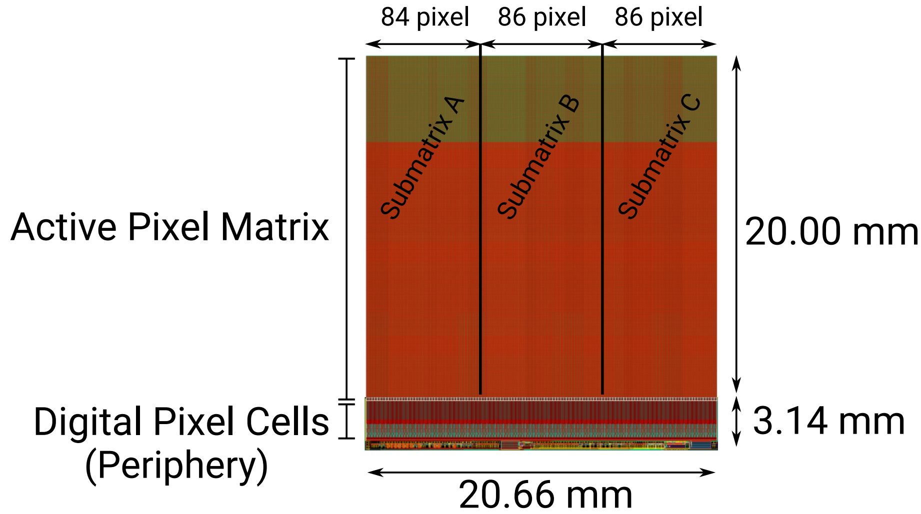


Figure 4.5: The MuPix10 chip. The pixel matrix is subdivided into three parts. Each sub-matrix is read out by an individual data link. [28]

with each of the readout links operated with 1.25 GBit/s. The data outputs can also be multiplexed and sent out by a shared data link.

Tight space constraints on the power lines require that the number of power channels is kept at a minimum. Thus, the chip is designed to need only a single supply voltage (VDD). The amplifier voltage VSSA is generated on-chip by a voltage regulator [28, 31, 59]. The chip configuration interface is supposed to be realized by a single differential input [28]. For MuPix10, the implementation is malfunctioning, which requires the usage of the serial peripheral interface (SPI) and results in necessary design changes of the ladders to operate the chips on them as discussed later. The average heat dissipation of the MuPix10 is measured to be around $220\,\mathrm{mW/cm^2}$. Hit efficiencies of $>99.9\,\%$ are reached for a noise-per-pixel-rate of $<2\,\mathrm{Hz}$. The intrinsic time resolution is determined to be $(6 \pm 1)\,\mathrm{ns}$. [28, 57]

The MuPix10 fulfills most major requirements for a pixel chip in Mu3e. The malfunctioning chip configuration of MuPix10, however, requires a modified ladder geometry to operate them on ladders. These changes are not compatible with the final detector design, as will be outlined in section 7.1. A MuPix10-based vertex detector prototype, though, is suitable to test the Mu3e pixel DAQ and the operation of a fully-equipped detector with helium cooling as done in the integration run described in part IV. For the final chip, MuPix11, some minor improvements have to be realized, particularly to enable the operation with the baseline ladder design.

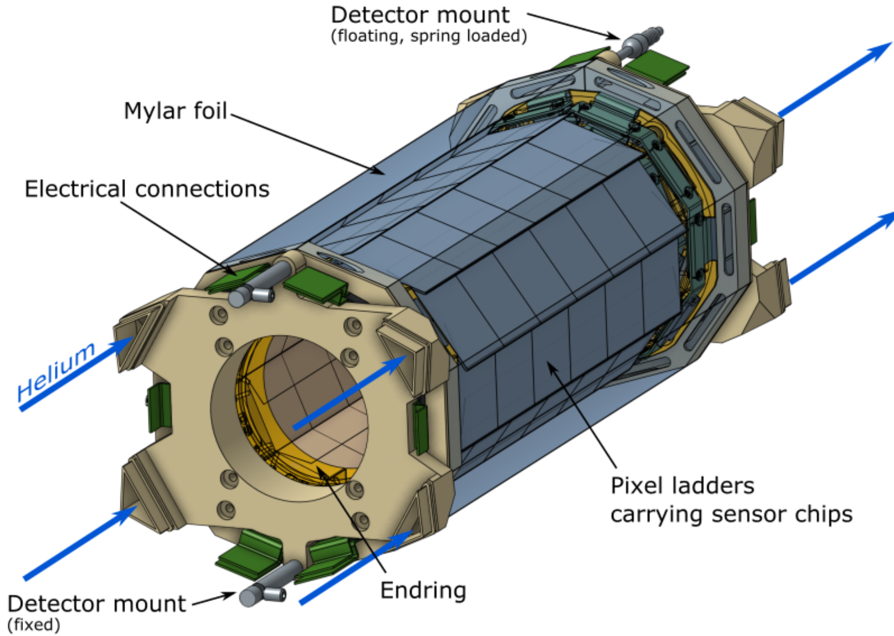


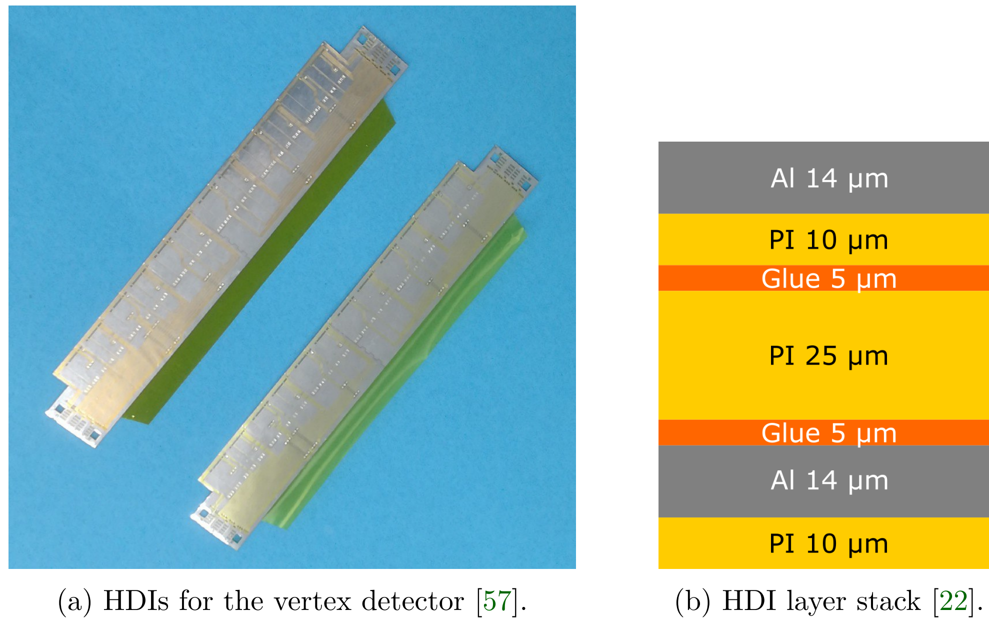
Figure 4.6: The Mu3e vertex detector [22].

4.3.2 Vertex detector

The Mu3e vertex detector (Figure 4.6) consists of the innermost two tracking layers around the stopping target. In the following, they are referred to as Layer 0 (L0) and Layer 1 (L1)[2]. An overview of the characteristics of the different tracking layers is given in Table 4.2. The basic building blocks of the detector are ladders. These are made of six MuPix chips glued on a high-density interconnect (HDI) provided by LTU [62]. The HDIs (Figure 4.7a) are flex circuits made of aluminum-polyimide laminates. Their layer stack is displayed in Figure 4.7b. It consists of two aluminum circuit layers with a polyimide insulating layer in between, the spacer layer. The HDIs provide the supply voltage, HV, reference clock, configuration lines, and data output lines (Figure 4.8). All three data lines per chip are used for the vertex detector to cope with the high rates. The ladders come with a gluing flap on one side, which forms a joint with the neighboring ladder. Chips from neighboring ladders have an overlap of their active pixel matrices, as illustrated in Figure 4.9. This increases the acceptance, particularly, for low momentum tracks. The glued ladders form a stiff and self-supporting structure. Besides the HDIs, chips, and adhesives, no other material is present in the acceptance region of the detector. The individual contributions to the material budget are listed in Table 4.3.

The detector is partitioned in four modules, corresponding to two half-shells per layer. Each partition is supplied by a common LV and HV channel. The ladders are mounted on end pieces made of polyetherimide (PEI) (yellow in Figure 4.6). The

[2] In many Mu3e publications like in [22], the tracking layers are numbered from 1 to 4. In this work, the layer numbering is kept consistently from 0 to 3.



(a) HDIs for the vertex detector [57]. (b) HDI layer stack [22].

Figure 4.7: HDIs for the Mu3e pixel detectors.

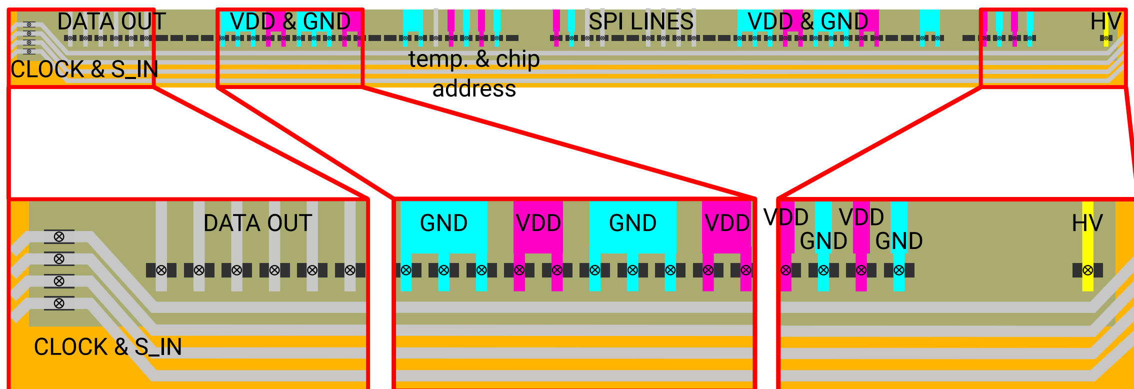


Figure 4.8: Sketch of the MuPix bonding scheme on HDI. In the bottom, three zoomed-in areas are shown. The supply voltage VDD is colored in magenta, GND in cyan, and HV in yellow. The external clock and the single differential input (gray) are provided by bus traces. The data output lines (gray) come as differential pairs, which are vertically aligned. The temperature diode of one chip per half-ladder is connected by a single-ended line. For MuPix10, SPI lines are integrated to configure the sensor, which are removed in the baseline design.

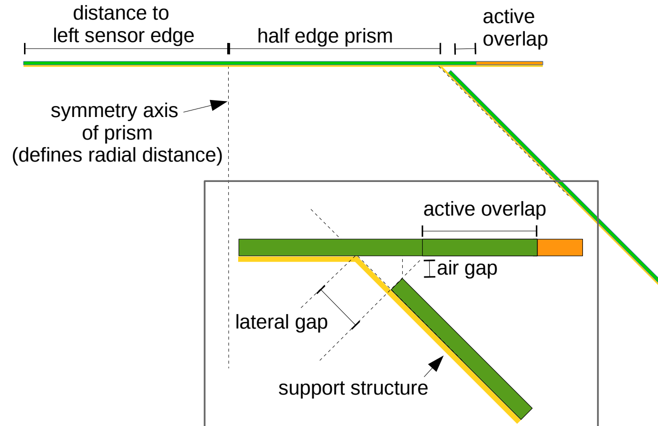


Figure 4.9: Overlap of two ladders of the same tracking layer in the vertex detector. Green indicates the active matrix, orange indicates the chip periphery. Material thicknesses are not to scale. [22]

	L0	L1	L2 (recurl)	L3 (recurl)
minimal radius [mm]	23.3	29.8	73.9	86.3
length [mm]	124.7	124.7	351.9	372.6
chips/ladder	6	6	17	18
# ladders	8	10	24	28
max. hit rate [10^6 /chip/s]	5.2	5.2	1.2 (0.15)	1.2 (0.14)

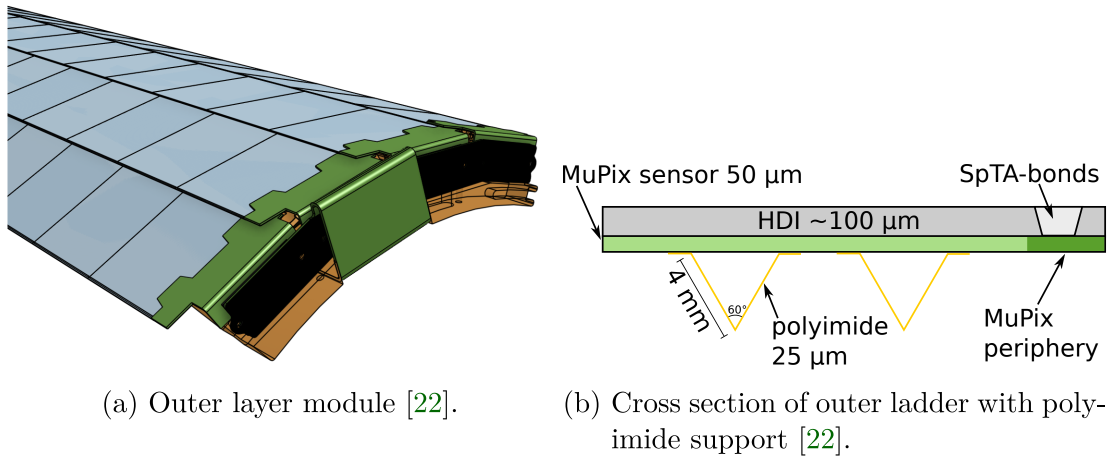
Table 4.2: Overview of tracking layer characteristics.

end pieces are mounted on an end ring that is connected to the gas distribution ring (light gray in Figure 4.6). The electrical connections to the outside are realized by conventional polyimide copper flex circuits. The HDI is connected to these flex circuits by an interposer (cf. section 5.2). The detector is placed between the beam pipes with mounts attached to the gas distribution rings. The ladders are tensioned by a spring load on one side. The LV is provided by copper rods with a cross section of $5 \times 2.5\,\mathrm{mm}^2$, which are glued onto the beam pipes

The coolant, gaseous helium, is provided via ducts placed on the beam pipes. By the distribution ring, the helium is uniformly distributed into two separate flow channels. The first is confined by L0 and L1 themselves. A second flow channel around L1 is confined by a 2 µm thin Mylar foil sealing the vertex detector. The helium system providing the gas is described in section 4.4.

	thickness [µm]	X/X_0
MuPix	50	0.54×10^{-3}
HDI polyimide & glue	45	0.18×10^{-3}
HDI aluminum	28	0.31×10^{-3}
polyimide support	25	0.09×10^{-3}
adhesives	10	0.03×10^{-3}
total	158	1.15×10^{-3}

Table 4.3: Material budget of a vertex detector layer.



(a) Outer layer module [22]. (b) Cross section of outer ladder with polyimide support [22].

Figure 4.10: Outer pixel layers.

4.3.3 Outer layers

The outer tracking layers are composed in a similar fashion as the vertex detector. The ladders are equipped with more chips, which makes them longer (cf. Table 4.2). Each layer in each station is modularized in groups of four ladders, as displayed in Figure 4.10a. The ladders are not glued together. They are supported by two v-shaped polyimide channels (Figure 4.10b) due to their length. The electrical connections are realized analogously to the vertex detector, except that only the multiplexed data link is used for each chip.

The helium gas is supplied via ducts on the beam pipes and distributed by the support ring into the volumes between the SciFi detector & Layer 2 (L2), and L2 & Layer 3 (L3). In addition, there is a global flow around the whole detector that cools the outermost layer.

4.3.4 Data Acquisition

The pixel DAQ is described briefly in this section. A detailed overview is given in [22, 63]. The Mu3e DAQ has to cope with 100 GBit/s for a muon stopping rate of $10^8\,\mu^+$/s. It runs triggerless and sorts all data into time slices to enable non-local track finding.

The data is sent from the MuPix chips via the HDI, flex circuits, and micro-twisted pair cables to the field-programmable gate array (FPGA)-based FEBs inside the magnet. On the FEBs, data from up to 36 links is received. It is time-walk corrected and sorted in time. The resulting output is a fully-time sorted data stream containing the hit addresses with time information.

This data is sent to an FPGA-based switching board in the counting house by optical links. The switching board receives the sorted data from up to 34 FEBs. On the board, the data is time aligned and merged. From the switching boards, the data is sent to the filter farm. A geometrical selection for track candidates from triplets, particle hits in the first three layers, is made. A multiple-scattering-based track fit searches for hits in the fourth tracking layer. If a combination of two positively and one negatively charged tracks with a common vertex is found, the corresponding time frame is tagged for readout. A full reconstruction is performed for these events and the data is stored. All steps reduce the data rate to store to 100 MBit/s.

In the integration run, described in part IV of this thesis, a simplified version of the Mu3e DAQ is used. Only hits from the two inner tracking layers are available. There is no filter farm implemented. The presented correlation analysis is based on the time-sorted data output from the switching board.

4.4 Helium cooling system

The helium cooling system provides cooling for the pixel detectors. The readout electronics of the timing detectors and the FEBs are cooled by a conventional water cooling system. The helium system is designed to ensure detector temperatures <70 °C, which is the glass transition temperature of the adhesives used, for power densities of up to 400 mW/cm^2. The design allows gas inlet temperature down to −20 °C. The baseline inlet temperature is 0 °C.

A functional sketch of the final helium cooling infrastructure is shown in Figure 4.11. It provides four individual supply channels, one for each outer layer station, and one for the vertex detector. The mass flows are 16 g/s and 2 g/s, respectively. A turbo compressor enables the mass flow on each line. Large diameter piping (inner diameter of $\varnothing = 50$ mm for 2 g/s, and $\varnothing = 125$ mm for 16 g/s) ensures a low pressure drop along the supply lines toward the magnet. The supply lines are coupled to the magnet via a flange plate. The warmed-up gas is guided back to the helium plant by a single exhaust channel. Beside the turbo compressors, the plant consists of a central heat exchanger to pre-cool the gas, a helium purification system, and a

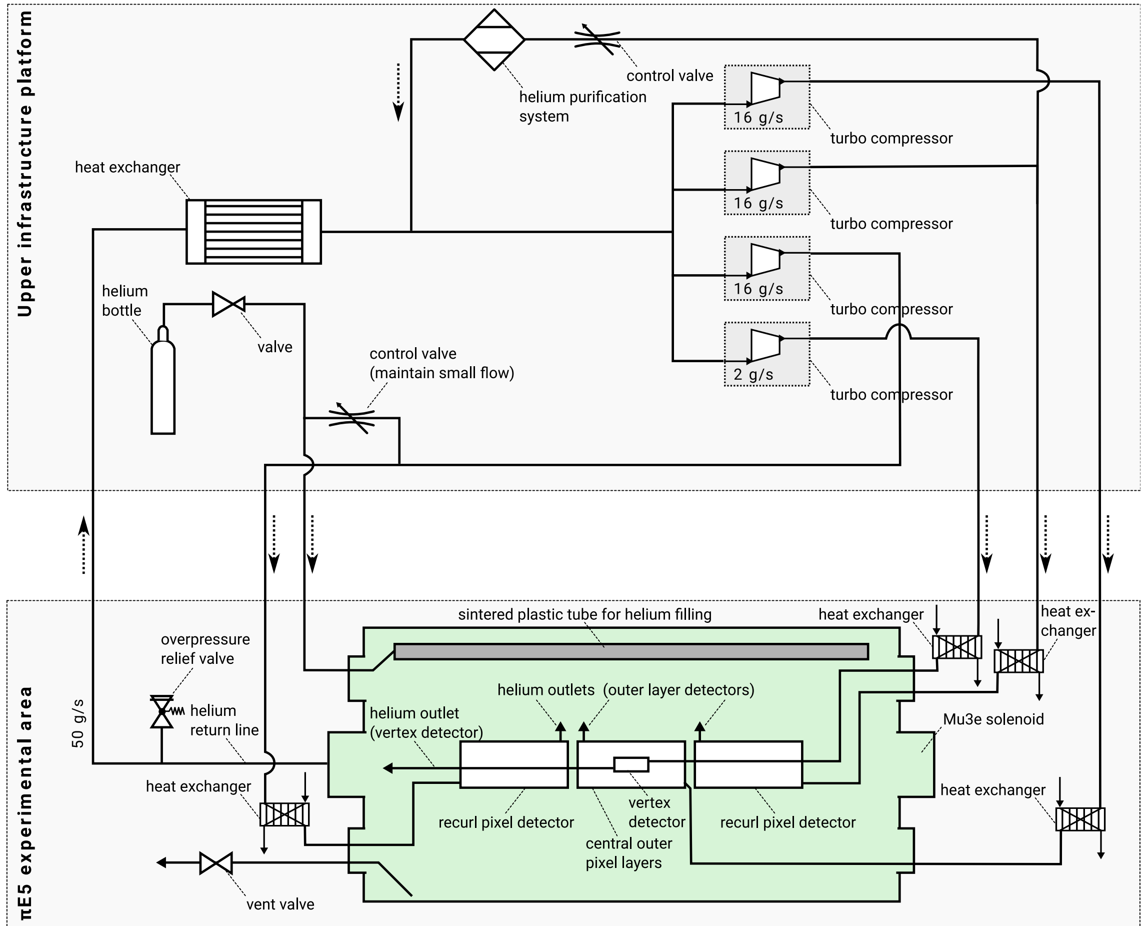


Figure 4.11: Process flow diagram of the helium cooling infrastructure. The cooling plant is located on an upper infrastructure platform. The conditioned helium is transferred through pipes and flexible tubing to the experiment in the πE5 area. [64]

heat exchanger at each gas inlet to the magnet to cool the gas to the nominal inlet temperature.

Inside the magnet, the helium channels are distributed to the corresponding detectors. In Figure 4.12, the helium flow channels in the central detector station are visualized. The helium is guided via ducts on the beam pipes. The gas distribution rings divide the helium into separate flows around the pixel layers.

In the cooling studies described in this thesis, a simplified version of the presented helium system is used. A single turbo compressor providing 2 g/s of helium is used in a closed loop together with a plate heat exchanger. No purification system is integrated, which is compensated by constantly flushing helium into the system, or operating the set-up in a finite period until the air contamination crosses a certain threshold.

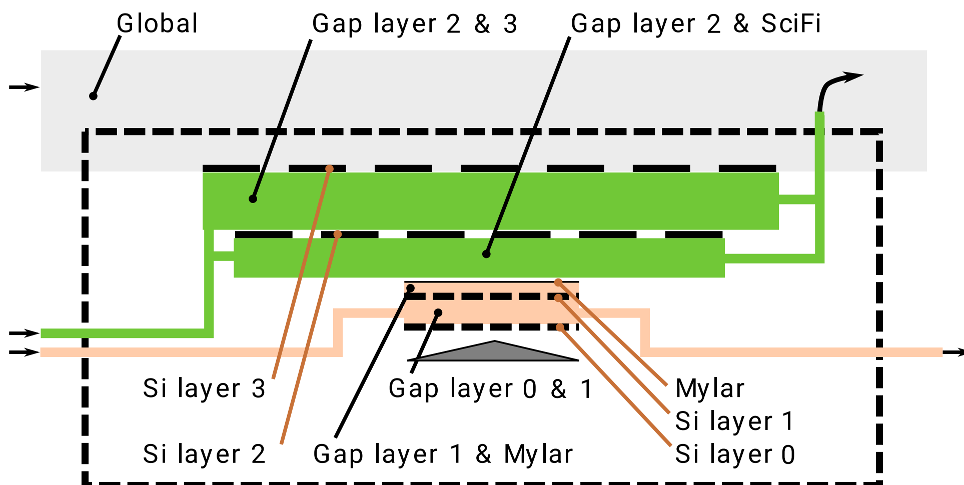


Figure 4.12: Sketch of the helium flows for cooling the central detector station. Pink is the gas flow for the vertex detector, green is the gas flow of the outer layers, light gray indicates an additional global flow, dark gray shows the muon stopping target. [61]

Part III

The construction and the helium cooling of thermal-mechanical mock-ups of the vertex detector

The Mu3e helium cooling system is a one-of-a-kind concept in particle physics. Gaseous cooling of pixel detectors has been successfully applied in STAR, as outlined in chapter 3. Helium as coolant, however, is a technical novelty that needs to be verified before detector construction.

Regarding the Mu3e vertex detector, this work concludes a series of studies that was carried out to validate the Mu3e helium cooling concept. First tests with an inductive heating setup performed by Zimmermann in 2012 showed that forced convection by gaseous helium cooling can be used to cool silicon sensors [65]. Huxold constructed in 2014 a first simplified thermal-mechanical mock-up of the outer pixel layers and characterized the cooling abilities using air, paired with simulations [66]. Both works studied an expected maximum heat dissipation of only 150 mW/cm^2.

These works were followed by simulation and measurement studies by Ng [67] and Herkert [68]. Ng showed in a detailed simulation that a cooling system can be realized for a heat dissipation of 250 mW/cm^2. It implied individual flow channels for the vertex detector and the outer layers, and additional helium channels in the v-shaped polyimide supports for the outer layers. For a conservative limit of 400 mW/cm^2, a modified v-fold geometry and higher mass flows were found to be required. Herkert performed first measurements with helium as coolant using simplified thermal-mechanical mock-ups of the outer layers. The experimental results were in good agreement to the simulations from Ng.

The realization of the helium supply inside the detectors was simulated by Tormann in 2018 [69]. It showed a sufficient cooling performance for the outer layers and indicated that a second cooling channel around L1 is necessary for the vertex detector.

All studies were based on simplifications of the detector geometry. The pixel layers were constructed and simulated assuming a circular or a prism-shaped design. Important geometrical details like the overlap of sensors on neighboring ladders were not included. The influence of the helium supply and the support material had not been considered.

The studies presented in this thesis aim to give the final picture of the gaseous helium cooling system for the vertex detector.

The thermal-mechanical mock-ups, constructed in the scope of this work, resemble for the first time the true detector geometry in all details. Two types of mock-ups are constructed. The first, simpler version, consists of aluminum-polyimide tapes which can be actively heated. The main difference to the final detector is that the tapes are the active heat source, and the chips are replaced by 50 µm thin steel chips. Thus, compared to the final detector, other materials are used. The corresponding thermal studies [70, 71] were carried out by Deflorin in 2019 at the FHNW and are only briefly summarized below. They confirm the necessity of a second helium flow around L1, which has been included in the baseline design since then.

The second mock-up type is based on silicon heater chips. They serve as active heat sources and form ladders on HDIs like in the final detector design. Its construction is accompanied by the development of the quality control (QC) procedure

for pixel ladders of the vertex detector. The QC results validating the mock-up construction are presented in detail in chapter 5. This silicon heater mock-up enables a highly granular temperature measurement, since every chip is equipped with a resistive thermometer. It is operated as the first mock-up together with the helium cooling plant prototype, which provides a closed helium flow of 2 g/s. The results of the thermal characterization and their consequences are discussed in detail in chapter 6.

The construction of the tape-heater and the silicon heater mock-ups for the outer layers are ongoing at the laboratories of the collaboration partners in Oxford and Liverpool, UK. The corresponding thermal studies are scheduled for 2022 and will finally conclude the cooling studies for the Mu3e pixel detectors.

Production of thermal-mechanical mock-ups

5

This chapter presents the production of the thermal-mechanical mock-ups of the Mu3e vertex detector. First, the requirements of the detector production are briefly discussed. This is followed by a summary of the mock-up construction, with a focus on the quantitative analysis of the chip placement, the glue thicknesses, and the electrical connections.

A detailed description of the developed tooling and working steps to construct the ultra-thin vertex detector ladders and modules is given in the appendix A of this thesis.

5.1 Requirements

The general geometrical constraints for the vertex detector are presented in chapter 4. The specific requirements to fulfill by the production are the spatial precision of the chip positioning, the minimization of the material budget, and a production that is reliable, safe, and comes with an appropriate timescale and yield.

5.1.1 Spatial precision

The placement precision for the chips on a ladder can be divided into the gap size and the lateral displacement. The placement pitch of the chips is specified to be 22.70 mm. With a chip width of 22.66 mm, this results in a gap size of 40 µm.

It is considered as the minimum possible distance to exclude chip collisions, as illustrated in Figure 5.1. This comes from the different thermal expansion coefficients α_i (equations 5.1 and 5.2) for polyimide [72] and silicon [73], the two materials forming a ladder.

$$\alpha_{Si} \approx 2.6 \times 10^{-6} K^{-1} \tag{5.1}$$

$$\alpha_{polyimide} \approx 20 \times 10^{-6} K^{-1} \tag{5.2}$$

The coefficients differ by almost a factor 10. The thermal expansion/contraction of the ladders is dominated by the polyimide. Approximating the glue dot distance for

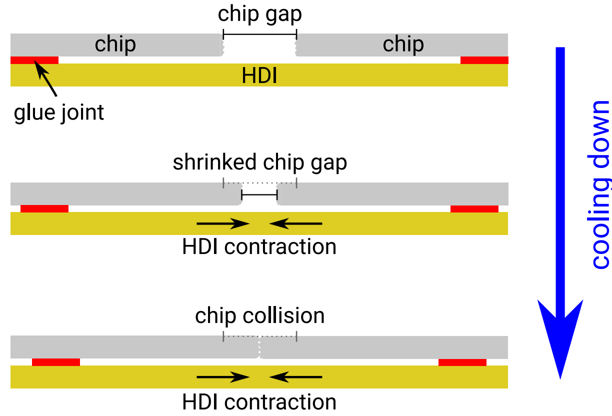


Figure 5.1: Chip gap shrinks when cooling down the detector due to the higher thermal expansion coefficient of the HDI compared to silicon (cf. equations 5.1 and 5.2). A minimum chip gap size is required during assembly to exclude chip collisions at low temperatures.

neighboring chips with 10 mm, this would result in a contraction of 2 µm/10 K. The ladders are produced at room temperature, the helium cooling system is designed to be able to provide gas temperatures down to −20 °C. Thus, a maximum contraction of 8 µm is expected. However, thermal coefficients for polymers are observed to vary by up to a factor 2. To stay safe, the defined gap size is 40 µm, which is double the distance of the conservative estimate for the contraction and also takes the uncertainty on the scribe line from chip cutting into account. The maximum allowed gap size deviation is defined to be $\sigma = 5$ µm.

The silicon heater ladders are designed for a smaller chip pitch of 20 mm, since the silicon heater chip dimensions correspond to an old design. This also includes a larger gap size of 100 µm. The same precision requirement on the longitudinal displacement of $\sigma = 5$ µm defined above is applied to their construction.

The lateral placement precision of the chips on a ladder is given by the overlap of the bus traces for the *reference clock* and *serial input* and their corresponding bond pads on the chip (Figure 5.2). This gives an allowed displacement of *pad width - trace width* / 2 = 13.5 µm.

5.1.2 Material budget

Each pixel layer of Mu3e is expected to have a radiation length of $X/X_0 \approx 0.115\,\%$. Since all components that constitute the ladders and the chips have a predefined thickness, the only material that can be minimized during production is the glue. The adhesives used for chip gluing are accepted in the technical design to have a thickness of 10 µm resulting in a radiation length of only $X/X_0 \approx 0.003\,\%$, being 2 % of the overall material budget of a pixel layer [22].

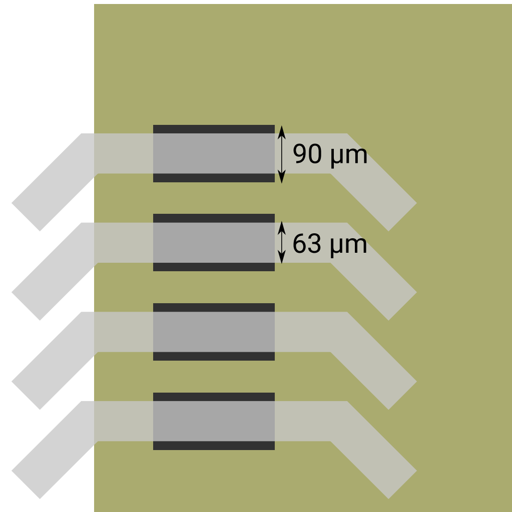


Figure 5.2: Sketch of the bottom left corner of a MuPix chip with overlaying aluminum traces of the HDI (cf. Figure 4.8). Lateral placement precision is determined by the trace width and bond pad width.

For the vertex detector production, the goal is to reach an average glue thickness of 5 µm. This way the effect of the glue on multiple-Coulomb scattering is minimized as much as possible.

5.1.3 Producibility

The Mu3e vertex detector consists of 18 ladders, totaling 108 MuPix chips. Considering pre-production and spares, these numbers are expected to triplicate for the overall production. It is a comparably small-scale project, compared to the outer layers with 2,736 installed MuPix chips,

Given the small number of detector units, the realization of an automated production, e.g. using a gantry to place chips and dispense glue for the ladder construction, is expected to tie up more resources than producing the vertex detector in a manual approach.

The goal is to develop tooling and working steps with an acceptable total yield of 50 % to 70 % and consistent performance. This includes minimizing the risk originating from human error and the reproducibility of the production. An appropriate timescale is the production of one ladder per working day. Assuming the production of all 54 ladders requested, this would result in less then 3 month production time.

5.2 Mock-up components

The used components for the construction of mock-ups can be divided in the following categories: chips, flex circuits, interposers, and support structures. For the tape heater mock-ups, the flex circuits and chips are replaced by aluminum-polyimide

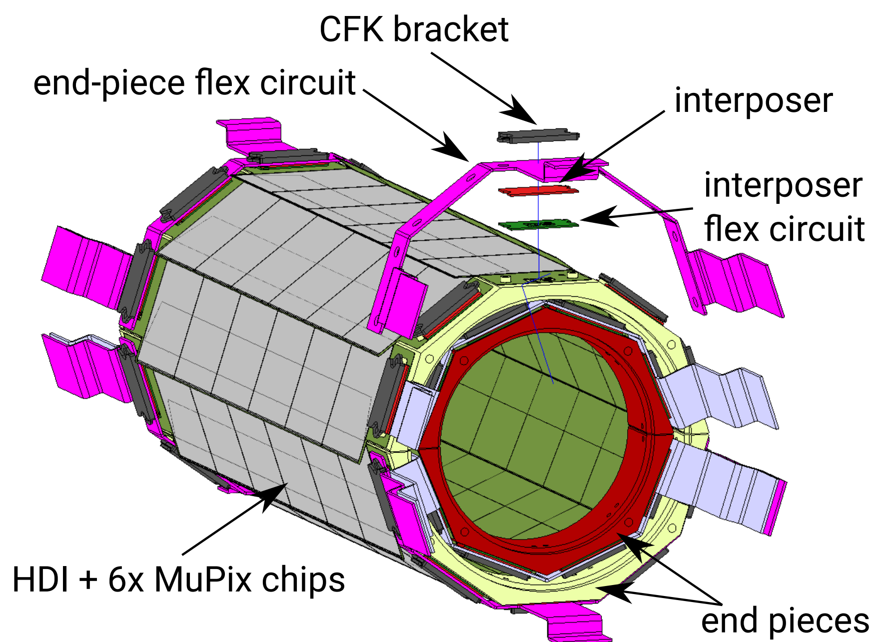


Figure 5.3: Exploded view of the electrical vertex detector components. The HDIs are contacted via the interposer flex circuits and interposer connectors to the end-piece flex circuits. Each stack is compressed by a carbon-fiber-reinforced polymer (CFK) bracket.

laminates and dummy steel chips. The silicon heater mock-up is made of the final materials, only their functionality differs from the final detector. An exploded view of the electrical components and the main support is shown in Figure 5.3.

5.2.1 Tape heater mock-up components

Aluminum-polyimide laminates

For the tape heater mock-up, the HDIs used for the final detector are replaced by custom aluminum-polyimide laminates of around 50 µm thickness. They are structured by a laser cutter in Heidelberg. In Figure 5.4, the top ladder shows a bare tape heater for L0 and L1. Through the polyimide film one can see the structured aluminum layer on the backside. Two meanders with a resistance of around 0.5 Ω can be used for heating. The tape heaters are equipped with 50 µm thin dummy steel chips of 20 mm × 23 mm size.

The mock-up is connected to the outside via custom end-piece flex circuits made of the same laminates as the heater ladders with integrated power contacts. The end-piece flex circuits are connected to all ladders of a module via interposer connectors,

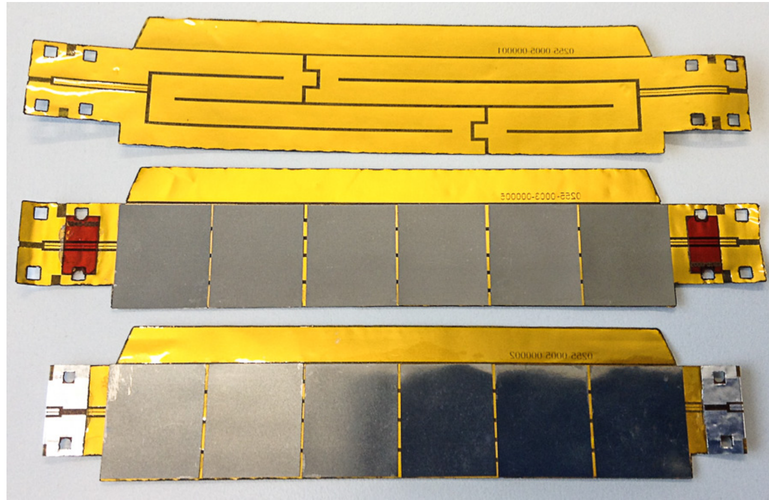


Figure 5.4: Ladders of the tape heater mock-up for L0 and L1. Top to bottom: bare heater with meander; stiffener attached to match final dimensions, dummy chips glued on; large contact pad pair on both ends used for powering. Chip size: 20 mm × 23 mm. [22]

which are described below. The flex circuit is structured such that all ladders are powered in series.

Interposer

The interconnection between ladders and the end-piece flex circuit is realized by interposers (cf. Figure 5.3). The interposer used is a Samtec ZA8H [74] connector (Figure 5.5). It provides a micro grid of 7 × 12 gold-spring contacts. Its overall size is 13.11 mm × 7.1 mm with a thickness of 300 µm in the compressed state. It combines a high-power rating of 500 mA per pin with a high-rate signal transmission of up to 30 GHz.

The type of connector is of particular interest for Mu3e due its small size and high contact density. The space taken by the interconnect is mainly limited to the size of the bracket which is needed to compress the interposer.

End pieces and end rings

The end pieces (Figure 5.6) are the main mechanical support for the vertex detector modules. They are milled half-rings made of PEI with 4 or 5 facets for each ladder to hold.

The end pieces are attached to a 3D printed helium distribution ring that is attached to the beam pipe. This ring is connected on one side to the helium ducts on the beam pipe that supply the detector with helium. On the other side, it distributes the helium into the flow channels: inside the gap between L0 and L1, and between L1 and the Mylar foil for the final design. The second channel around

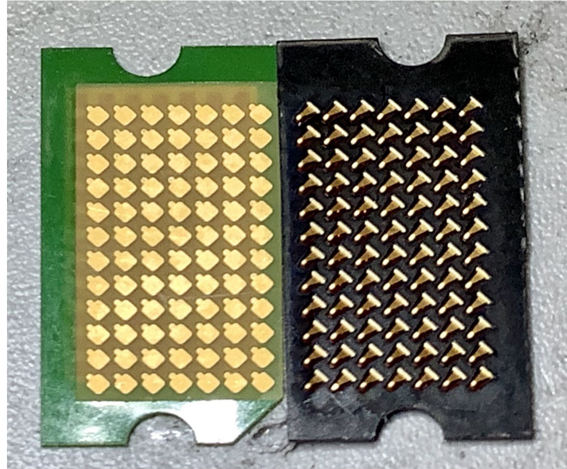


Figure 5.5: Interposer flex circuit (left) for the silicon heater ladders and interposer connector (right).

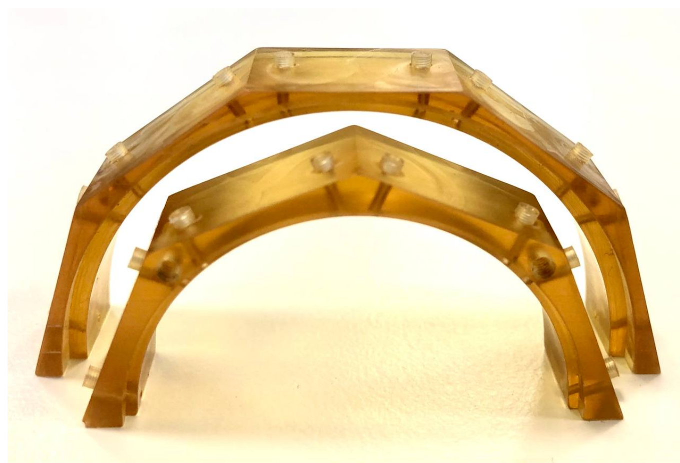


Figure 5.6: PEI end pieces for L0 (front) and L1 (back). The facets are equipped with pins of 2 mm diameter with M1.2 threads for screws to compress the interposer stack.

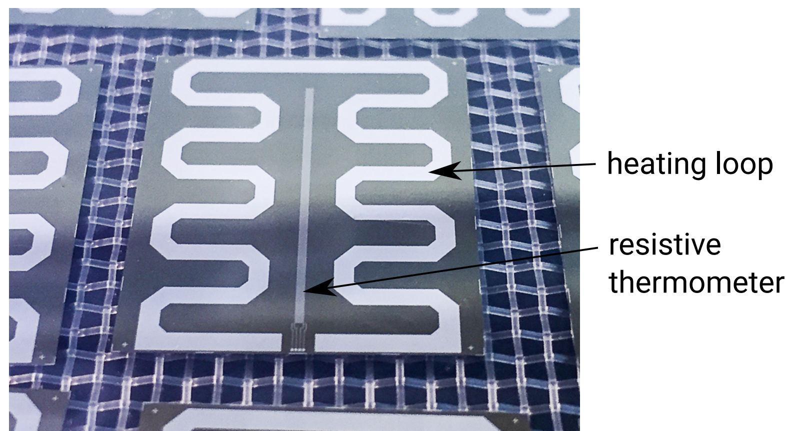


Figure 5.7: Silicon heater chip with two aluminum meanders, one for heating, the other as a resistive thermometer. The thermometer consists of 10 windings of a 10 µm thin aluminum trace. The chips have been manufactured at the Max-Planck Halbleiterlabor in Munich. [22]

L1 was not baseline when the tape heater mock-up was constructed and is only implemented for the silicon heater mock-up.

5.2.2 Silicon heater mock-up components

Silicon heater chips

The silicon heater chips (Figure 5.7) serve as stand-ins for the active MuPix chips for thermal-mechanical studies. They are 50 µm thin silicon chips with a slightly smaller size (19.9 mm × 23.0 mm) compared to the MuPix chips. An aluminum layer is sputtered on the silicon substrate and structured to form two meanders. One meander serves as a heating resistor with a designed resistance of 3.24 Ω. The second is a resistive thermometer with a resistance of around 1250 Ω at 0 °C. It is connected to four bond pads enabling four-wire sensing for the temperature readout. The chip can be resistively heated with variable heat loads while reading constantly its temperature. The silicon heater chips come with fiducial marks at the corners to align the HDI to the chips. Variations of up to 100 Ω on the reference resistance require a calibration of the thermometer for each chip. The heating resistance of the chips is found to deviate systematically from the design value. It is measured to be $(2.75 \pm 0.05)\,\Omega$, which is around 15 % below the expected value.

High-density interconnects

An HDI for the silicon heater mock-up is shown in Figure 5.8. Each chip is individually connected to power via the wide traces to minimize the voltage drops. The four narrow traces for each thermometer are guided between the power traces. A schematic drawing is displayed in Figure 5.9. The silicon heater HDIs come in

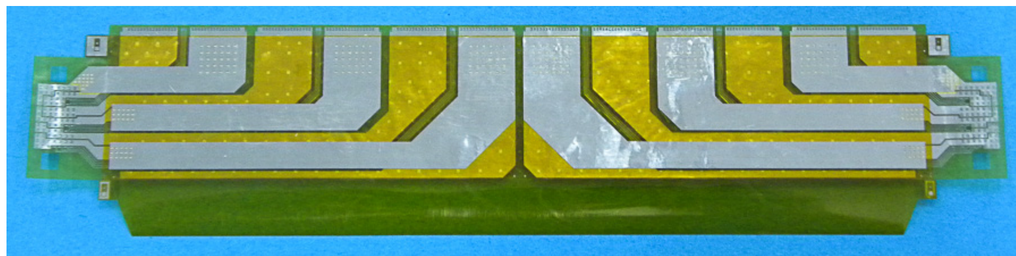


Figure 5.8: HDI for the silicon heater mock-up. Left (US) and right (DS) sides are electrically separated. Gluing flap on bottom side is glued to neighboring ladder on the module. [22]

two flavors: with and without a polyimide spacer layer (Figure 5.10). The default stack (cf. section 4.3.2) includes the spacer layer. The production of ladders without spacer is motivated by a stability test to evaluate if the material budget can be further reduced. As the gluing flap is made of the spacer layer in the baseline design, the ladders without spacer come without gluing flap. The silicon heater modules are made of one ladder without spacer at the edge where no gluing flap is needed and all other ladders with spacer.

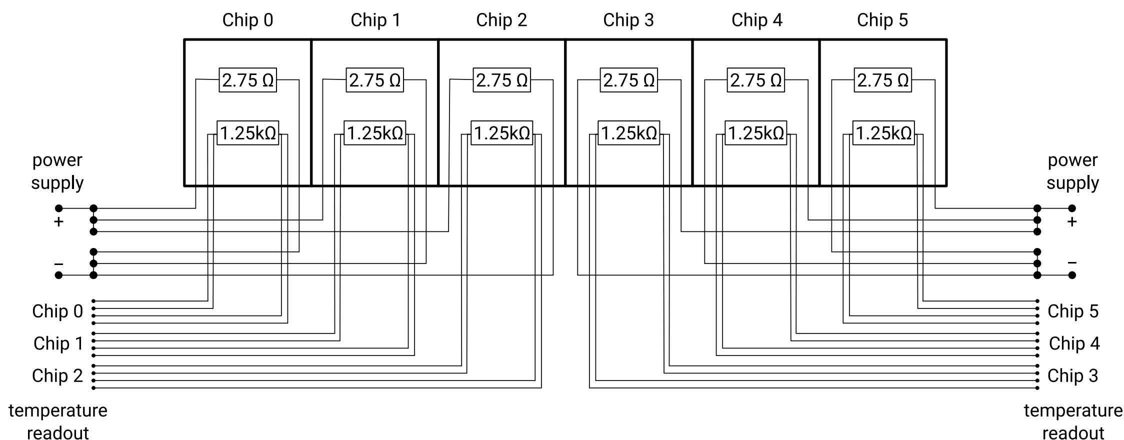


Figure 5.9: Schematics of a silicon heater ladder. On both sides, the three heater chips are powered in parallel.

Interposer and end-piece flex circuits

These flex circuits are used to guide power and signal lines from and to the detector. Both the interposer and end-piece flex circuits are conventional 6-layered copper-polyimide flex circuits. They are used for contacting the interposer, which can not be done with the soft aluminum traces of the HDIs.

The interposer flex circuit then connects to the interposer connector (cf. Figure 5.3). The version for the silicon heater ladders is shown in Figure 5.5. Its

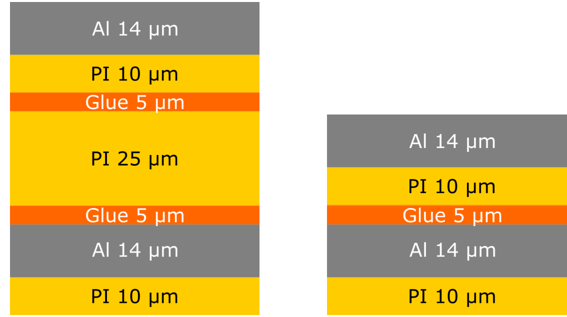


Figure 5.10: Comparison of the HDI layer stacks. Left: baseline including polyimide spacer layer in the middle, right: without spacer layer.

backside matches the pattern of the interposer micro-grid. For the silicon heater mock-up, the interposer flex circuit is simply a point-to-point connector with a 7×12 grid for spTAB on the front side.

The end-piece flex circuits for the silicon heater mock-up for L0 and L1 are shown in Figure 5.11. They connect a detector module to the outside. On both sides, US and DS, they connect to all interposers (4/5 for L0/L1) of one side of a module and guide power and signal lines via their wings toward the beam pipe. For the silicon heater mock-up, the temperature and power lines of each half-ladder share a common ground due to limited space. The cables for powering the heater chips and reading out the thermometers are directly soldered on the solder pads on the wings.

For the final vertex detector, the end-piece flex circuits are connected to interface printed circuit boards (PCBs) located on the beam pipe via a 10×20-pin interposers. This non-permanent connection enables the separate mounting of the vertex detector and its power and data cables on the beam pipe.

5.3 Production of the tape heater mock-ups

The tape heater mock-up is constructed to verify the thermal simulation studies described in [70] and to serve as proof-of-principle for the constructibility of the vertex detector. The ladder assembly is based on a rudimentary procedure. The dummy steel chips are glued and positioned by hand to the tape heater ladders. In turn, the module assembly is performed on the final assembly tools presented in the appendix A.3. The working steps of the assembly of a module are performed in the same way as foreseen for the final detector construction. The resulting modules (Figure 5.12) show that the ultra-thin detector is self-supporting and offers an impressive intrinsic stability. All working steps are verified, no collisions or other problems are observed. The tape heater mock-up demonstrates that the conceptual design of the tooling for the module construction works.

For thermal studies, thermocouples are glued onto the modules, as shown in Figure 5.12. Power for heating is applied to the end-piece flex circuit wings. This way, the heating loops on each side of a module are powered in series. The full mock-

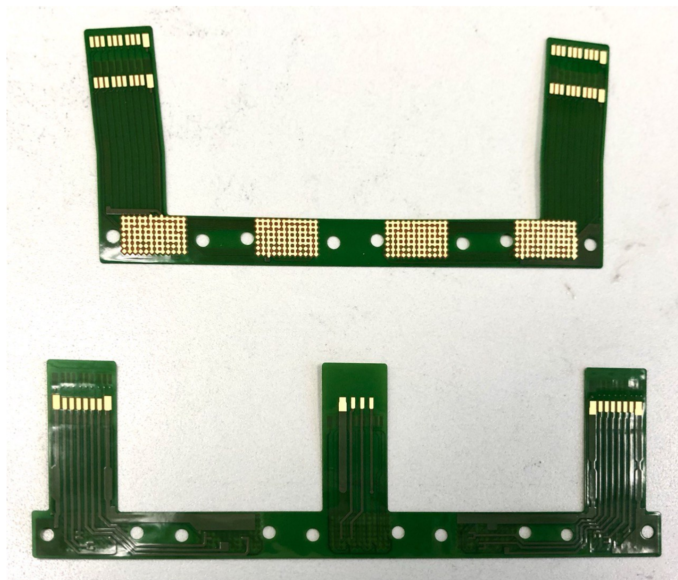


Figure 5.11: End-piece flex circuits for L0 (top) and L1 (bottom) for the silicon heater mock-up. The bar integrates the interfaces to contact the interposers. The 2 or 3 wings guide temperature and power lines away from the mock-up.

up is cooled by a gas flow between the two layers. The corresponding results are summarized in chapter 6.

5.4 Production of the silicon heater mock-up

The goal of the silicon heater mock-up construction is to verify that the requirements introduced above can be fulfilled by the manual construction approach. The developed tooling and the construction of the silicon heater mock-up are described in more detail in the appendix A.

This section focuses on the evaluation of the detector construction. The placement precision and glue thickness are analyzed in sections 5.4.1 and 5.4.2, and compared to the Mu3e requirements discussed in section 5.1. The spTAB procedure is evaluated and the observed issues are critically discussed in section 5.4.3. Finally, in section 5.4.4, the yield of the ladder construction is presented as well as some remarks on the module construction. Cooling studies performed with the silicon heater mock-up are presented in chapter 6.

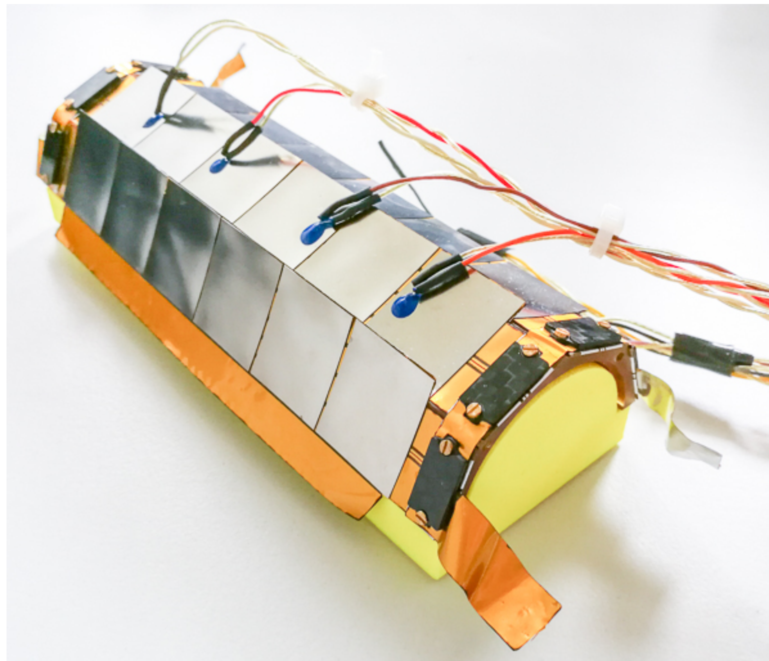


Figure 5.12: L0 tape heater module equipped with four resistive thermometers. [22]

5.4.1 Chip placement

Silicon heater dimensions

Although the silicon heater dimensions are specified to be $19.9 \times 23.0\,\text{mm}^2$, metrology measurements with a digital microscope revealed that the chips are wider by around 25 µm. Thus, the previously defined gap size between the chips of 100 µm shrinks down to 75 µm.

Chip bending

It is observed that the chip gap size decreases on the assembly tool by around 5 µm after releasing the vacuum. The chips are bent slightly by the vacuum and flatten back after vacuum release. Therefore, the nominal gap size during chip placement (with fixation by vacuum) is 80 µm.

Gap size measurements

The gap sizes are measured always close to the chip edge (Figure 5.14). A sketch of the chip pitch, the gap size, and the naming scheme for the two sides of the chip is shown in Figure 5.13. During chip placement the gap is measured with a digital microscope on the bond pad side of the chip. After placing all six chips, the gap sizes are measured also for the flap side of the ladder.

For the silicon heater production, the single chip placement procedure is considered as failed if the gap size at the bond pad side deviates from the nominal 80 µm

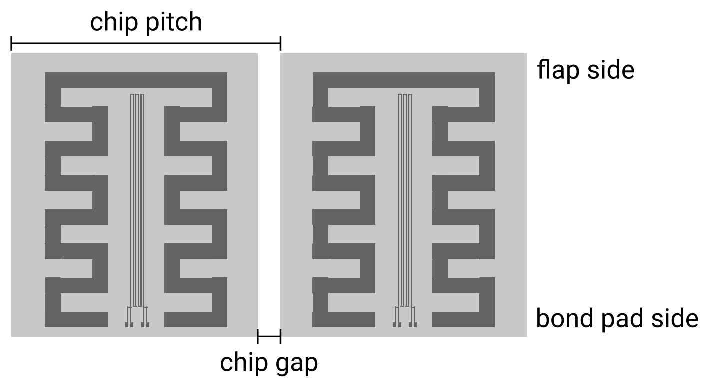


Figure 5.13: Sketch of the chip pitch and the chip gap of two silicon heater chips.

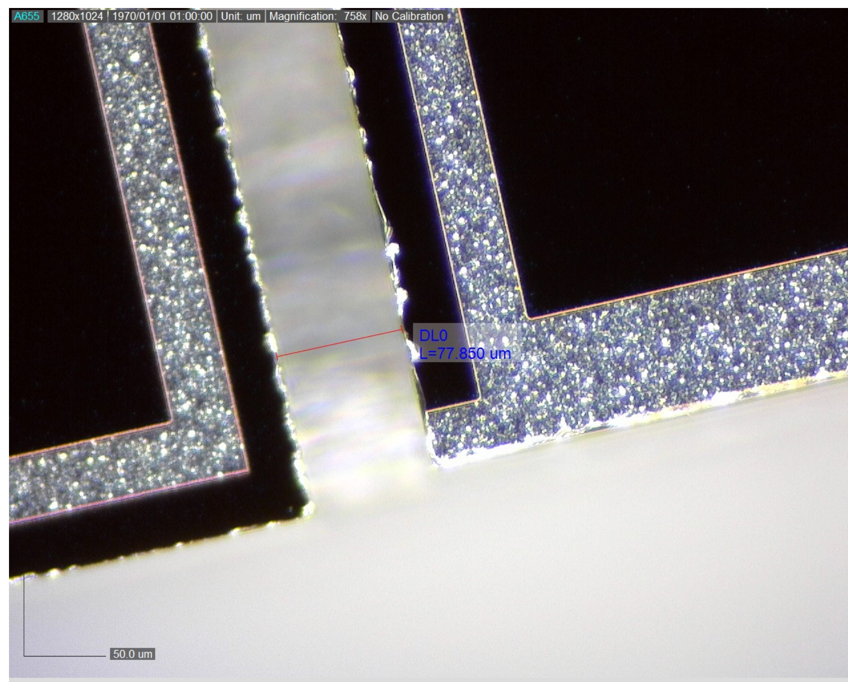


Figure 5.14: Silicon heater chip gap size measurement during chip placement.

by more than 5 µm. In this case, the chip is taken off the mounting tool and its placement is started from scratch. If multiple repetitions are needed, outliers are accepted to minimize the risk of damaging a chip. For the silicon heaters, the chip gap size is not as critical as for the final production regarding thermal contraction, since it is 80 µm wide compared to 40 µm in the final design.

The obtained gap size distribution for all silicon heater ladders excluding *pre-production*[1] is shown in Figure 5.15. An average gap size of (79.5 ± 3.7) µm is

[1] The first four silicon heater ladders manufactured are considered as pre-production. The correct silicon heater dimension and the chip bending were observed during their production. Also the glue application was under development. All ladders following show more uniform features and are considered as final production.

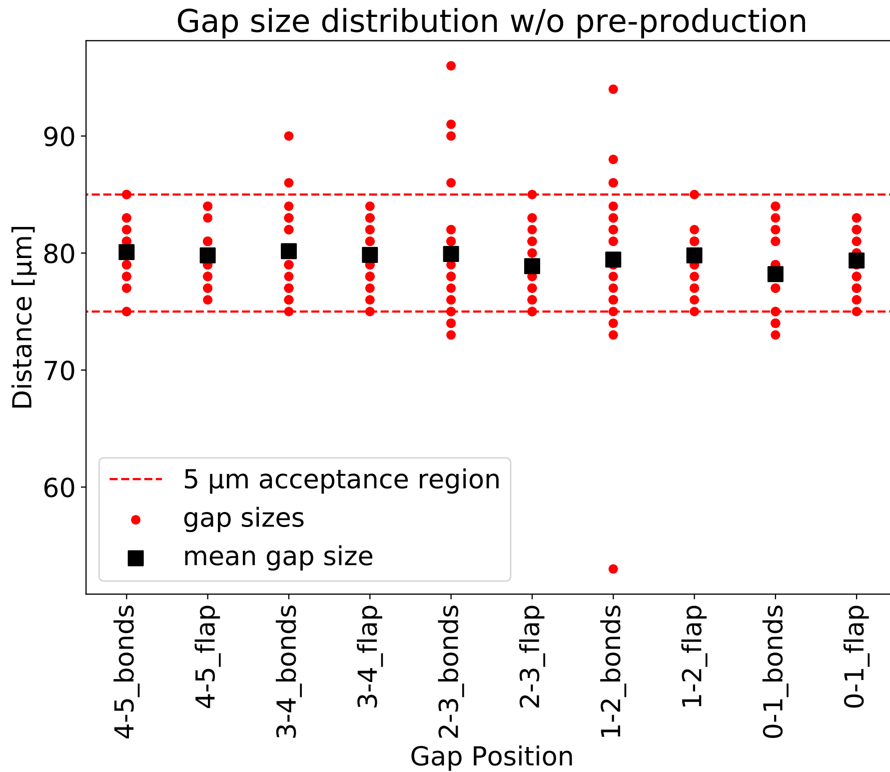


Figure 5.15: Chip gap size distribution for the silicon heater production measured on both the bond and flap side of the chips. The chip placement procedure resulted in some cases in outliers like for "1-2_bond". They are accepted for the silicon heater ladders if multiple repetitions do not improve the chip position to preserve the mock-up components from damage. Values are given excluding pre-production ladders.

achieved, which meets the requirements of (80 ± 5) µm. However, for around 5 % the gap size is <75 µm. For the final production, these outliers are not acceptable since they violate the safety requirements for thermal contraction, as outlined in section 5.1.1. The placement of chips for the final ladder production has to be more strict. This implies that, if the gap size is lower than the minimum, the chip placement must be redone until an acceptable gap size is achieved.

Chip rotation

For the silicon heater production, a systematic chip rotation is observed, which is caused by the imperfection of the right angle of the L-shaped slide used for the chip placement (cf. section A.2.1). In Figure 5.16, the resulting lateral displacement from one chip to another is shown. The average lateral displacement measured for the silicon heater production is (9 ± 3) µm. This is in agreement with the maximum allowed lateral displacement of 13.5 µm discussed in section 5.1.1.

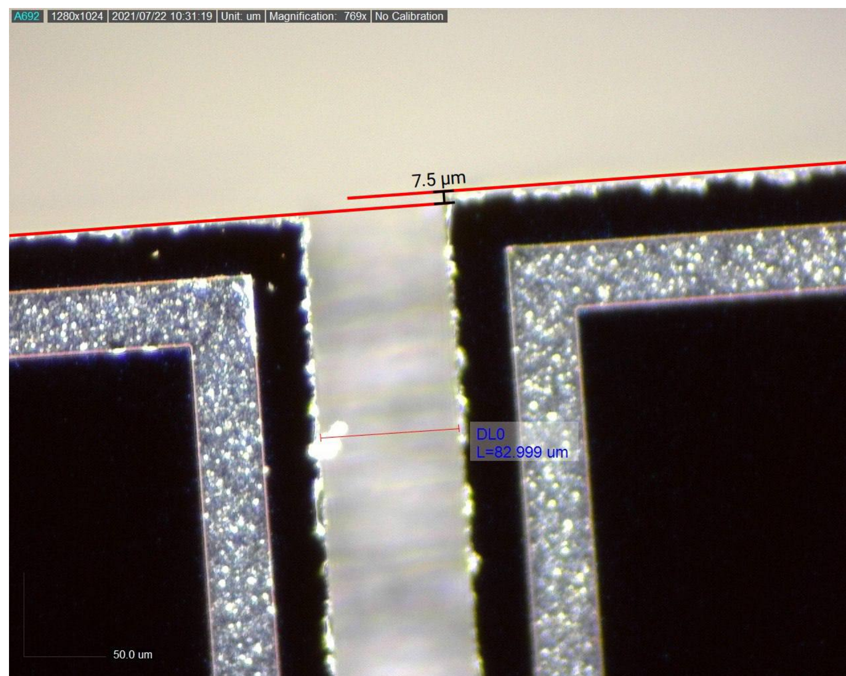


Figure 5.16: Lateral chip displacement due to chip rotation.

To further reduce the lateral displacement for the final production, the production of a few slides of higher precision is foreseen. The slide with the smallest systematic chip rotation is then taken for production.

5.4.2 Glue thickness

The chip gluing is done manually, as described in more detail in appendix A.2. During the silicon heater production, the glue thickness for every ladder produced is measured. This is to verify that an average glue thickness of 5 µm can be achieved.

This study is particularly important since this measurement is not foreseen for the final production. Scratches on the chip surface originating from the thickness gauge can be accidentally produced, since the measurement tool has direct contact to the measured material. For the heater chips, the substrate is not biased, which makes them resilient to such scratches. For the MuPix chips, however, the risk of such scratches must be avoided.

The thickness is measured for the heater chips, the HDI, and the glued ladder. Each heater chip is measured at five positions analogous to the gluing pattern. The HDI is measured at the corresponding positions. The heater chip thicknesses differ by up to 6 µm. The HDI thickness varies locally by up to 30 µm due to different layer stacks and additional glue at the vias between the two aluminum layers.

An example of such a measurement is shown in Figure 5.17. The thicknesses of the chips, the HDI, and the manufactured ladder are displayed. The last map shows the resulting glue thickness. Glue thicknesses lower than 10 µm are colored in green,

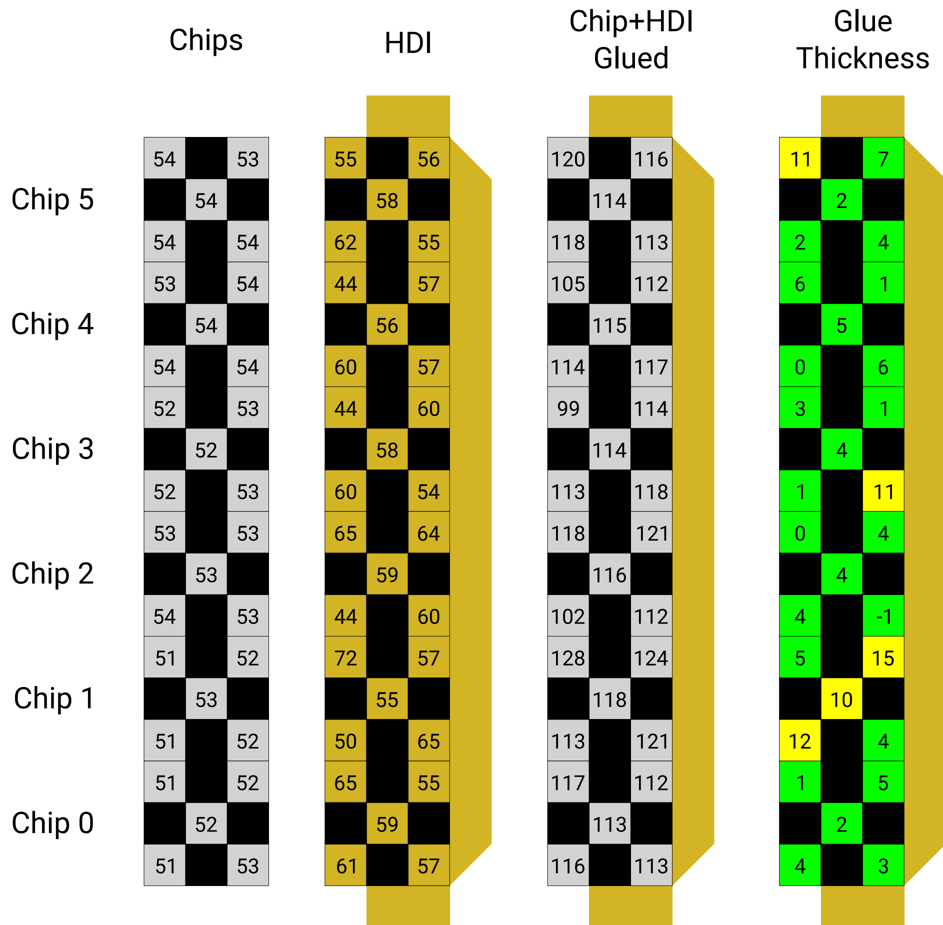


Figure 5.17: Thicknesses in µm of the silicon heater ladder components (chips & HDI), the ladder after gluing, and the resulting glue thickness (Ladder #24).

values higher than 10 µm but lower than 20 µm are colored in yellow. The average thickness of this particular ladder is (5 ± 4) µm.

In Figure 5.18, the evolution of the glue thickness during the ladder production is shown. After the pre-production ladders with larger thicknesses and uncertainties, the glue thickness was well under control and scattered around the aimed value of 5 µm. As the glue thicknesses have a large spread for the pre-production ladders originating from the ongoing training of the glue application, the corresponding ladders are excluded from the analysis. The resulting average glue thickness is found to be (5.3 ± 1.7) µm.

In addition, an analysis is performed on the glue distribution for each glue dot position. Figure 5.19 shows the numbering scheme used. In case of irregularities of the tooling or a systematic usage of different amounts of glue for different positions,

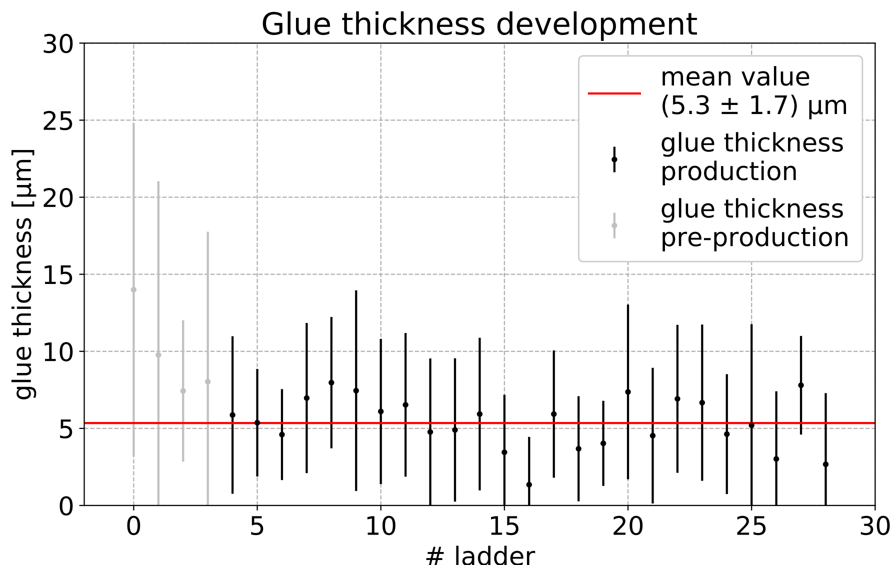


Figure 5.18: Glue thickness and standard deviation of all silicon heater ladders produced in chronological order. Mean value is given by excluding pre-production ladders.

systematic deviations are expected to be observed. In Figure 5.20, all measured thicknesses are plotted for each glue dot position. Negative values most probably originate from the compression of the HDI or dust particles present in the initial thickness measurement. Large positive outliers originate most probably from dust particles that were trapped in the glue. No obvious pattern is observed.

The measured thicknesses are satisfying, matching the aimed value of 5 µm. The manual gluing procedure is approved for the final ladder production.

5.4.3 SpTAB quality control

The spTAB QC includes the electrical test of all connections conducted directly after bonding and after transport of the modules to the FHNW and PSI, Switzerland, where the cooling studies are conducted. In addition, the mechanical impact of the bonding process on the silicon chips is monitored. On ladder level, the electrical connections are checked with a custom test board called *silicon heater tester*, which is shown in Figure 5.21. It consists of a mount for the interposer and the ladder, a current source, a 12-bit analog-to-digital converter (ADC) to measure the resistance via the voltage drop on the line, six 32-channel multiplexers to select the channels, and an Arduino board controlling the measurement. The stack of HDI, interposer flex circuit, interposer, and test board is pressed together by a dummy PCB plate which is fixed by screws. All $84^2 = 7056$ combinations are measured within a second.

For each half-ladder, a resistance map like in Figure 5.22 is obtained to validate if all spTAB are electrically contacting. The mapping of the interposer channels with

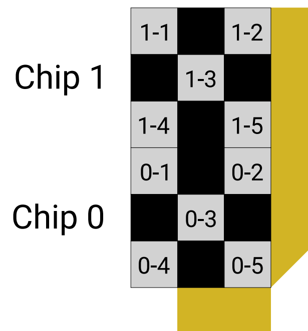


Figure 5.19: Numbering scheme of the glue dot position.

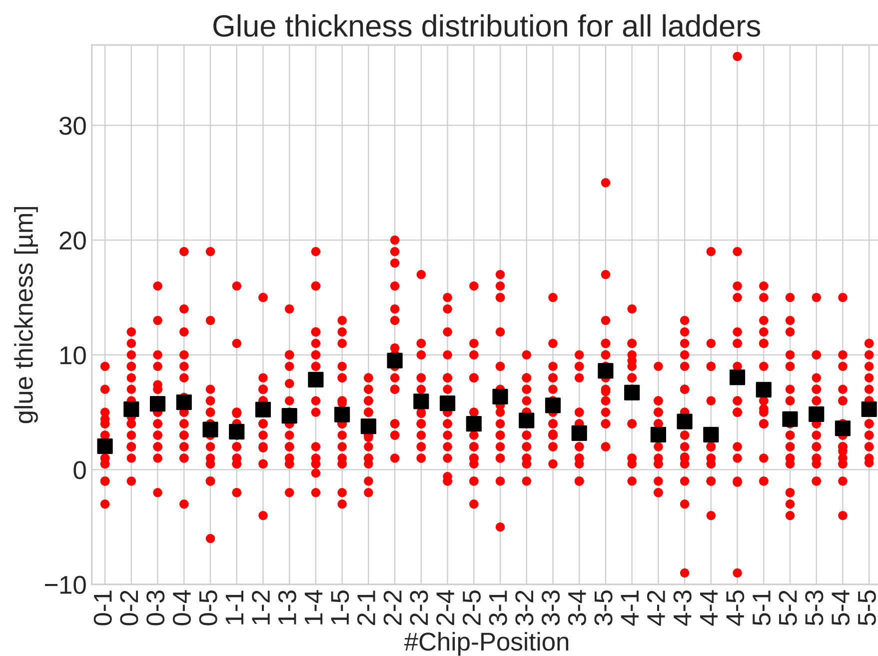


Figure 5.20: Glue thickness distribution for all glue positions on each chip (for numbering see Figure 5.19). Red dots show all measured glue thicknesses. Black squares show the average glue thickness for each position.

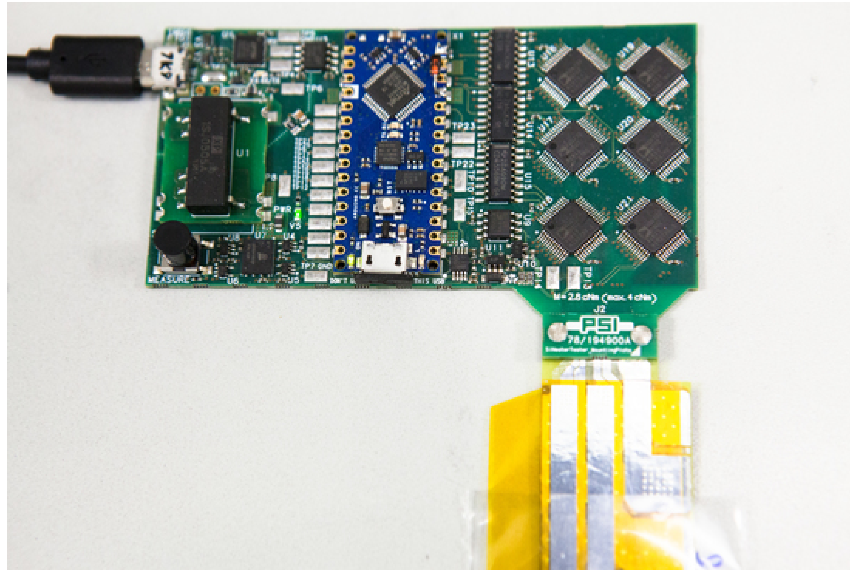


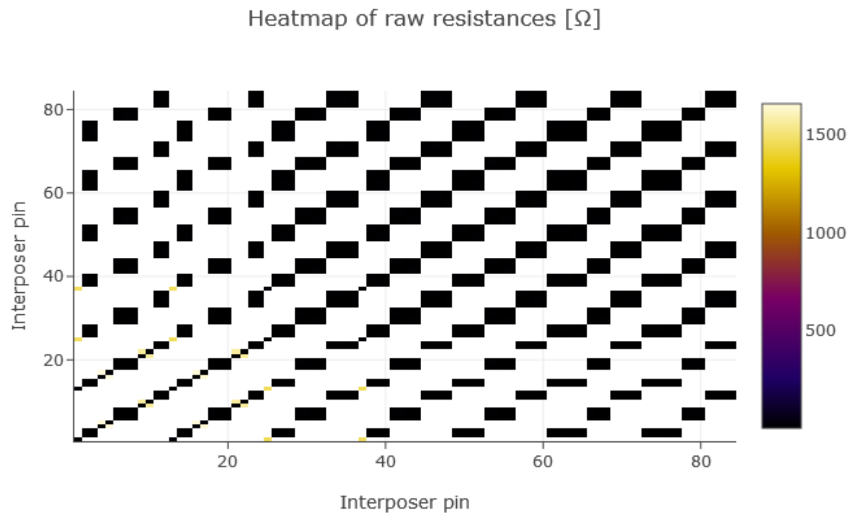
Figure 5.21: *Silicon heater tester* attached to a silicon heater ladder. The board is a custom development from the PSI electronic workshop.

the expected resistance is shown in Figure 5.23. From the HDI to the interposer flex circuit, the power and ground lines for each heater chip are connected to 12 bond pads each (see Figure 5.24), which results in groups of 24 interposer channels connected to each other through a low-ohmic resistance of $<10\,\Omega$. Four interposer channels are connected to one resistive thermometer. Each of these is connected to one channel through a low-ohmic resistance, and to two channels through a resistance of $\approx 1.25\,\mathrm{k}\Omega$. A non-contacting bond on the power line is recognizable in the map by a cross of infinite resistance values as in Figure 5.22b. This is only valid for connections at the interposer flex circuit-HDI interface, since the power lines are connected via 25 spTABs between HDI and chip in parallel (cf. Figure 5.24). A non-contacting bond for a thermometer connection is recognized for both interfaces due to missing redundancy.

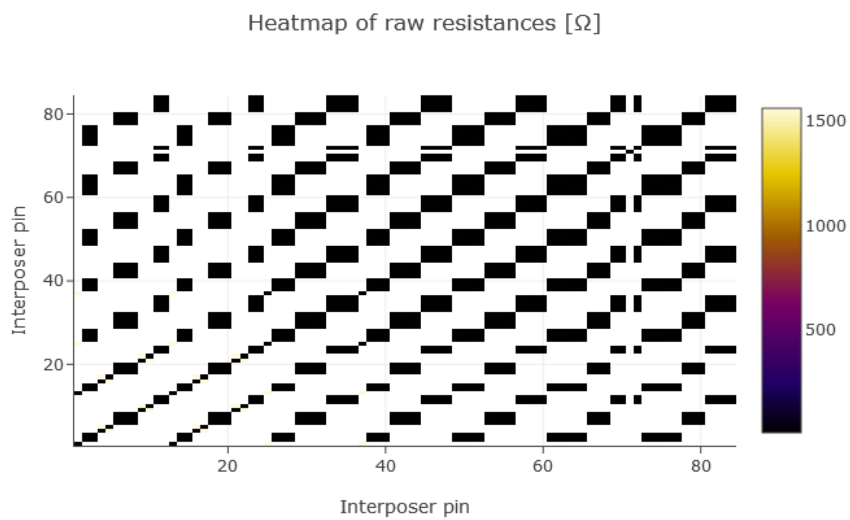
In the few cases of non-contacting spTABs, rebonding the trace was necessary. All such cases led to a contacting bond after rebonding. All non-contacting spTABs on the thermometer lines are observed at the interposer flex circuit-HDI interface. This indicates that the bond parameters used for spTAB on flex circuits are not optimal while the settings for spTAB on chip are suitable. This assumption is validated by the time dependent contact loss discussed next.

Time dependent contact loss

After module assembly, all heating and thermometer contacts are tested. For the silicon heater mock-up, in total 102 of 108 thermometers have been functional and 104 of 108 chips have been working for heating before transport from Heidelberg



(a) All bonds contacting.



(b) Channel 71 not contacting.

Figure 5.22: Silicon heater tester resistance maps for a half-ladder with good contacts, and a half ladder with one bad contact. The channel mapping is sketched in Figure 5.23

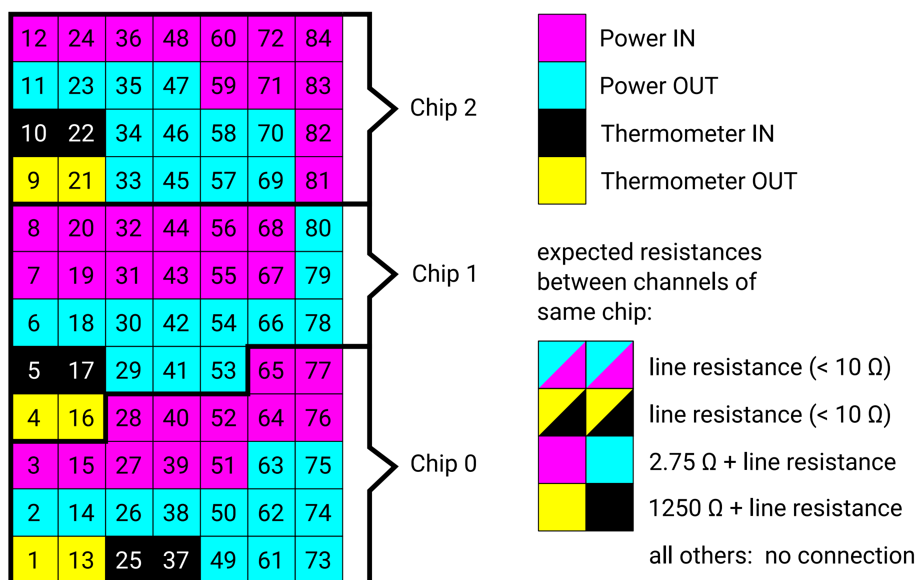


Figure 5.23: Interposer channel mapping for the US side of the silicon heater mock-up. Only channels of the same chip are contacting. The expected resistances are displayed in the right-bottom corner.

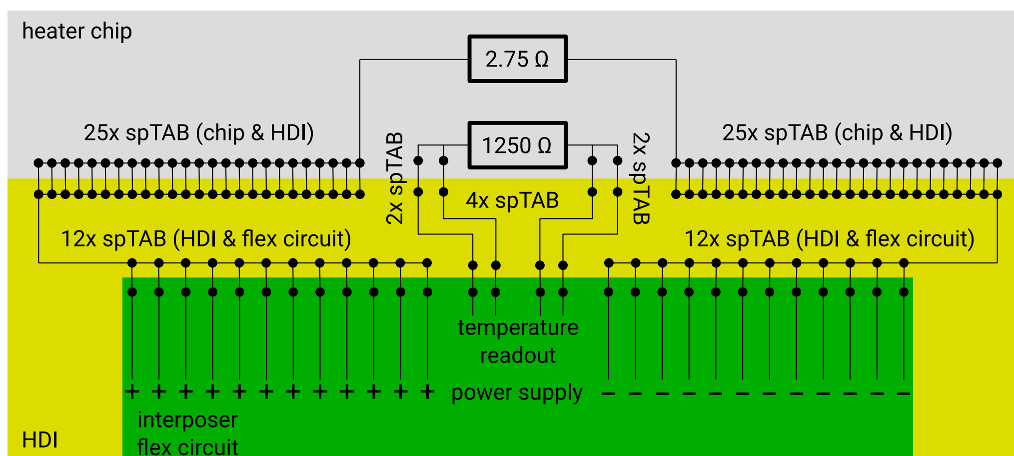
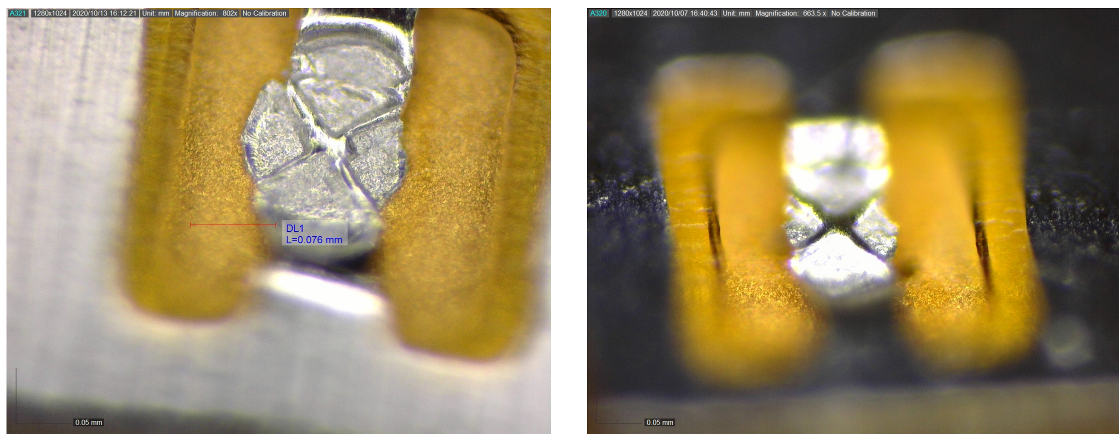


Figure 5.24: Sketch of the spTAB connections from interposer flex circuit to HDI, and from HDI to one silicon heater chip. For each chip, 28 interposer channels are connected: 12 + 12 for power, and 4 for the temperature readout.



(a) Proper spTAB. (b) Lift-off of an spTAB.

Figure 5.25: Examples of a proper spTAB connection and a lift-off of an spTAB. Both show an HDI on an interposer flex circuit.

to FHNW, Switzerland.[2] A few ladders with broken chips or broken temperature meanders are accepted due to limited availability of HDIs.

After transport, the contact quality is re-tested. A large degradation is observed. In total 52 of 108 thermometer connections are lost. The bonds of the interposer flex circuits are no longer accessible on module level (cf. Figure A.8). The analysis of the electrical connections is only possible by removing the ladders from the module. After inspection, the lost connections could be retraced to lift-offs of bonds, as shown in Figure 5.25b.

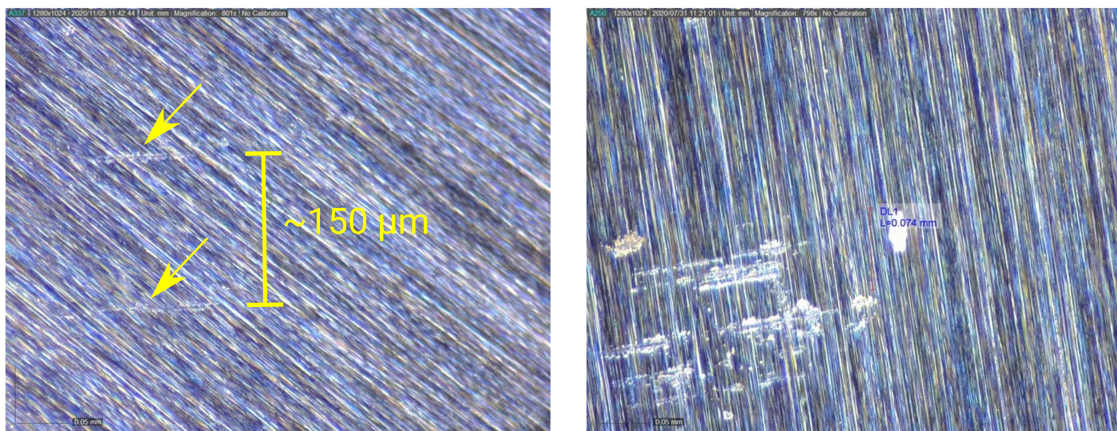
After re-optimizing the spTAB parameters, all ladders are rebonded and reassembled to modules. An additional polyimide strip substitutes the gluing flap that has been cutoff during disassembly. 100 out of 108 thermometers have been functional after the reassembly of the modules.

In summary, it can be concluded that the spTAB parameters for the initial production have been insufficient. The silicon heater tester graded most contacts as good. This test, however, has been carried out directly after bonding. Prior to the final detector production, a greater emphasis has to be placed on spTAB QC using HDI test structures. For pre-production samples, the spTAB quality is suggested to be monitored also after some weeks after the initial production.

Scratches on the rear side of the chips

For some silicon heater chips, cracks on the surface of the silicon substrate have been observed to develop over time on the ladders. To mitigate the risk of functional damage due to growing cracks cutting the aluminum meanders, they are covered by epoxy.

[2]Every chip has either a working thermometer or is working for heating - no double damages.



(a) Two scratches. Distance matches bond pitch.

(b) Scratches from ≈50 % higher bond force compared to (a).

Figure 5.26: Backside scratches caused by spTAB on silicon heater chips.

The origin of the cracks can be pinpointed to scratches on the chip backside (Figure 5.26) that are caused by spTAB. The scratches appear with the same pitch as the spTABs and are all oriented in the same direction. The chips are placed with the backside facing the bonding jig, a polished aluminum surface with vacuum holes. The ultrasonic energy of the bond wedge causes friction of the silicon substrate and the aluminum surface leading to this type of damage. To avoid scratches, a fine-polished bonding jig with lower surface roughness has been produced. Bonding tests on this optimized jig indicate no significant improvement.

A possible solution is to use a polyimide underlay that is placed between the bonding jig and the chips, which is made with cutouts for the vacuum holes. No scratches are observed for first preliminary tests with such an underlay. Prior to the final detector production, an extensive study with MuPix chips and spTAB test structures has to verify the feasibility of using a polymer underlay and approve new bonding parameters. Such a study is however beyond the scope of this thesis.

5.4.4 Ladder production yield

In total, 19 ladders went through the full QC procedure of the silicon heater production when excluding pre-production. Four QC grades are used to classify the ladders:

- A: fully-functional ladder - without limitations.
- B: functional ladder - minor limitations accepted, like no temperature readout for one chip.
- C: usable ladder for cooling tests - functionality comparable to A or B but with additional structural damage, e.g. broken off chip edges or other limitations that would lead to its exclusion when more material would be available.

- D: QC not passed - broken chip, interposer flex circuit gluing failed, or missing electrical connections.

Grade-A and grade-B ladders are both considered to have passed the QC. The non-functional thermometers of the grade-B ladders result from scratched-away aluminum of the thermometer meander. This is not induced by the manufacturing procedure but by the thickness measurement that is not foreseen for the final MuPix ladders. QC grades C and D are both considered as not passed. Some grade-C ladders, though, have to be used for the silicon heater mock-up due the limited amount of material for ladder production.

10 ladders are considered as fully functional (grade A). 3 ladders have one thermometer which is not readable (grade B). 3 ladders each are assigned with the grades C and D. The resulting yield is around 68 %, a satisfying number considering the manual production procedure and the fact that it was the first production of HDI-based ladders in our laboratory. The yield is expected to increase for the final production, since most discarded ladders originate from human handling errors or cracks from bonding in the chips. Production routines are developed to mitigate the former. The latter has to be fully excluded prior to production anyway.

The ladder production based on HDIs without a spacer layer emerged to be more prone to handling mistakes than for HDIs with a spacer layer. The ladders are less stiff and thus more difficult to handle. However, 3 out of 5 ladders, which went through the full QC procedure, passed the QC test. The yield is in an acceptable range, which opens the possibility to consider them as baseline for the vertex detector, which would further reduce the material budget by around 0.01 % X_0 per layer.

5.5 Summary and outlook

The mock-up production, particularly the silicon heater production, successfully demonstrated that the Mu3e vertex detector can be built with the present tooling for a manual assembly procedure. The chip placement shows an impressive precision of 4 µm in longitudinal and 3 µm in lateral direction which is competitive to robotic gantries. The glue thickness is well under control and reaches an average value of (5.3 ± 1.7) µm. Issues concerning spTAB, like contact loss of bonds at the interposer flex circuits and backside scratches on the heater chips, are understood and solutions are found. Prior to the final production, an extensive spTAB parameter validation is foreseen using the final materials.

The ladder production yield of around 68 % is within the aimed expectations and at a level where yield has no significant negative impact on the production time and material costs. This makes the manual production approach not only very precise but also a reliable and cost-effective option that competes with automatic approaches for small-scale projects.

In the near future, a small-scale MuPix10 HDI ladder program with 10 ladders is going to verify the above findings and check the spTAB quality before final module

production with MuPix11 chips. The associated electrical tests will also study the signal transmission quality for ladders with and without polyimide spacer layer, which will lead to the final decision for the layer stack.

Helium cooling 6

This chapter presents the results of the cooling studies with the thermal-mechanical mock-ups of the Mu3e vertex detector. In the beginning, the helium cooling plant prototype is introduced. Some remarks on its general operation and the mass flow measurement with Venturi tubes are given.

Results originating from the tape heater mock-up cooling studies are briefly summarized, see [70] for more details.

The main focus is on the measurements performed with the silicon heater mock-up, which give a detailed and realistic picture of the cooling capabilities of the foreseen cooling system. The measurement setup and the calibration of the on-chip thermometers of the heater chips is described. The thermal behavior for different heat loads and mass flows is analyzed. Transient studies for the thermalization after powering on and off the detector are described. The thermostatic results are compared to simulation studies carried out by Marin Deflorin.

6.1 Helium cooling plant prototype

The helium cooling plant prototype is used for the cooling studies of the silicon heater mock-up presented in section 6.4, and for the cooling of the vertex detector prototype described in part IV. It is a simplified version of the Mu3e helium cooling system described in section 4.4. It provides only a single flow channel with a mass flow of 2 g/s. The flow is supplied by a miniature turbo compressor. The gas is cooled by a plate heat exchanger. The pressure, temperature, and mass flow are monitored for the inflow and outflow of the compressor. A control system allows for different operating conditions and also acts as safety system for the turbo compressor. No gas purification system is integrated. Beyond that, the prototype plant has the same working principle as the final cooling system.

6.1.1 Setup

The cooling plant prototype is mounted in a rack, as shown in Figure 6.1. A simplified sketch is shown in Figure 6.2. The warmed-up helium enters the plant, a 1 m long straight tube ensures uniform flow before the Venturi tube (section 6.1.3),

which measures the mass flow. After the turbo compressor, the helium is cooled in a plate heat exchanger and exits the plant through a second Venturi tube for a redundant mass flow measurement. Between inflow and outflow, a bypass is located that can be promptly opened by pressurized air. The tube diameter is constantly at 50 mm to minimize pressure differences, matching the Klein Flansch - ISO standard (KF) 50. The cross section is only reduced inside the compressor and the heat exchanger. An oxygen sensor is integrated into the system, which is located as far as possible from the plant at the outflow of the mock-up/prototype. This increases the allowed response time in case of a leak at the detector until the more dense gas reaches the compressor, which requires to throttle it down.

The control and monitoring of the system is done by a Raspberry Pi connected to an SCS-3000 unit[1]. This unit measures all analog sensor signals and digital statuses of the plant. A simple MIDAS [76] front-end monitors all relevant parameters of the system and serves as a control panel for the compressor operation.

6.1.2 Turbo compressor

A custom turbo compressor prototype from Celeroton [77], designed to provide a helium mass flow of 2 g/s, is used for the prototype plant. It comes with a gas bearing and can be operated in a broad gas temperature range of -30 to 70 °C. The maximum rotational frequency is 245 krpm. The resulting mass flow depends on the pressure ratio between inflow and outflow. The performance map of the turbo compressor is shown in Figure 6.3. It can be seen that a high pressure difference reduces the efficiency of the compressor performance. Therefore, it is recommended to keep the pressure ratio at a feasible minimum. This is reached mainly by using large tube diameters.

The performance strongly depends on the gas density. For higher gas densities than helium like for air, the compressor has to be throttled down. The control unit automatically adjusts the maximum allowed rotational frequency of the compressor in case of an air leak to safeguard the compressor. It depends on the measured oxygen concentration in the system, assuming a gas mixture of only air and helium.

Surge protection

A compressor surge occurs when the operation point in Figure 6.3 crosses the surge limit. This is the case when the pressure difference at the compressor is above the limit to provide stable gas flow. Thus, opening a bypass valve results in the recovery of the gas flow, since the pressure difference drops to a minimum. It is important to apply this surge protection as fast as possible to effectively protect the compressor from damage. A possible cause for surge is that the gas flow is blocked at the experiment.

[1] SCS-3000 is a PSI developed control system. https://www.psi.ch/sites/default/files/import/ltp-electronics/WwwDocumentsEN/User_Manual_SCS3000_RevB_V1.1.pdf

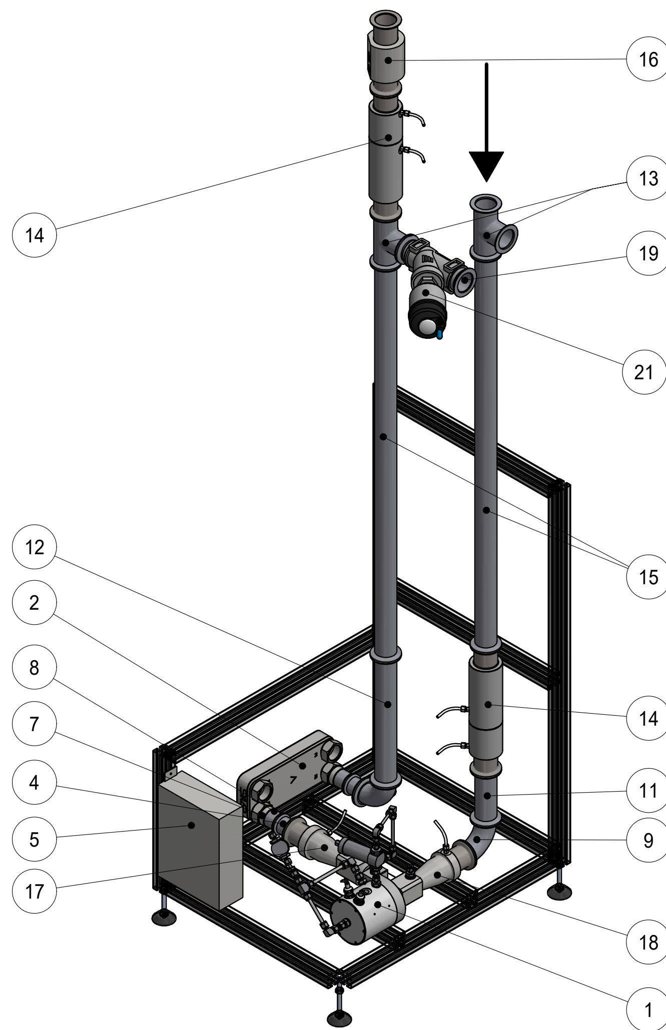


Figure 6.1: Rack for the helium cooling plant prototype based on a miniature helium turbo compressor. The main components are: (1) a miniature turbo compressor, (2) a plate heat exchanger, (5) the control unit, (12) Venturi tubes, (16) a measuring station for pressure & temperature, (17/18) a diffuser/confuser equipped with pressure and temperature sensors, and (21) a safety valve. [75]

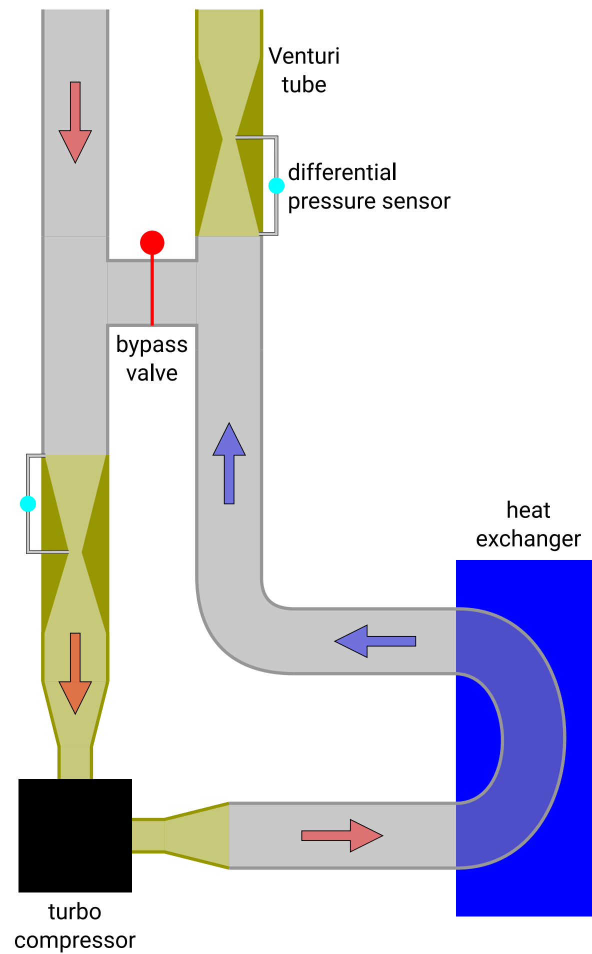


Figure 6.2: Sketch of the helium cooling plant prototype. Helium is circulated by a turbo compressor and cooled by a plate heat exchanger. The mass flow is measured by two Venturi tubes. A bypass valve can be opened at the plant.

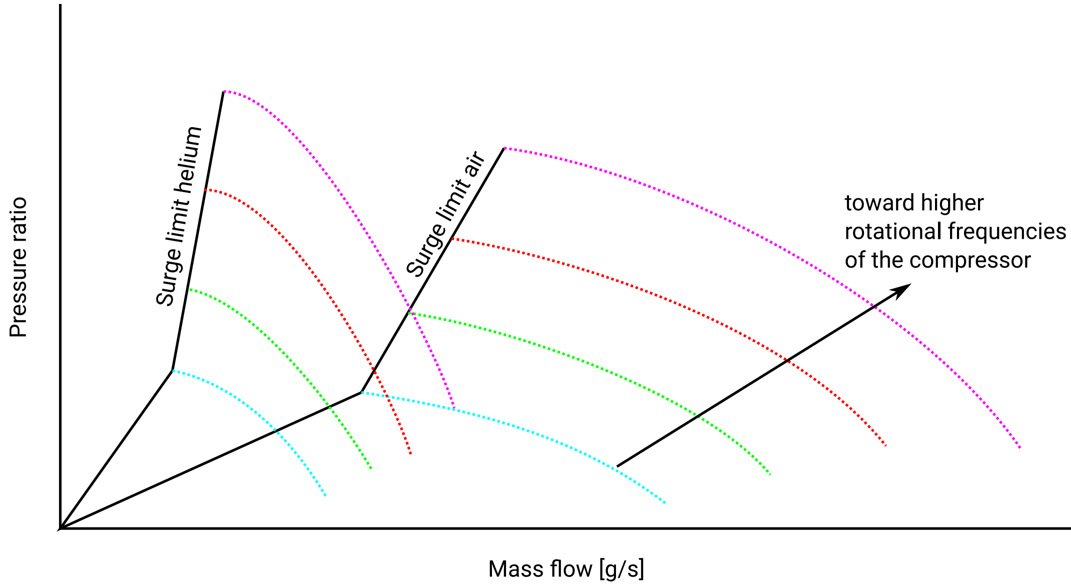


Figure 6.3: Sketch of a typical performance map for helium (left) and air (right) operation of a miniature turbo compressor. The mass flow depending on the pressure ratio is plotted for different rotational frequencies. The black dashed lines describe the surge limits. Operation in the area left of it results in a compressor surge.

In the plant, a potential surge is detected by monitoring constantly the mass flow and the differential pressure in the system. If the operation point of the compressor passes the surge line in the performance map (Figure 6.3), the bypass valve is automatically opened.

6.1.3 Mass flow measurement using Venturi tubes

The helium mass flow is measured by two custom Venturi tubes (Figure 6.4). Inside these brass tubes, the tube diameter of 50 mm is decreased to half the value. This results in a pressure difference between large and narrow tube diameter. The pressure difference Δp depends directly on the mass flow $\dot{m}$, as described by equation 6.1 [78], which is an approximation for incompressible flows:

$$\dot{m}^2 = \Delta p \cdot \rho \cdot \frac{2A_1^2}{\left(\frac{A_1}{A_2}\right)^2 - 1} \tag{6.1}$$

With $D_2 = D_1/2$, $D_1 = 50\,\text{mm}$, and $A_1 = \pi \cdot (D_1/2)^2 = 20.11\,\text{cm}^2$, equation 6.1 is reduced to:

$$\dot{m}^2 = \Delta p \cdot \rho \cdot \frac{2}{3}\left(20.11\,\text{cm}^2\right)^2 \tag{6.2}$$

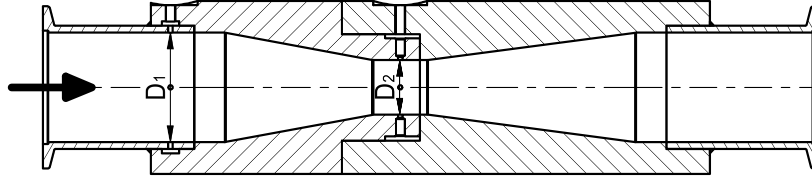


Figure 6.4: Technical drawing of the Venturi tube used for the mass flow measurement in the helium cooling plant at 2 g/s. The diameters are $D_1 = 50\,\mathrm{mm}$, and $D_2 = 25\,\mathrm{mm}$. [75]

This relation is only valid for a uniform flow inside the tube, which thus is required for a Venturi tube. The uniform flow is ensured by long straight tubes at the inlet and a gentle slope inside the Venturi tube.

For a helium mass flow of 1 g/s to 2 g/s, a pressure difference Δp of the order of 30 Pa to 70 Pa is expected. This low pressure difference inside the Venturi tube makes the assumption of an incompressible flow reasonable. Small silicon tubes connect the boreholes of the Venturi tube to a differential pressure sensor which is powered and read out by an SCS-3000 unit.

6.2 Cooling studies with the tape heater mock-up

The cooling studies conducted with the tape heater mock-up are the first thermal measurements that account for all geometrical details of the vertex detector. As mentioned previously, only a helium flow inside the gap of L0 and L1 is provided, according to the old baseline design. The measurements are paired with simulations presented in [70], which predict the necessity of an additional flow channel around L1.

The measurements are performed at a test stand at the FHNW, Switzerland. A detailed description of the measurement and the analysis is given in [70]. The mock-up is mounted in a mini-cage (cf. section 6.3). In contrast to the silicon heater mock-up, the presented measurements are carried out by supplying helium directly from a compressed helium gas bottle and not by the helium cooling plant prototype. The mass flow is set to 2 g/s for the measurement. The temperature can be read out by several thermocouples glued onto chips in both L0 and L1 and by an infrared camera. For the camera measurement, one module of L1 is painted by black coating with an emissivity of 98 %. The applied heat dissipation is around $400\,\mathrm{mW/cm^2}$. The result from the infrared camera measurement is shown in Figure 6.5.

The highest temperatures reached have a $\Delta T = 70\,\mathrm{K}$–$75\,\mathrm{K}$ to the inlet temperature. The hot area indicates the presence of a backflow region, which is observed also in the computational fluid dynamics (CFD) simulations carried out in [70]. The high temperatures above the limit of 70 K are reached for uniform heating. Considering an even hotter periphery for the MuPix chips, the cooling with one flow between

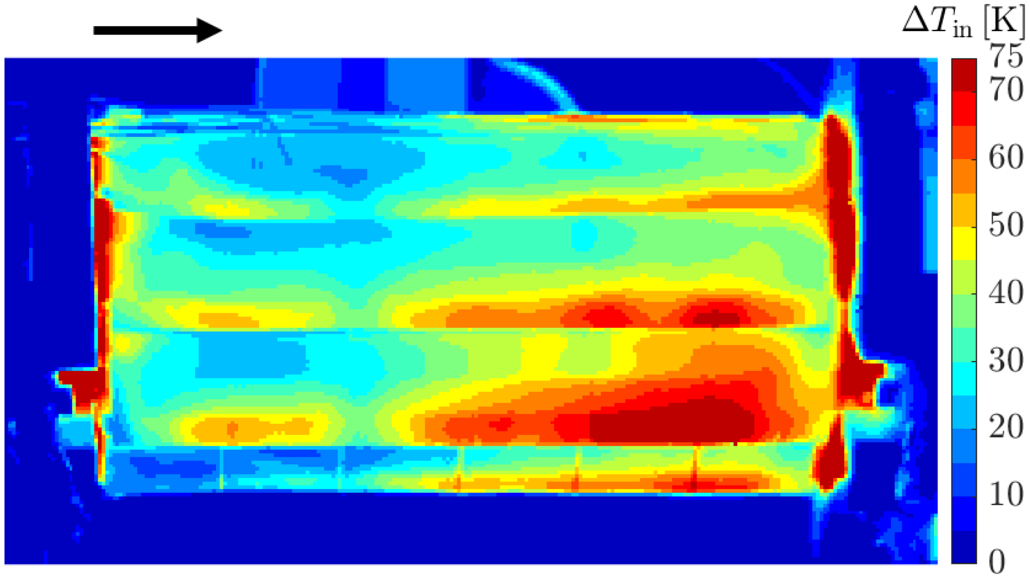


Figure 6.5: Temperature measurement of the tape heater mock-up with an infrared camera. Heat dissipation of 390 mW/cm^2, the arrow indicates the flow direction. The temperature difference to the inlet temperature is displayed. The highest temperature is reached on Ladder 3 of L1. [70]

L0 and L1 is not sufficient for Mu3e. The findings of this measurement have led to a redesign of the supply geometry of the helium gas for the vertex detector and an additional flow channel around L1.

The updated geometry as well as a series of more detailed measurements, including the transient temperature behavior and different mass flows, is then studied with the silicon heater mock-up. It features a more granular temperature readout with integrated thermometers on every chip. The heat is produced directly on the silicon substrate, which makes the silicon heater mock-up favorable for the detailed investigations presented in section 6.4.

6.3 Cooling setup for the silicon heater mock-up

6.3.1 Mounting of the mock-up

The silicon heater and tape heater mock-ups are both mounted in a so-called *mini-cage*, which is shown in Figures 6.6 and A.12. This mini-cage mimics the support of the central part of the Mu3e experiment. It integrates the detector mounts for the vertex detector, the outer pixel layers, and the SciFi detector. For the silicon heater mock-up, the mini-cage is located inside an acrylic glass tube (Figure 6.6) equipped with two flange plates sealing the helium volume. Helium is provided via tubes from the flange plates to the gas distribution rings. Cables for powering and

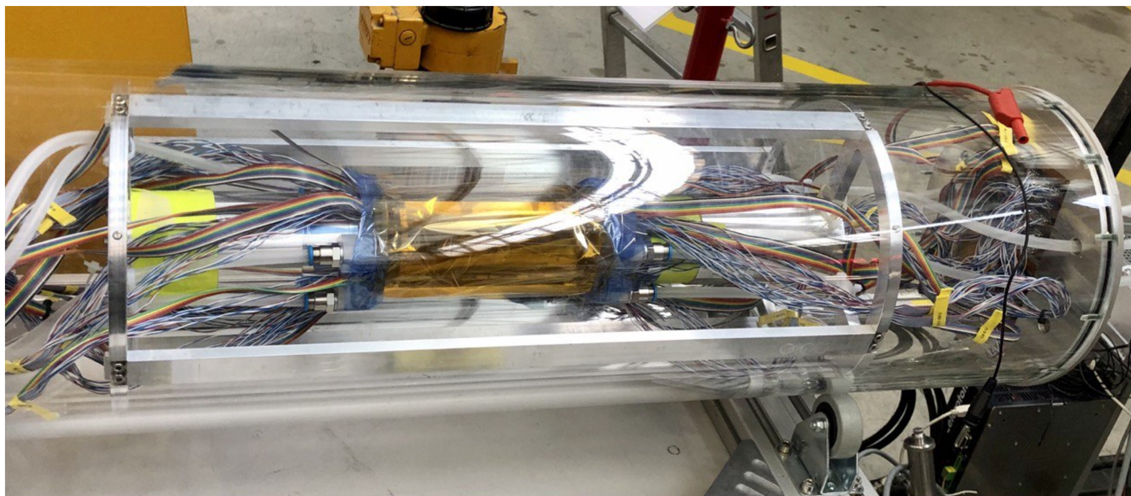


Figure 6.6: Acrylic glass tube containing the mini-cage with the silicon heater mock-up mounted.

reading out the mock-up are guided along the cage from the end-piece flex circuits to the flange plates, where they are connected to a glued-in interconnection board.

6.3.2 Powering and readout

Ribbon cables are directly soldered to the end-piece flex circuits connecting power and the temperature readout of the mock-up. A Eurocard-sized PCB is glued into the flange plates (Figure 6.7). This board serves as an interconnection for both power and readout from the inside to the outside of the tube.

All power and temperature cables are connected to the pins of the board. At the outside, the pin connector interface, shown in Figure 6.8, allows to select the thermometers of choice and power the mock-up. With a set of jumpers, each half-ladder can be individually turned on and off.

Powering scheme

The mock-up is powered with a HAMEG HMP4040 power supply, which provides a constant current to the silicon heaters. The heat load of the silicon heater chips is defined by the current, which is not affected by resistive losses on the supply lines. The standard settings for the cooling studies are powering all half-ladders with either 1.65 A or 2.1 A. For the designed heating resistance of the heater chips of 3.24 Ω, this would result in 215 mW/cm^2 and 350 mW/cm^2 nominal heat dissipation on the chips, respectively. However, as mentioned in section 5.2.2, the true heating resistance value is $(2.75 \pm 0.05)\,\Omega$, which reduces the nominal heat dissipation to 182 mW/cm^2 and 295 mW/cm^2, respectively. The US and DS side of the mock-up are electrically separated and powered by individual channels of the power supply. In case of a non-functional chip, a wire wound resistor of 3.3 Ω is connected on the

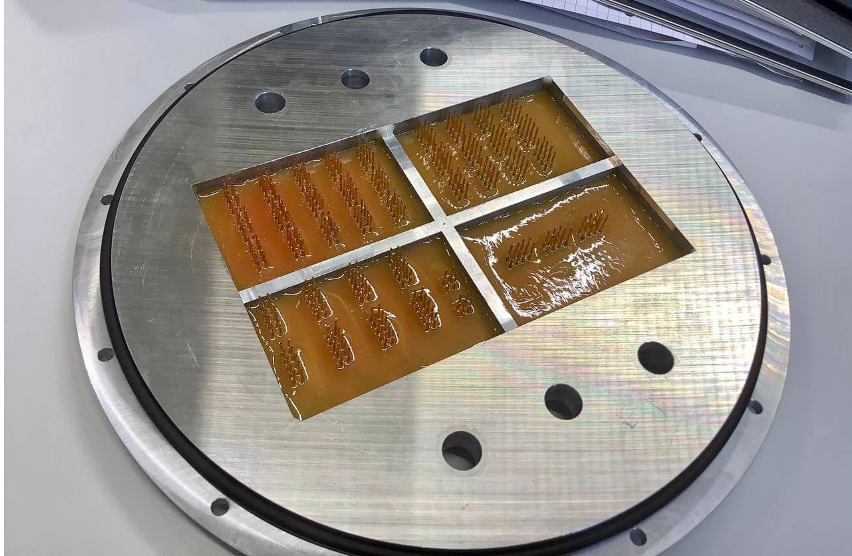


Figure 6.7: Flange plate for the acrylic glass tube hosting six feedthroughs for the helium tubes. The electrical connections are realized by pin connectors. The PCB is sealed with epoxy.

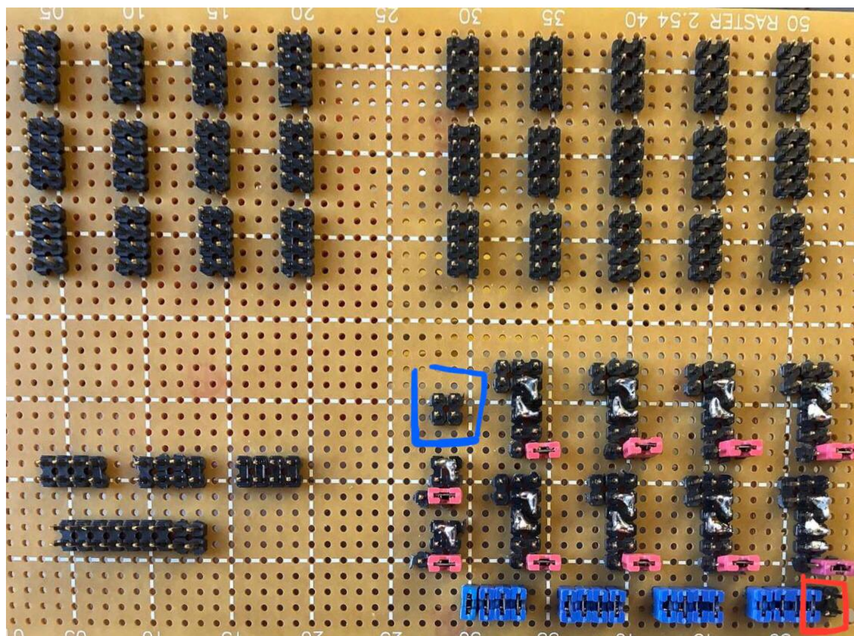


Figure 6.8: Interface PCB glued into the flange plate (Figure 6.7) for the silicon heater mock-up. Top half are the pin connectors for the 4-wire temperature readout for each sensor. Bottom-right quarter is the power connection: The red and blue squares indicate +/− connection to the power supply. The red and blue jumpers select which half-ladders are powered. Bottom-left quarter are spare electrical connections.

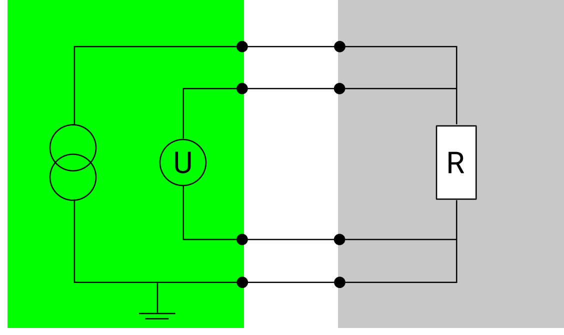


Figure 6.9: Schematic of the 4-wire sensing method to read out the silicon heater temperature. A constant current source is connected by two wires to the thermal resistance R. Another two wires are connected to measure the resulting voltage U.

interface PCB in parallel to the remaining chips of the half-ladder to balance the current. It takes into account the resistance on the supply line to the chip.

Temperature readout

The temperature readout is done via an SCS-3000. The device is equipped with measurement cards for temperature reading via 4-wire sensing, as sketched in Figure 6.9. The measurement cards are specified for reading out standard Pt-1000 thermometers. Thus, a software conversion has to be applied to obtain the correct temperature when reading the aluminum thermometers on the heater chips. This conversion is outlined below.

The thermal resistance of a Pt-1000 can be described by the following second order polynomial:

$$R_{Pt}(t) = R_0 \cdot (1 + AT + BT^2) \tag{6.3}$$

with $R_0 = 1\,\mathrm{k\Omega}$, and $A = 3.9083 \times 10^{-3}\,°\mathrm{C}^{-1}$ and $B = -5.775 \times 10^{-7}\,°\mathrm{C}^{-2}$ as the temperature coefficients of platinum [79]. In turn, the thermal resistance of the silicon heater chips is described by:

$$R_{Al}(t) = R'_0 \cdot (1 + \alpha\ \Delta T) \tag{6.4}$$

with $\alpha = (4.17 \pm 0.02) \times 10^{-3}\,°\mathrm{C}^{-1}$ as the temperature coefficient measured in [69] and R'_0 as reference resistance at $0\,°\mathrm{C}$.

To obtain the conversion between the true temperature T and the output temperature T_{SCS} of the SCS-3000, the reference resistance $R_{0,i}$ of each chip i has to be measured. For a known true chip temperature T_{ref}, e.g. the environmental temperature at zero power, this reference resistance $R'_{0,i}$ of each chip is derived from:

$$R'_0 = \frac{R_0 \cdot (1 + AT_{SCS} + BT_{SCS}^2)}{1 + \alpha\ T_{ref}} \tag{6.5}$$

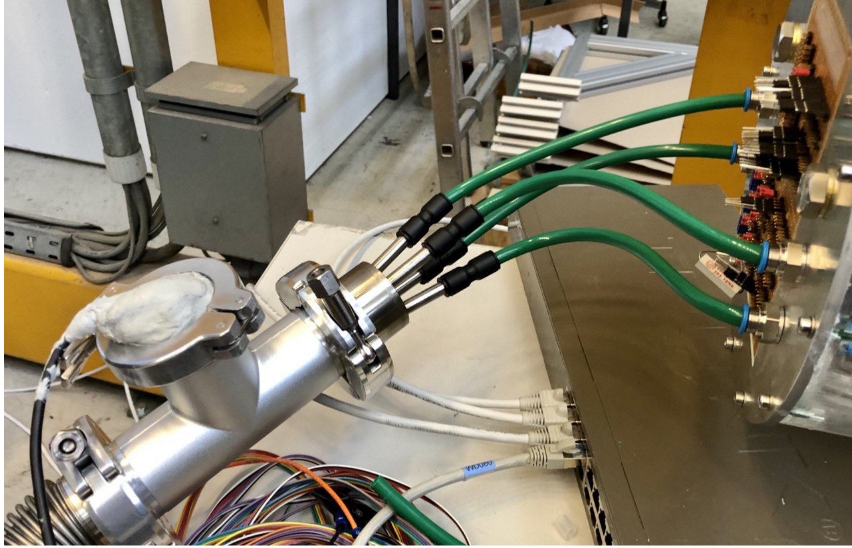


Figure 6.10: Helium flow adapter from KF40 to 4 × 8 mm tubes. Left of the adapter, the T-piece containing the oxygen sensor is visible.

The precision on the temperature T_{ref} and on α defines the uncertainty on the temperature measurement, as will be discussed in section 6.4.2. With R'_0 known, T_{SCS} can be converted to the true temperature T by:

$$T = \frac{1}{\alpha}\left(\frac{R_0(1 + AT_{SCS} + BT_{SCS}^2)}{R'_0} - 1\right) \tag{6.6}$$

6.3.3 Gas connection to the helium plant

The flange plate shown in Figure 6.7 is equipped with feedthroughs for the gas tubes. The gas distribution rings of the silicon heater mock-up have 4 inlet/outlets with connectors for 8 mm outer diameter tubing. With an inner tube diameter of 6 mm, this provides a rather small cross section of 113 mm^2 compared to around 200 mm^2 in the final system. The tubes are guided along the mini-cage toward the flange plate. On the outside, the tubes are connected via a custom adapter piece to KF40 tubing (Figure 6.10).

At the outflow, this adapter is directly connected to a KF40 T-piece containing the oxygen sensor to maximize the distance between sensor and turbo compressor. On both sides, KF40/50 corrugated tubes of a few meters length are connecting the mock-up setup to the helium plant. Inflow and outflow tubing can be swapped at the helium adapters to study the cooling for nominal and inverted flow configurations.

6.3.4 Helium filling

The helium bottle for filling the plant and the mock-up setup is connected by a T-piece and a valve at the inlet of the helium plant prototype. Helium is constantly flushed during the measurements to compensate for small leaks. A gas outlet is realized by a 10 m long tube with a small diameter of 2 mm connected to one feedthrough of the flange plates. The small cross section and the length of the tube inhibit the diffusion of air into the system. The system is slowly filled with helium while operating the turbo compressor at a reduced rotational speed. As soon as the oxygen sensor measures a concentration of less than 1 %, the turbo compressor is brought to the final rotational speed.

6.4 Cooling studies with the silicon heater mock-up

The silicon heater mock-up is tested in a series of detailed thermal measurements. These studies are enabled by the helium cooling plant prototype being finalized in parallel to the mock-up construction. This way, a continuous circulating helium flow can be used for days. The corresponding cooling studies are carried out mainly by powering on and off the mock-up and recording the temperature data from the resistive thermometers on the heater chips. In each measurement, three thermometers can be read out at once, which corresponds to all chips of a half-ladder. To characterize the full mock-up, $108/3 = 36$ measurements have to be conducted. The temperature values are always given as *temperature difference* ΔT:

$$\Delta T = T_{measured} - T_0 \tag{6.7}$$

with $T_{measured}$ as temperature in the powered state and T_0 as temperature before powering. This way, T_0 corresponds to the inlet temperature.

The mock-up is powered by providing a constant current to all half-ladders. In case of a measurement series including multiple heat dissipation values, the current is increased stepwise starting with zero power. The helium flow is always kept on and in the same conditions independent of the power status of the mock-up.

Through thermal changes of the resistivity of the heater chips while heating, the heat dissipation of each chip varies. This induces non-uniformities concerning the heat dissipation for the mock-up. To translate the measurements to a uniformly heated system, corrections are applied on the measured raw data, which are presented in the next section. It is followed by a discussion about measurement uncertainties of the set-up including electrical noise, temperature shifts of the environment, and calibration offsets.

The presented measurements are transient studies of the heating and cooling of the mock-up, temperature maps for the thermalized mock-up for nominal heat dissipations of $182\,\mathrm{mW/cm^2}$ and $295\,\mathrm{mW/cm^2}$, the temperature-to-power relation

for one ladder of L0 and L1 each, and the mass-flow dependent temperature change of the mock-up.

The heat dissipation values were chosen on the basis of the nominal heating resistance of the heater chip, which was found to be lower on the physical chips. The aimed values to measure were 215 mW/cm^2 and 350 mW/cm^2. A heat dissipation of 215 mW/cm^2 represents a scenario comparable to the initial operating conditions of MuPix10 chips used in the laboratory. A heat dissipation of 350 mW/cm^2 represents the specification limit for the MuPix chips set by the cooling system[2]. The findings from the temperature-to-power relation studies allow to translate the measurement results to the aimed heat dissipation values.

6.4.1 Corrections of the effective heat dissipation

The silicon heater mock-up is heated by providing a constant current. From the resistance of a heater chip of $R_0 = (2.75 \pm 0.05)\,\Omega$, the resulting heat dissipation is retrieved from $P = R \cdot I^2$. Three heater chips are powered in parallel. This way, the effective resistance of a half-ladder is $R_{HL} = R_0/3 \approx 0.92\,\Omega$. This results in a heat dissipation of 182 mW/cm^2 or 295 mW/cm^2, when a current of 1.65 A or 2.1 A is applied, respectively.

The resistance and thus the true heat dissipation of each chip, however, is dependent on its temperature. Different chip temperatures on a half-ladder result in a non-uniform current flow. In addition, a constant effect of the finite HDI resistances has to be taken into account for the different chip positions. The corrections for all these effects are discussed below. The resulting correction factors are presented.

Thermal resistance correction

The resistance of the silicon heater chips changes with temperature. It depends on the temperature coefficient $\alpha = (4.17 \pm 0.02) \times 10^{-3}\,°\mathrm{C}^{-1}$ of the aluminum meander (cf. section 6.3.2), as described by:

$$R(T) = R_0(1 + \alpha\Delta T) \tag{6.8}$$

Therefore, a chip with a higher temperature dissipates more heat with the same current provided. As an example, the resistance of a heater chip with $\Delta T = 50\,\mathrm{K}$ increases by around 20 % increasing the heat dissipation by the same amount. Thus, the thermal resistance change is a significant effect that has to be considered in the analysis of the temperature measurements. The correction factor f_r to obtain the true heat dissipation is defined as:

$$f_r = (1 + \alpha\Delta T) \tag{6.9}$$

[2] 400 mW/cm^2 are regarded as conservative limit (cf. section 4.4) for the full pixel detector including resistive losses on the supply lines. The quoted 350 mW/cm^2 are dissipated on the chips only.

Thermally dependent current changes

Three heater chips are powered always in parallel for the silicon heater mock-up, as indicated in Figure 6.11. A temperature gradient is expected along a ladder for the present cooling scheme. The thermal dependent resistances lead to different currents flowing through each heater chip. This partially compensates the above effect since the highest current flows through the coldest chip.

The correction factor $f_{c,i}$, to compute the true heat dissipation value of chip i on a half-ladder, is given by:

$$f_{c,i} = \frac{1}{1+\alpha T_i} \cdot \frac{3}{\frac{1}{1+\alpha T_0} + \frac{1}{1+\alpha T_1} + \frac{1}{1+\alpha T_2}} \tag{6.10}$$

The correction factor is applied on the current. Thus, the heat dissipation depends quadratically on $f_{c,i}$.

HDI resistance correction

An HDI used for the silicon heater mock-up is displayed in Figure 5.8. The trace lengths of the power lines differ, which induces different HDI resistances that have an impact on the current flowing through the individual heater chips. A distinction is made for *inner*, *middle*, and *outer* chips of a half-ladder while *outer* is considered as close to the end piece. The following resistances, for the power and ground lines combined, are measured:

$$R_{outer,HDI} \approx 18\,\mathrm{m\Omega} \tag{6.11}$$

$$R_{middle,HDI} \approx 45\,\mathrm{m\Omega} \tag{6.12}$$

$$R_{inner,HDI} \approx 65\,\mathrm{m\Omega} \tag{6.13}$$

Compared to the heating resistance of $2.75\,\Omega$, this results in a relative increase of the resistance for each heater line of 0.65 %, 1.64 %, and 2.36 % for outer, middle and inner chip. This changes the correction factor $f_{c,i}$, introduced in equation 6.10, to:

$$f_{c,i} = \frac{1}{1+\alpha T_i + \frac{R_{i,HDI}}{2.75\,\Omega}} \times \frac{3}{\frac{1}{1+\alpha T_{outer}+0.65\,\%} + \frac{1}{1+\alpha T_{middle}+1.64\,\%} + \frac{1}{1+\alpha T_{inner}+2.36\,\%}} \tag{6.14}$$

The impact of thermal changes on the resistances of the HDI lines can be neglected safely, as they only contribute marginally to the introduced correction factors.

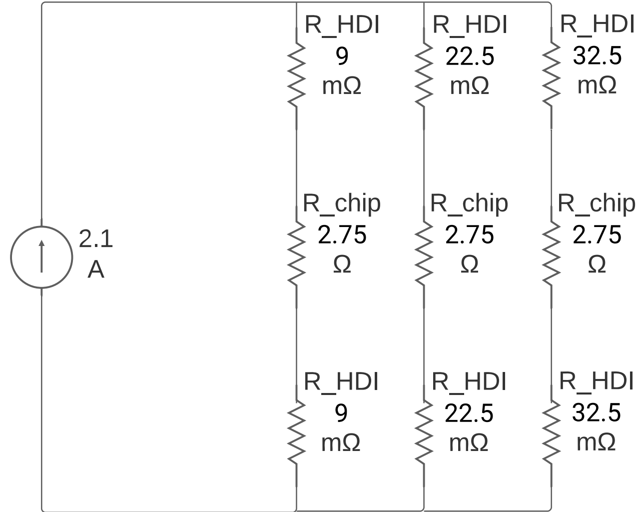


Figure 6.11: Simplified circuit diagram for the powering of a silicon heater half ladder. In the 295 mW/cm^2 scenario, the current source provides 2.1 A to three chips connected in parallel on an HDI with different resistances on each supply line.

Missing temperature measurements of chips

To obtain the correction factor $f_{c,i}$ for each chip, every chip temperature on the corresponding half-ladder is required. For the silicon heater mock-up 18 resistive thermometers, however, are not readable. Each of these non-readable chips is actively heated. For the six ladders, where all thermometers are functional, the results from the temperature map measurements (section 6.4.4) are used to study the temperature profile on a ladder. In the appendix B.2, it is shown that a 2-dimensional polynomial fit describes approximately the temperature profile on each ladder. For every ladder with missing temperature information, such a 2-dimensional polynomial fit is applied. The resulting chip temperatures for the missing chips are then considered in the above corrections.

6.4.2 Temperature measurement uncertainties

Three contributions to the measurement uncertainty of ΔT are discussed in the following. First, temperature shifts of the environment are analyzed. During the finite measurement time the environmental temperature of the experiment location can change. Since the corrugated steel tubes are a good heat exchanger, the environmental temperature couples directly to the helium temperature of the cooling system. The temperature of three heater chips is monitored for *zero power* and *helium plant off* over a time period of 20 h. The maximum temperature fluctuation

observed within a 120 s time window (typical measurement time) over the whole time period is 0.03 K.

Second, the electrical noise on the temperature readout channels is analyzed, again for *zero power* and *helium plant off*. The temperature data is taken for 30 min and is corrected for the environmental temperature shift by a second order polynomial fit. The amplitude of the noise is found to be $\sigma_T \approx 0.002\,\mathrm{K}$. Thus, measurement uncertainties resulting from electrical noise can be neglected due to their small absolute scale.

The last contribution analyzed is the calibration offset. Each sensor or rather its resistance is calibrated to the state at *zero power* but *helium plant on*, as described in section 6.3.2. The reference (inlet) temperature is estimated to be $T_{ref} = (15.5 \pm 1.5)\,°\mathrm{C}$ with the uncertainty resulting from the absence of a temperature sensor directly in the gas inlet. An over or underestimation of the chip resistance R'_0, and the uncertainty on α have an impact on the temperature reading.

The relative uncertainty on the measured *temperature difference* ΔT is obtained by error propagation from equations 6.5 and 6.6:

$$\frac{\sigma_{\Delta T}}{\Delta T} = \frac{1}{\alpha\left(1 + \alpha T_{ref}\right)}\sqrt{\alpha^4 \sigma^2_{T_{ref}} + \left(2\alpha T_{ref} + 1\right)^2 \sigma^2_\alpha} \approx 0.8\,\% \tag{6.15}$$

with $\sigma_{T_{ref}}$ and σ_α the uncertainties of T_{ref} and α. This means that the calibration offset dominates the temperature uncertainty for $\Delta T > 4\,\mathrm{K}$. Thus, for all relevant temperature measurements, the relative uncertainty is considered to be $\pm 0.8\,\%$.

6.4.3 Transient temperature behavior

The time scale for the thermalization and the cool down of the vertex detector are analyzed. This allows to deduce when the system reaches stable conditions and becomes ready to be operated, and how the detector behaves when power is turned off. The analysis is based on the same data used for the temperature maps in the next section. In this section, no corrections on the heat dissipation are yet applied. The measurements are carried out individually for each half-ladder. Such a half-ladder measurement is shown in Figure 6.12. The reference measurement at *zero power* to define T_0 is performed in the 5 s before power is turned on. In two steps, a heat load of $182\,\mathrm{mW/cm^2}$ and $295\,\mathrm{mW/cm^2}$ is applied to all chips for 30 s to 60 s each. Afterward, power is turned off and the next half-ladder is connected to the readout. For some measurements, power is lowered to $182\,\mathrm{mW/cm^2}$ prior to turning off the power as can be seen in Figure 6.12. The helium mass flow is kept constantly at 2 g/s. The inflow for this configuration is always US. Thus, it is expected that chips of higher numbers are warmer.

The temperature curves show that the temperature increase is fast and a plateau is reached within seconds. Within the plateau the temperature is slowly rising asymptotically. This motivates that the data can be described by two exponential functions with time constants τ_0 and τ_1, as discussed below. The choice of exponen-

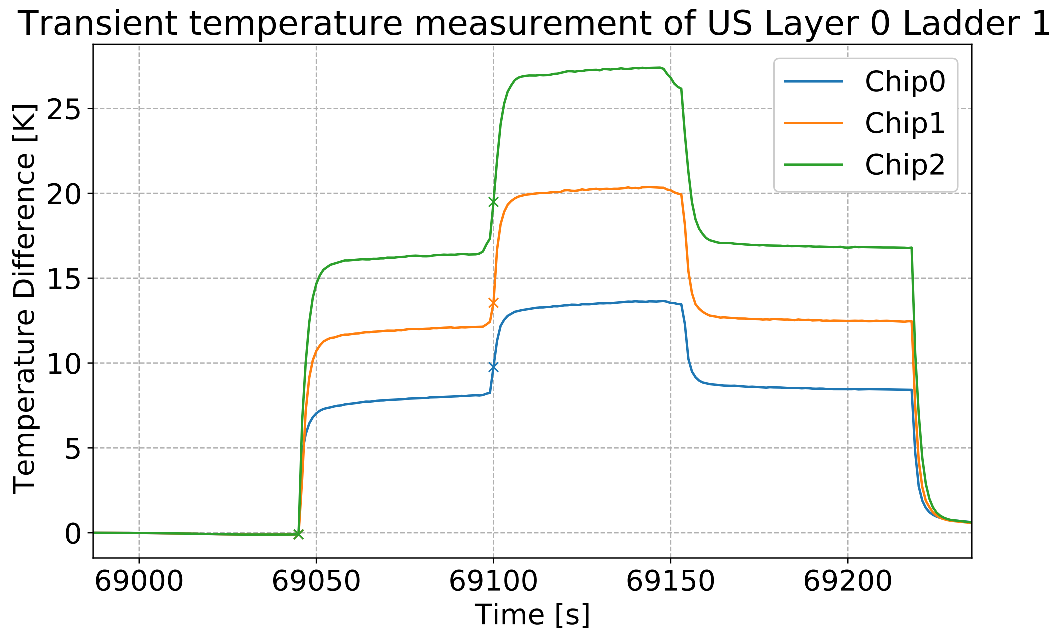


Figure 6.12: Temperature measurement for the US chips of L0 Ladder 1. The heat load of 182 mW/cm^2 and 295 mW/cm^2 is applied stepwise. The crosses indicate the maxima of the temperature curve derivatives (cf. Figure 6.13).

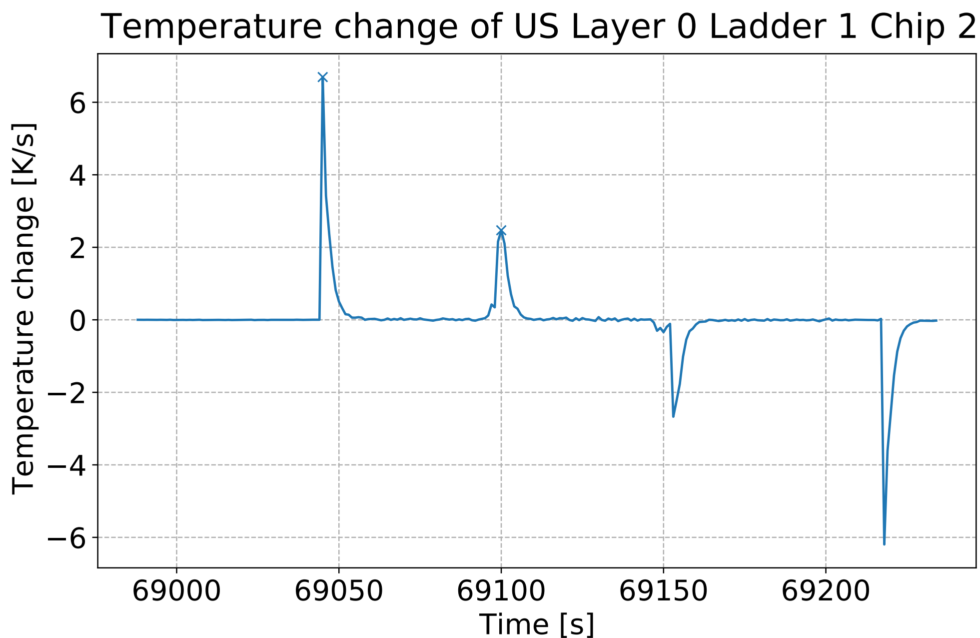


Figure 6.13: Derivative of the temperature curve of L0 Ladder 1 Chip 2. Python peak finder detects peak positions.

tial functions is supported by the fact that the differential heat equation is solved by:

$$\frac{T(t) - T_\infty}{T_0 - T_\infty} = e^{-t/\tau} \tag{6.16}$$

$$T(t) = T_\infty(1 - e^{-t/\tau}) \tag{6.17}$$

with T_∞ as the saturation temperature. T_0 is set to 0 K such that the temperature T corresponds to ΔT.

The presence of two time constants is confirmed by a simplified transient Autodesk CFD simulation: A 50 µm thin silicon substrate of 2.3 mm × 12 mm size[3] on a 50 µm thin PCB ladder is actively heated and cooled by a helium flow of 10 m/s (corresponds roughly to a mass flow of 2 g/s in the vertex detector). Without surrounding material the simulated temperature follows the single exponential function in equation 6.17. In a second configuration, polyvinyl chloride (PVC)[4] end pieces and an interposer dummy on the end piece are added. The interposer can be slightly heated as well. The end piece and the interposer preheat the cooling gas in front of the silicon. Due to their higher heat capacity, this process takes longer to equilibrate. The silicon temperature then follows the sum of two exponentials:

$$T(t) = T_a(1 - e^{-t/\tau_0}) + T_b(1 - e^{-t/\tau_1}) \tag{6.18}$$

with T_a and T_b the temperature contributions of the two time domains. Thus, the used fit function for the transient temperature data is:

$$T_{fit}(t, T_a, T_b, \tau_0, \tau_1, dt) = T_a \cdot \left(1 - e^{-(t-dt)/\tau_0}\right) + T_b \left(1 - e^{-(t-dt)/\tau_1}\right) \tag{6.19}$$

with dt as time offset of the zero crossing. Similarly, the temperature curve for powering off the detector is described by:

$$T_{fit}(t, \tau_0, \tau_1, dt_0, dt_1) = T_0 \left(e^{-(t-dt_0)/\tau_0} + e^{-(t-dt_1)/\tau_1}\right) \tag{6.20}$$

The starting point of the fits is defined by the maximum (or minimum) of the temperature derivative

$$\dot{T}(t_n) = \frac{T(t_{n-1}) - T(t_n)}{t_{n-1} - t_n} \tag{6.21}$$

as shown in Figure 6.13.

The US and DS side of the mock-up are turned on individually by hand, which results in a slight time offset. In case, this manual turn-on procedure induces two maxima in the temperature derivative, always the second peak is considered as

[3]Corresponds to the dimensions of six silicon heater chips placed next to each other.

[4]Standard material of the simulation program is used instead of PEI. Both polymers, PVC and PEI, come with similar thermal properties.

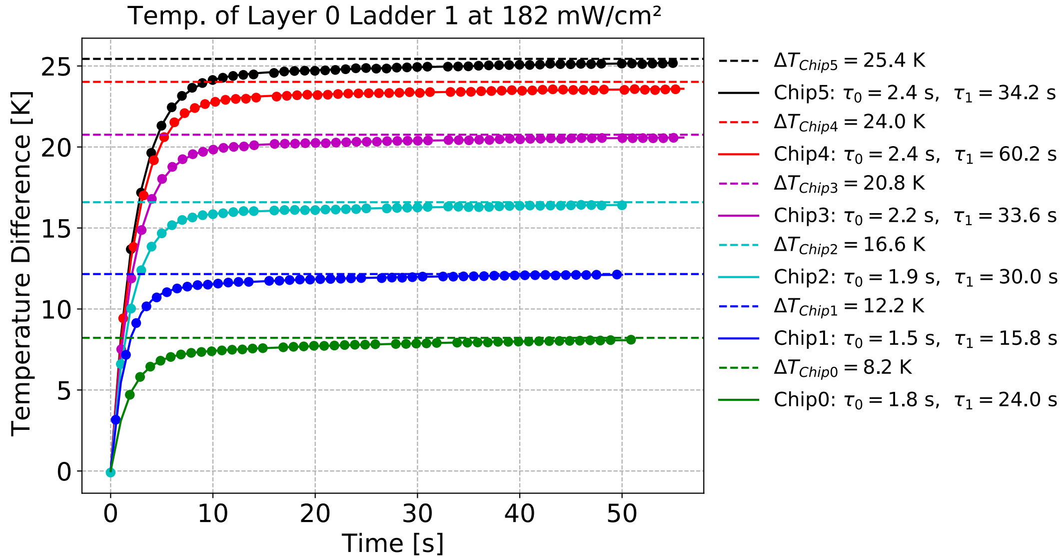


Figure 6.14: Temperature measurement for all chips of L0 Ladder 1 at 182 mW/cm^2. Dots represent data points, solid lines show the fits, dashed lines represent the saturation temperature values from the fit.

starting point of the temperature fit. The fit function in equation 6.19 is used to describe the time constants of the heating process and the saturation temperature (which equals the temperature difference to *zero power*) $\Delta T = T_a + T_b$. This value is used to obtain the temperature maps of the mock-up in the next section.

An example is shown in Figures 6.14 and 6.15 for the transient temperature analysis for a ladder of L0 at heat dissipations of 182 mW/cm^2 and 295 mW/cm^2. The fast time domain has a maximum time constant of $\tau_0 = 2.4$ s for chips 4 and 5. The slow time domain gets dominant in less than 10 s. Its contribution to the saturation temperature is only $T_b/\Delta T = 2\,\%$–$10\,\%$.

In Figures 6.16 and 6.17, the transient temperature curves are shown for a ladder of L1. It can be seen that the time constants for L0 are larger than for L1, which is related to the higher temperatures reached.

With the results obtained, a safe power-up procedure for the vertex detector could be as follows: The detector is divided into eight power partitions. A power partition consists of all half-ladders on one side of the module. An efficient and safe launching procedure is to turn on one power partition and to configure all its chip simultaneously, waiting $4 \cdot \tau_{0,max} \approx 10$ s to reach 98 % of T_a, check all temperatures, and then continue with the next partition. Such a start-up takes 80 s in total. With an additional waiting time of $3 \cdot \tau_{1,max}$, after having configured all sensors, a fully thermalized vertex detector would be ready to operate in less than 5 min in a safe and reliable manner.

In Figures 6.18 and 6.19, the fitted temperature curves of the same ladders as before are shown for the cool down after powering off the mock-up. The initial heat

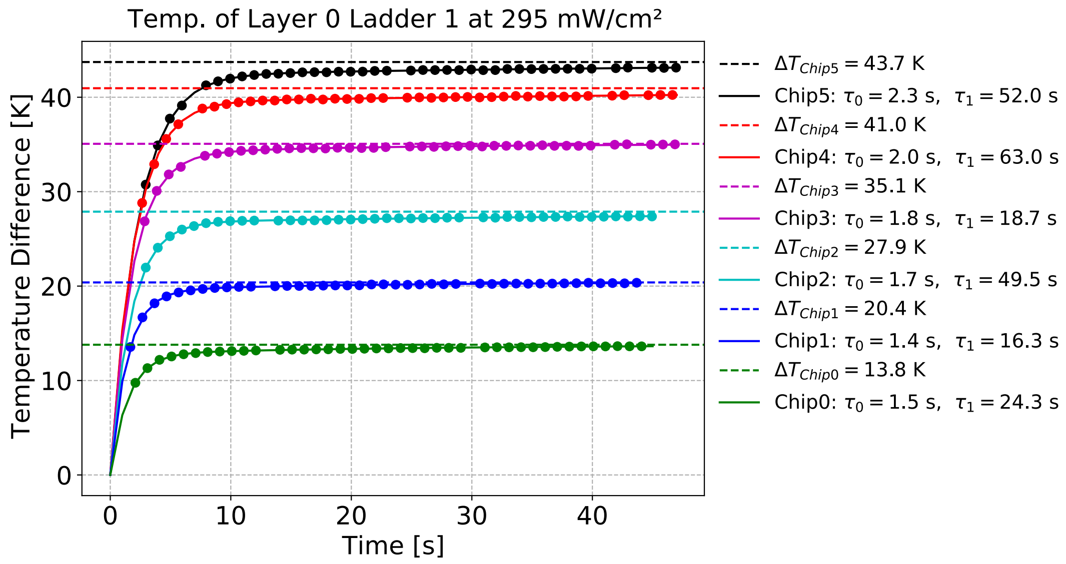


Figure 6.15: Temperature measurement for all chips of L0 Ladder 1 at 295 mW/cm^2. Dots represent data points, solid lines show the fits, dashed lines represent the saturation temperature values from the fit.

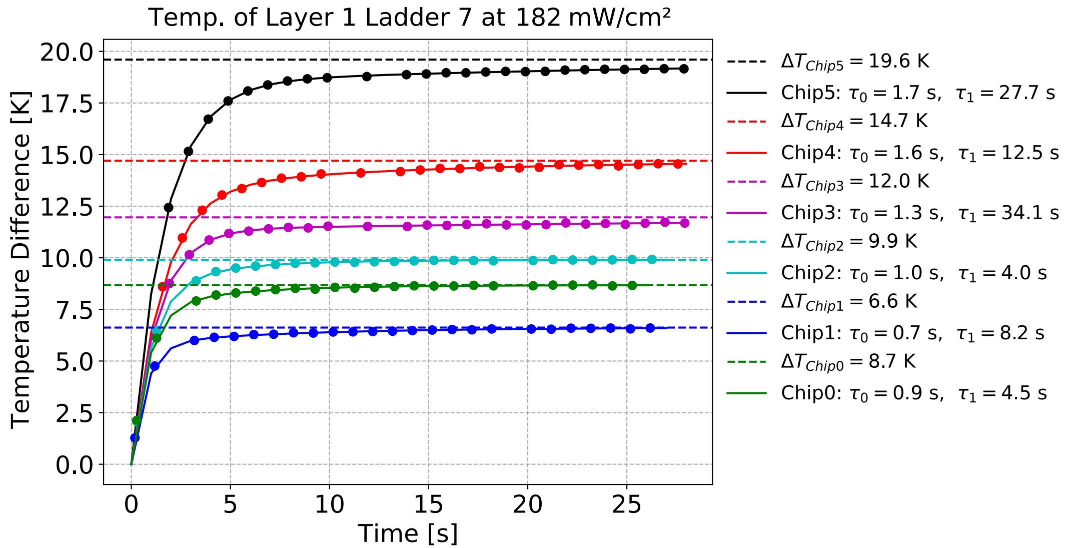


Figure 6.16: Temperature measurement for all chips of L1 Ladder 7 at 182 mW/cm^2. Dots represent data points, solid lines show the fits, dashed lines represent the saturation temperature values from the fit.

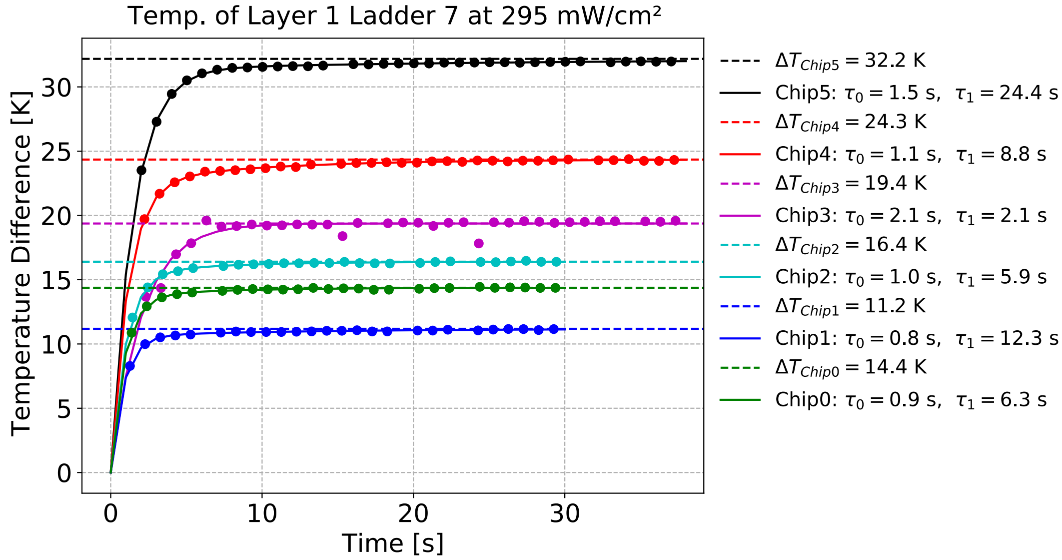


Figure 6.17: Temperature measurement for all chips of L1 Ladder 7 at 295 mW/cm^2. Dots represent data points, solid lines show the fits, dashed lines represent the saturation temperature values from the fit.

dissipation is at 182 mW/cm^2 for both layers. The turning-off is prompt and can be compared to an emergency shutdown of the detector with the helium cooling still operating. The time constants τ_0 for powering on and off the detector match each other (cf. Figures 6.14 and 6.16). Within less than 5 s, the temperature difference of the silicon chips to the inlet temperature is <5 K. The low heat capacity of the detector and the high thermal conductivity of the helium enable a fast and safe shutdown of the detector.

6.4.4 Temperature maps

The temperature maps of the silicon heater mock-up are generated from the saturation temperatures obtained from the transient temperature fits described in the previous section. The saturation temperatures represent the state of a thermalized system. To better understand the ladder mapping in the following plots, the ladder numbering is shown in Figure 6.20. Counting starts for both layers with 0. The chips are counted from 0 to 5 on a ladder, going from US to DS.

The temperature maps are obtained for two different flow configurations. *Nominal flow* describes helium going from US to DS. *Inverted flow* describes helium going from DS to US, while the mock-up remains unchanged.

In Figure 6.21, the temperature maps are shown for L0 for both flow configurations and both heat loads, 182 mW/cm^2 and 295 mW/cm^2, respectively. It is clearly visible that Ladder 3 and Ladder 4 face the highest temperatures for nominal and inverted flow. This indicates that the helium flow is not distributed uniformly inside the mock-up. A region of reduced flow or even backflow potentially reduces locally

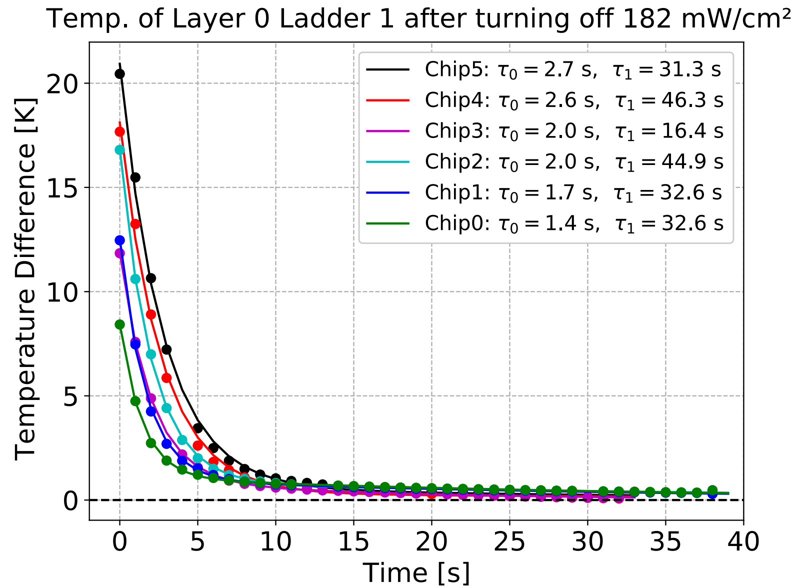


Figure 6.18: Prompt cool down of L1 Ladder 7 from an initial heat dissipation of 182 mW/cm^2. Dots represent data points, solid lines show the fits, dashed lines represent a temperature difference to the inlet temperature of 0 K.

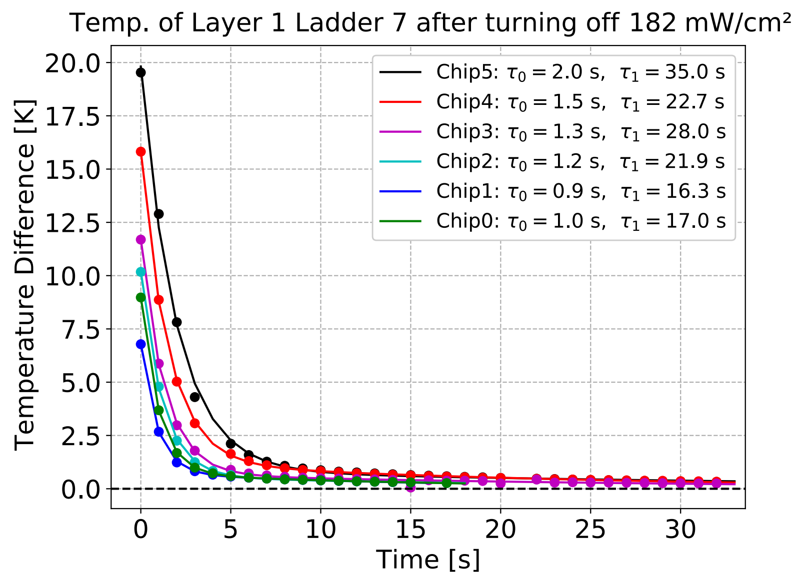


Figure 6.19: Prompt cool down of L0 Ladder 1 from an initial heat dissipation of 182 mW/cm^2. Dots represent data points, solid lines show the fits, dashed lines represent a temperature difference to the inlet temperature of 0 K.

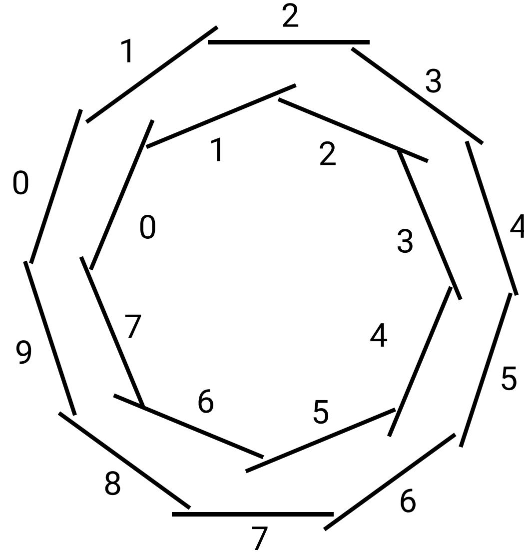


Figure 6.20: Ladder numbering of the vertex detector looking at the detector from US. L0: inner eight ladders, L1: outer ten ladders.

the cooling effect. Such backflow regions are observed for the simulation studies described in [69, 70] and for the tape heater measurements described in section 6.2. The associated vortex is assumed to originate from the symmetry breaking inside the detector caused by the overlaps of the ladders (cf. Figure 6.20). The presence of a potential mirrored backflow region on the opposite side, which is observed in the simulations, is not clearly identifiable for the silicon heater mock-up. The measurements show only a minor temperature increase for Ladder 0 and Ladder 7 of L0. In the appendix, inactive chips are marked with a red square in the temperature maps in Figure B.1. For both, L0 Ladders 0 & 7, a non-active chip is present, which might inhibit the formation of a second hot area there. Inverted and nominal flow configurations show a similar behavior concerning the temperature scale and the temperature distribution.

The results for L1 are shown in Figure 6.22. They confirm the occurrence of a hot region at the same position as L0 for nominal and inverted flow. The increased temperature for Ladder 0 compared to neighboring ladders indicates the presence of a region of reduced flow on the opposite side. However, analogous to L0, the fully non-active DS Ladder 9 might inhibit a further temperature increase on this side of the mock-up. The temperatures measured for L1 are overall lower than for L0. This is expected considering that this layer is cooled by a helium flow from both sides, one flow channel enclosed by the layer and one channel surrounding the layer.

The maximum ΔT as well as the average temperature of both layers for each configuration are summarized in Table 6.1. The raw temperature data is given for all chips of both layers in the appendix B.4.

For both flow configurations, the results are comparable. Only the maximum temperature of L1 is considerably higher for the inverted flow. Non-uniformities

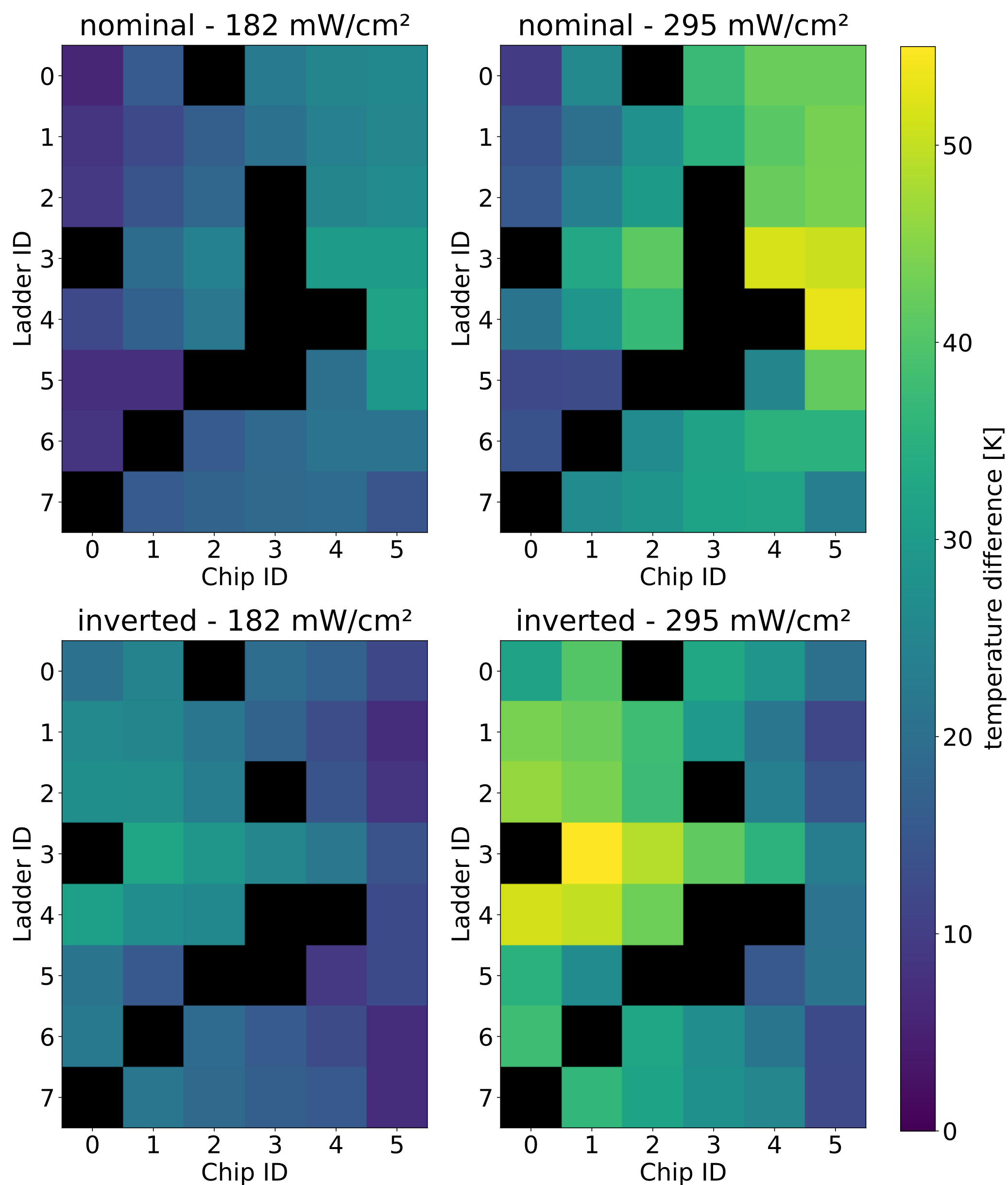


Figure 6.21: Temperature maps of L0 of the silicon heater mock-up for nominal and inverted flow and heat loads of $182\,\mathrm{mW/cm^2}$ and $295\,\mathrm{mW/cm^2}$. Chips without temperature readout are marked black. Inactive chips marked in Figure B.1.

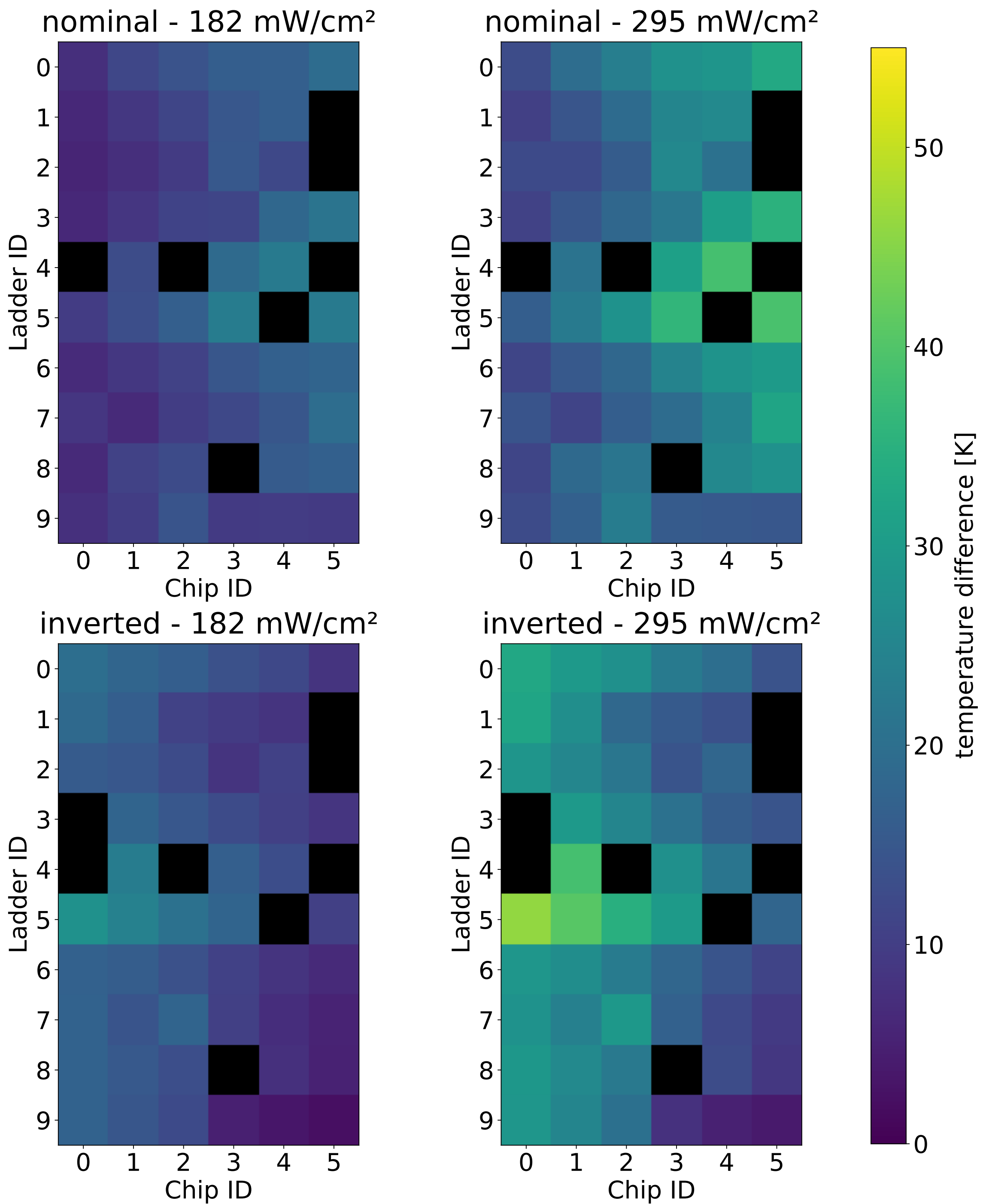


Figure 6.22: Temperature maps of L1 of the silicon heater mock-up for nominal and inverted flow and heat loads of $182\,\mathrm{mW/cm^2}$ and $295\,\mathrm{mW/cm^2}$. Chips without temperature readout are marked black. Inactive chips marked in Figure B.2.

	heat dissipation	max. ΔT nominal	max. ΔT inverted	average ΔT nominal	average ΔT inverted
L0	182 mW/cm^2	31.7 K	32.6 K	18.9 K	19.0 K
	295 mW/cm^2	53.3 K	54.8 K	31.3 K	31.8 K
L1	182 mW/cm^2	23.2 K	27.8 K	12.8 K	13.3 K
	295 mW/cm^2	39.2 K	46.1 K	21.6 K	22.2 K

Table 6.1: Maximum and average ΔT of the silicon heater mock-up from the uncorrected temperature maps.

in the gas flow distribution are considered as the main driver for local hot spots. Geometrical effects are expected to be a source for such deviations. The rotational asymmetry of the mock-up might result in a different flow distribution for flow inversion. In addition, the imperfect shape of the polyimide foil surrounding the mock-up (Figure A.13) might have a non-negligible effect on the helium flow.

Temperature maps including corrections for the effective heat dissipation

As discussed in section 6.4.1, the true heat dissipation of the mock-up for these measurements is higher than the nominally applied 182 mW/cm^2 (295 mW/cm^2). The temperature maps are corrected for the described effects by the correction factors $f_r \cdot f_c^2$. The necessary missing chip temperatures are obtained by polynomial fits of the chip temperatures as described before (cf. Figure B.5). The corrected temperature maps are shown in Figure 6.23 and 6.24. The corrected maximum and average temperatures for the silicon heater mock-up are summarized in Table 6.2.

	heat dissipation	max. ΔT nominal	max. ΔT inverted	average ΔT nominal	average ΔT inverted
L0	182 mW/cm^2	28.3 K	29.7 K	17.4 K	17.7 K
	295 mW/cm^2	44.5 K	47.5 K	27.3 K	28.2 K
L1	182 mW/cm^2	24.6 K	25.3 K	12.6 K	12.7 K
	295 mW/cm^2	41.6 K	39.6 K	20.5 K	20.5 K

Table 6.2: Maximum and average ΔT of the silicon heater mock-up from the corrected temperature maps.

The applied corrections account for the effect of the self-heating of the chip. The enhanced warming of the cooling gas by the increased heat dissipation is not considered. Thus, the presented corrected temperature maps are expected to overestimate the temperatures. A more detailed discussion follows below, where the results are

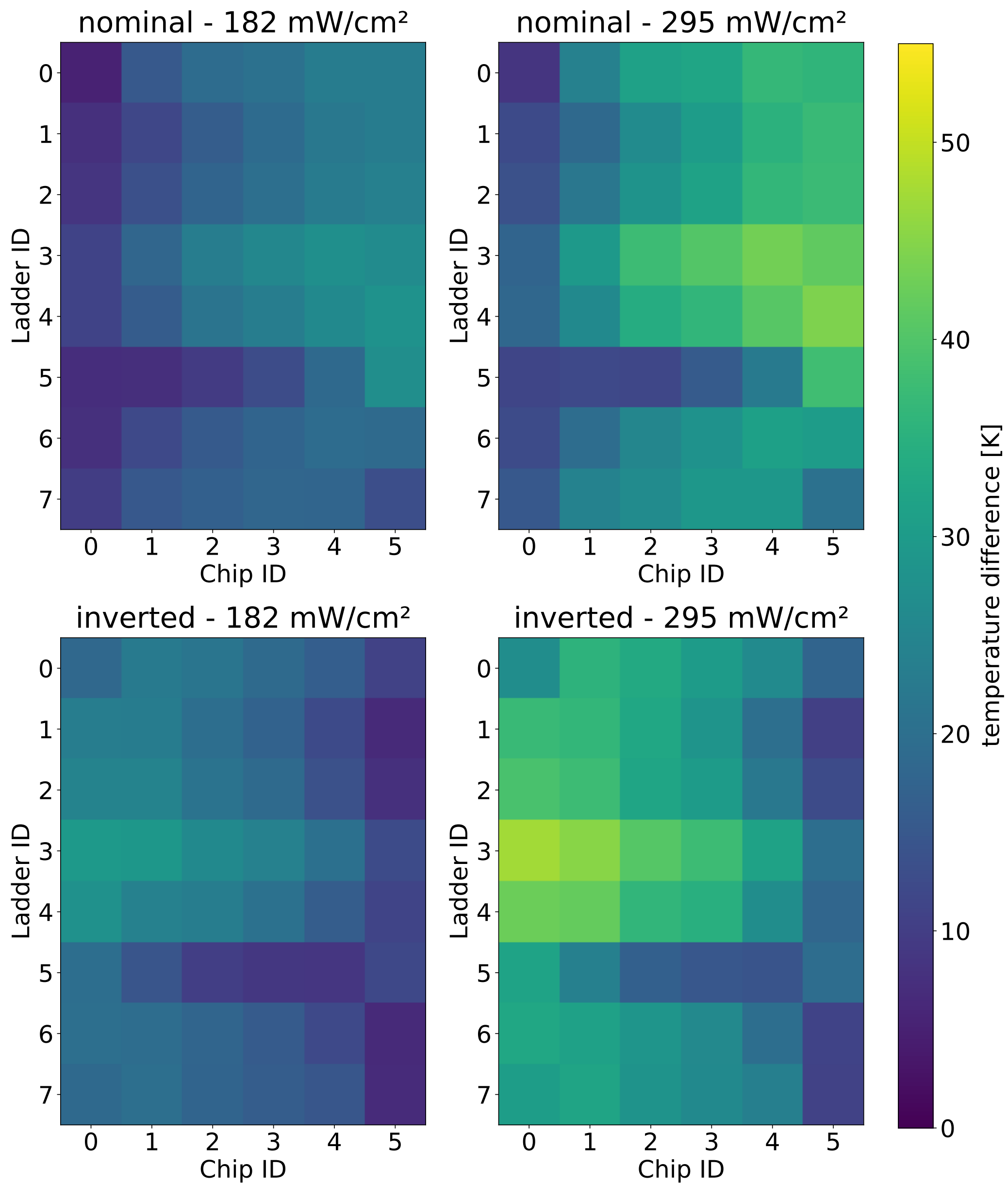


Figure 6.23: Corrected temperature maps and interpolated results for chip without working readout of L0 of the silicon heater mock-up for nominal and inverted flow and heat loads of $182\,\mathrm{mW/cm^2}$ and $295\,\mathrm{mW/cm^2}$. Inactive chips marked in Figure B.3.

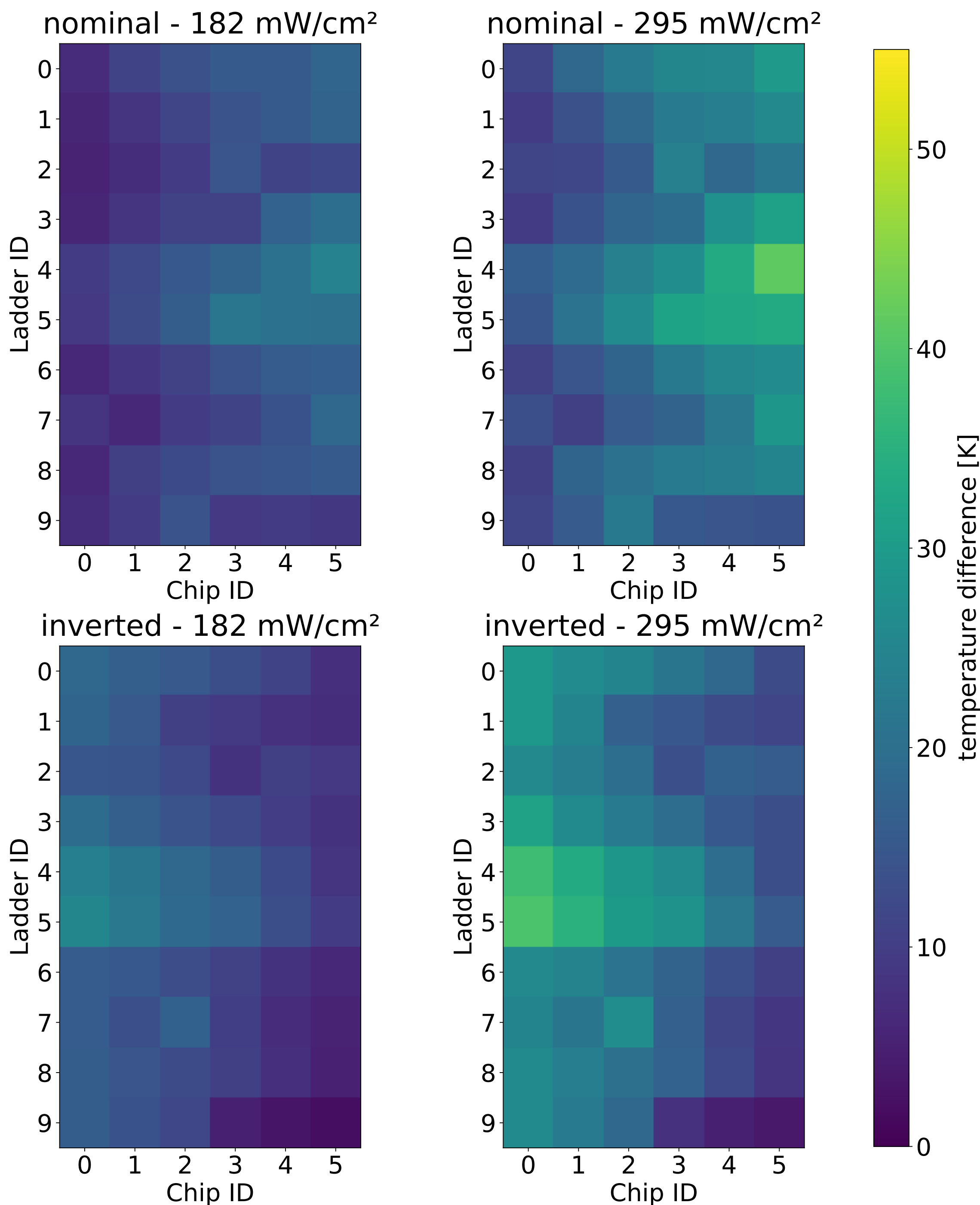


Figure 6.24: Corrected temperature maps and interpolated results for chip without working readout of L1 of the silicon heater mock-up for nominal and inverted flow and heat loads of 182 mW/cm^2 and 295 mW/cm^2. Inactive chips marked in Figure B.4.

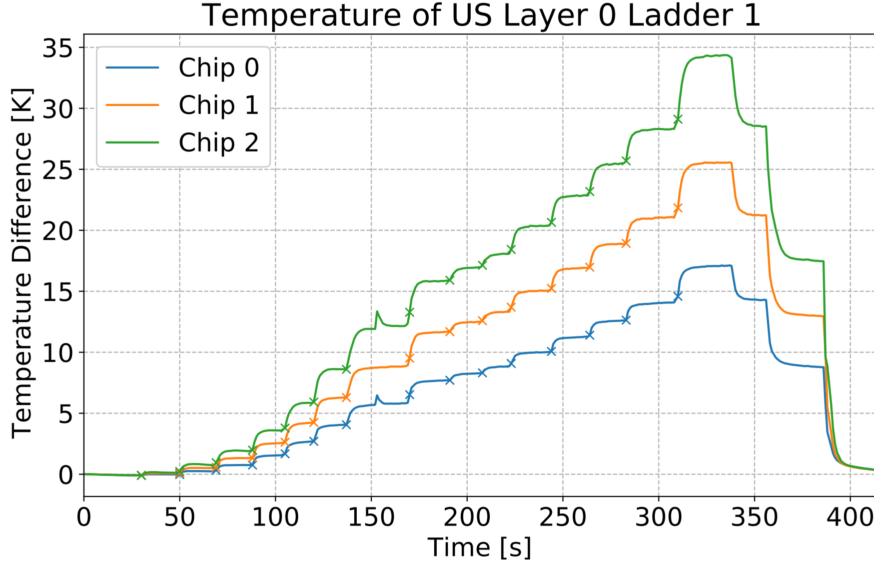


Figure 6.25: Power scan for US L0 Ladder 1. The crosses indicate the maxima of the temperature curve derivatives.

compared to simulation studies. For both heat dissipation value, 182 mW/cm^2 and 295 mW/cm^2, all chip temperatures are below 50 K.

The results can be translated also to higher and lower heat load, as will be discussed in section 6.4.5. This allows to estimate the temperatures for the expected heat dissipation of 215 mW/cm^2 and the conservative limit of 350 mW/cm^2. The corresponding results are presented in section 6.4.6.

6.4.5 Temperature-to-power relation

The temperature maps obtained in the previous section show the thermostatic behavior of the silicon heater mock-up for only two specific heat loads. The heat dissipation of the MuPix chips depends on their operation mode. Depending on the particular settings used in the experiment, e.g. to optimize the time resolution or to tune the sensor in a different way, the consumed power may vary in a broad range.

To be able to translate the above measurements to different heat loads, a power scan is performed. The temperatures are read out for all six chips of one ladder of L0 and L1 each. For L0, Ladder 1 is chosen, since it is the only inner ladder with six functional temperature readouts. For L1, Ladder 7 is chosen. All measurements are performed with the nominal flow direction and the full mock-up heated.

In Figures 6.25 and 6.26, the recorded US and DS temperature curves for the power scan of L0 Ladder 1 are displayed. Due to the relation $P = RI^2$, power increases with the square of the current that is provided by the power supply. The current is increased in steps of 0.2 A from 0 A to 1.6 A, in steps of 0.05 A from 1.6 A

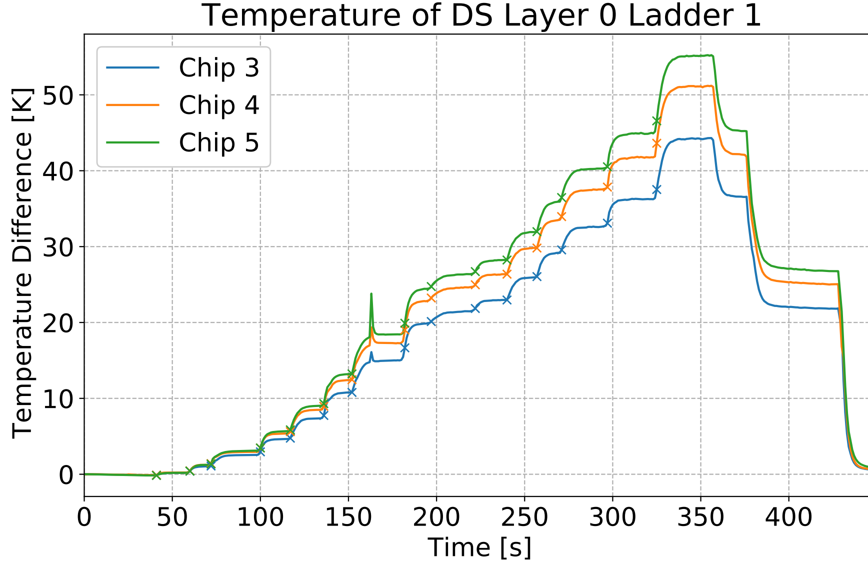


Figure 6.26: Power scan for DS L0 Ladder 1. The crosses indicate the maxima of the temperature curve derivatives.

to 1.7 A, and in steps of 0.1 A from 1.7 A to 2.1 A, plus a final measurement at 2.3 A. The last value corresponds to an uncorrected heat dissipation of 353 mW/cm^2.

For every current value, the individual saturation temperatures ΔT_i are again obtained by fitting an exponential function. Due to the stepwise increase of power, the resulting temperature steps are smaller than in the previous section. Thus, a single time constant is found to describe the temperature curves sufficiently. The resulting fit function is:

$$T_{fit}(t, \Delta T, \tau, dt) = \Delta T \cdot \left(1 - e^{-(t-dt)/\tau}\right) \tag{6.22}$$

The starting points for the fits are again the local maxima of the temperature derivative (cf. equation 6.21). They are indicated in Figures 6.25 and 6.26 as crosses on the temperature curves.

In the appendix, the temperature data with the corresponding exponential fits is shown for L0 Ladder 1 in Figures B.6, B.7 and B.8. The resulting ΔT values are plotted against the corrected heat dissipation (cf. section 6.4.1) in Figure 6.27. The effective heat dissipation increases, in the most extreme case, from the nominal 353 mW/cm^2 to 426 mW/cm^2 for Chip 3. The plot shows a linear relation between temperature and the applied heat load for every chip.

For L1, the results are shown in Figure 6.28. The outcome is analogous to L0, the relation between temperature and applied heat load is linear.

The measurements demonstrate that the temperature-to-power relation can be regarded as linear. This way, the temperature maps obtained in the previous section can be translated to any applied heat load.

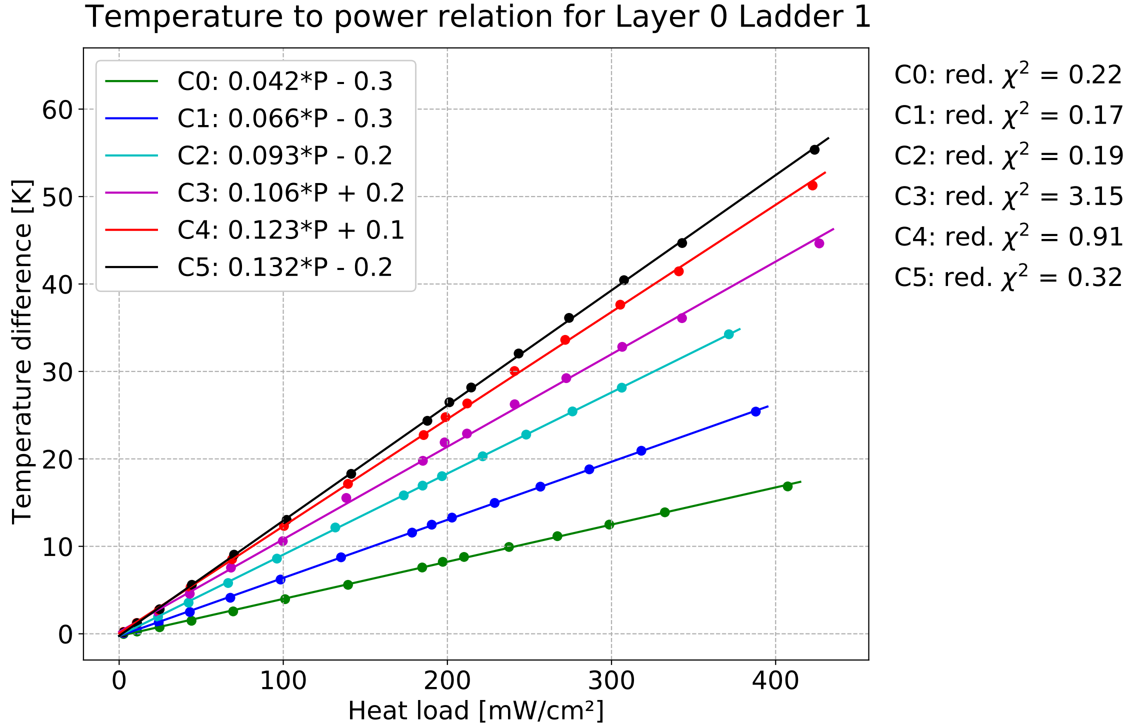


Figure 6.27: Temperature-to-power relation for L0 Ladder 1. Uncertainty on the temperature is based on the calculations in section 6.4.2 (For $T > 4\,\mathrm{K}$: $0.8\,\% \cdot T$, else: $0.03\,\mathrm{K}$).

6.4.6 Extrapolated temperature maps for the expected heat load

The temperature maps from section 6.4.4 are extrapolated to the measured heat dissipation of MuPix10 chips of $215\,\mathrm{mW/cm^2}$ and to the specification limit of the cooling system of $350\,\mathrm{mW/cm^2}$ dissipated on the chips. In the previous section, it was demonstrated that the temperature-to-power relation is linear. Thus, the temperatures from Figures 6.23 and 6.24 are scaled to the heat dissipation of interest. The resulting temperature maps are shown in Figures 6.29 and 6.30. The corresponding maximum and average temperatures are summarized in Table 6.3.

For both L0 and L1, the specified requirement of $\Delta T < 70\,\mathrm{K}$ is valid for every chip. However, considering that the periphery is around $20\,\mathrm{K}$ warmer than the average temperature (rough estimate from [70]), the peak temperature of the periphery for $350\,\mathrm{mW/cm^2}$ is expected to be above this limit. For the expected heat dissipation of $215\,\mathrm{mW/cm^2}$, the highest temperature reached is $34.9\,\mathrm{K}$. In this case, all chips are well below $70\,\mathrm{K}$ also under the assumption of the warmer periphery.

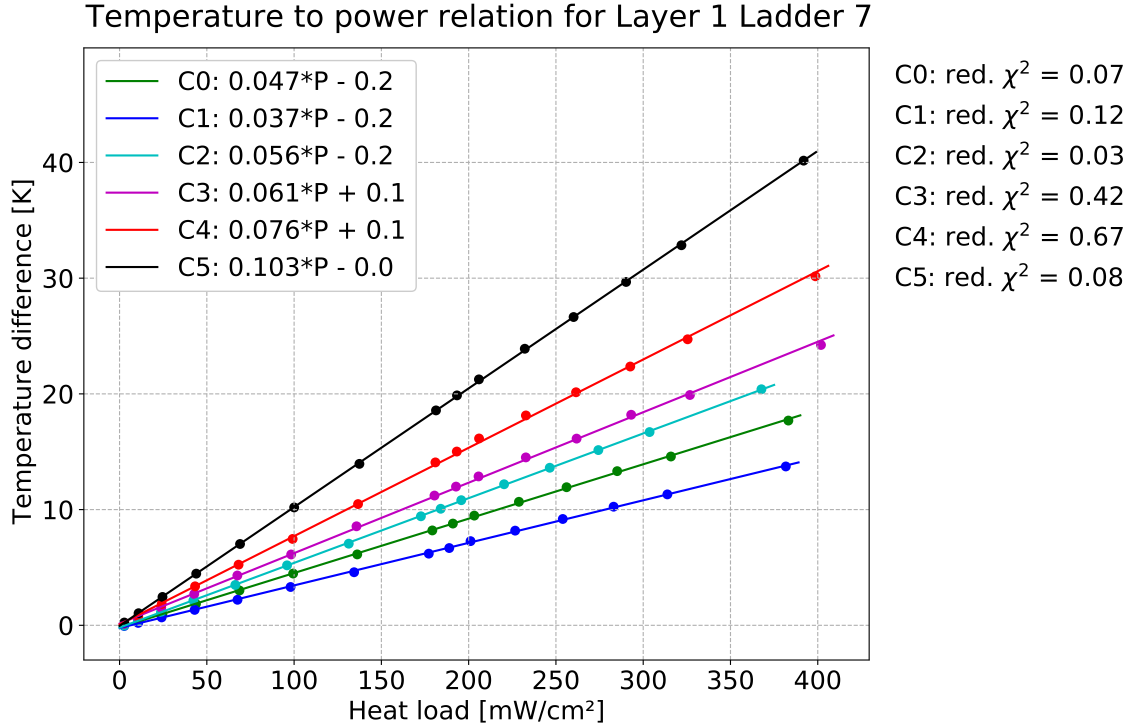


Figure 6.28: Temperature-to-power relation for L1 Ladder 7. Uncertainty on the temperature is based on the calculations in section 6.4.2 (For $T > 4\,\text{K}$: $0.8\,\% \cdot T$, else: $0.03\,\text{K}$).

Comparison of the temperature maps to simulation results

The temperature map analysis is concluded by a comparison to simulation data. The thermal simulation studies of the vertex detector presented in [70] contain only one configuration, which includes the updated scheme of two helium flow channels. It simulates the thermal behavior of MuPix chips, which dissipate more heat in their periphery as outlined in section 4.3.1. In the described implementation, the average heat dissipation is $400\,\text{mW/cm}^2$ with an 8.65 times higher heat dissipation in the chip periphery compared to the active pixel matrix. The maximum local temperature difference reached in this simulation is 51.9 °C.

To compare the measurements presented above to the simulation studies, this simulation has been repeated for this work by Marin Deflorin with an adapted heat dissipation profile. Like the silicon heater mock-up, the chips are heated uniformly. The heat dissipation is set to $350\,\text{mW/cm}^2$. The resulting temperature maps are shown in Figure 6.31. One should keep attention to the different color scale compared to the measurement results.

It is clearly visible that the temperature maps from simulations and measurements (Figure 6.31 vs. Figures 6.29 and 6.30) show a different temperature distribution. The simulation indicates the presence of two backflow regions, which are less distinct than the single hot region visible in the silicon heater mock-up measurements. The

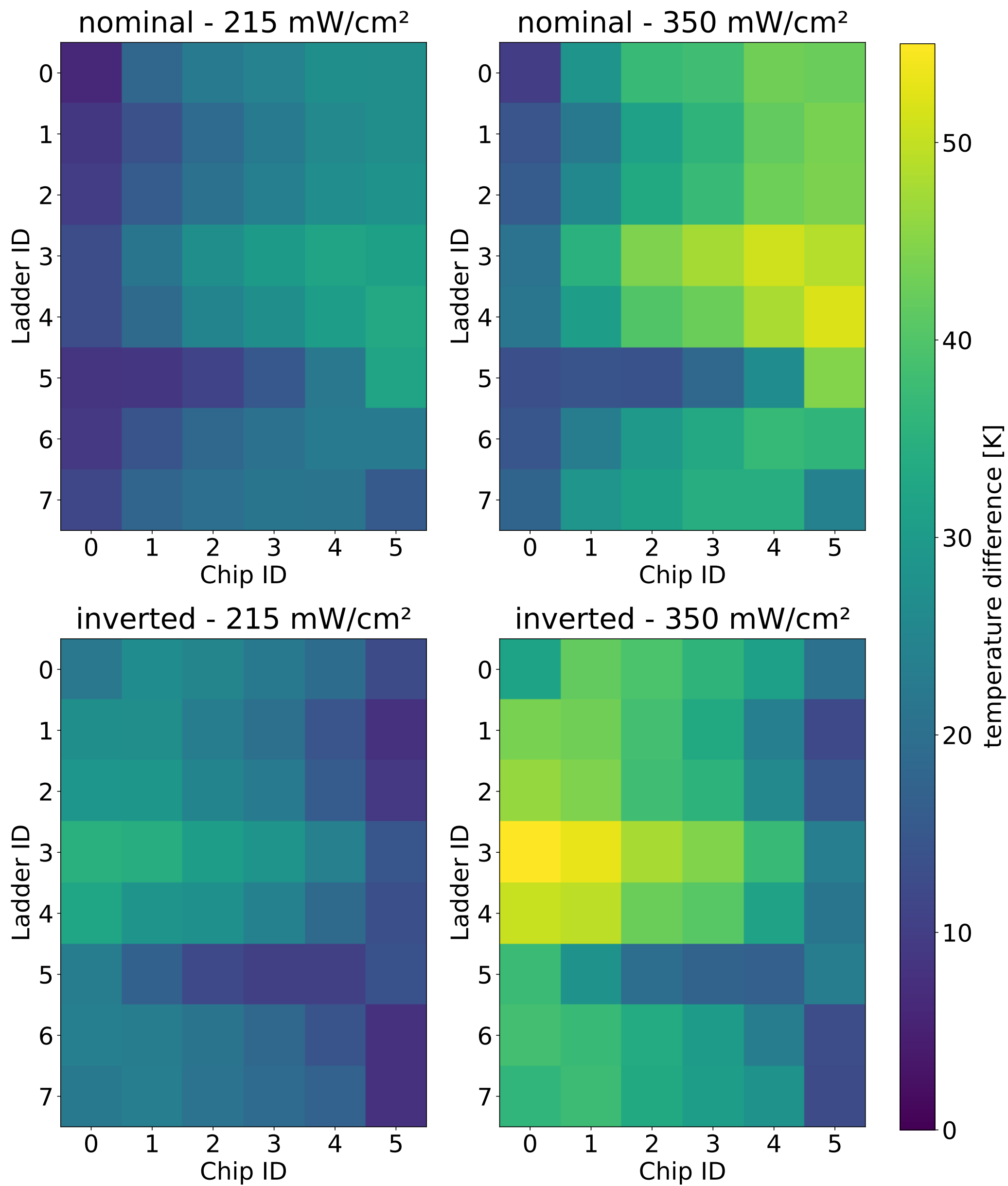


Figure 6.29: Temperature maps of L0 of the silicon heater mock-up extrapolated to heat loads of $215\,\mathrm{mW/cm^2}$ and $350\,\mathrm{mW/cm^2}$ for nominal and inverted flow. Values from Figure 6.23 multiplied by $P_{extrapolated}/P_{measured} = 1.178$.

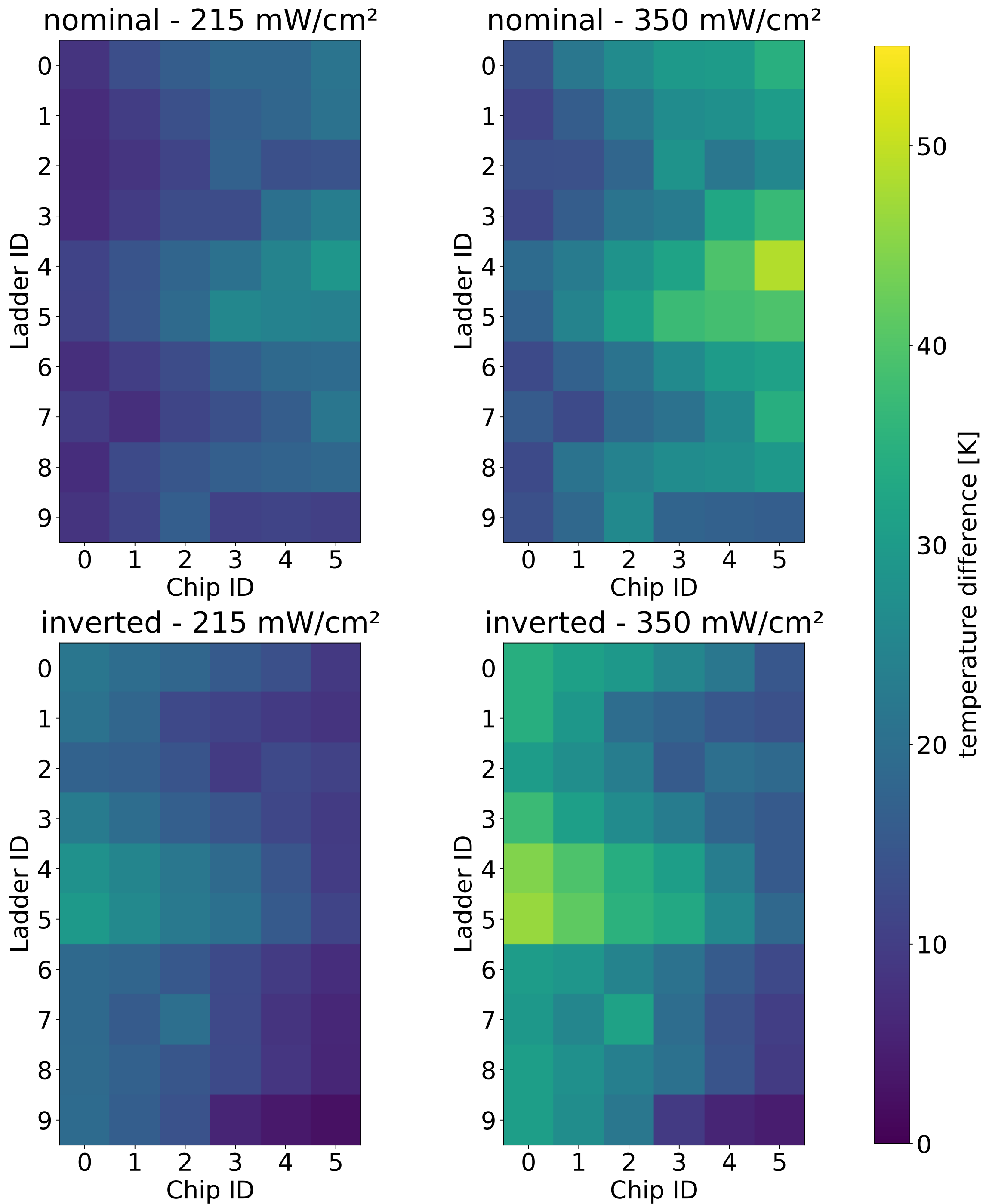


Figure 6.30: Temperature maps of L1 of the silicon heater mock-up extrapolated to heat loads of $215\,\mathrm{mW/cm^2}$ and $350\,\mathrm{mW/cm^2}$ for nominal and inverted flow. Values from Figure 6.24 multiplied by $P_{extrapolated}/P_{measured} = 1.178$.

	heat dissipation	max. ΔT nominal	max. ΔT inverted	average ΔT nominal	average ΔT inverted
L0	215 mW/cm^2	33.1 K	34.9 K	20.5 K	20.8 K
	350 mW/cm^2	52.2 K	55.7 K	32.2 K	33.3 K
L1	215 mW/cm^2	28.8 K	29.7 K	14.9 K	15.0 K
	350 mW/cm^2	48.7 K	46.5 K	24.2 K	24.2 K

Table 6.3: Maximum and average ΔT of the silicon heater mock-up from the extrapolated temperature maps. 215 mW/cm^2 corresponds to the measured heat dissipation of MuPix chips in the laboratory. 350 mW/cm^2 corresponds to the specification limit of the cooling system.

		max. ΔT	average ΔT
L0	measurement	52.2 K	32.2 K
	simulation	33.9 K	26.0 K
L1	measurement	48.7 K	24.2 K
	simulation	22.6 K	17.5 K

Table 6.4: Maximum and average ΔT comparison of the corrected temperature maps obtained from silicon heater measurements and simulations of a uniformly heated mock-up, both at 350 mW/cm^2.

average and maximum temperatures of the extrapolated temperature maps for L0 and L1 are compared with the simulation results in Table 6.4.

The maximum temperatures are significantly off by 18 K for L0 and 26 K for L1. The average temperatures are 6 K higher for the measurements compared to simulation, despite 8 of 108 chips not being heated in the mock-up. The simulation assumes a simplified inflow geometry for the outer flow, which does not correspond to the realized final geometry. In addition, no resistive heating in the supply lines and no heat capacity of the surrounding materials are included in the simulation. The resistive heating from the HDIs is expected to add only 1 % to 2 % (cf. HDI resistances in section 6.4.1). However, the inflowing gas also passes the interposer stack, where the power connector and its surrounding material preheat the gas, which is not included in simulations. As discussed in section 6.4.4, the measured temperatures are expected to overestimate the temperature, since the chips dissipate more heat due to thermal resistance changes.

The comparison shows that for the present configuration, the simulation framework does not predict reliably the temperature profile of the vertex detector. The average temperature of the silicon heater mock-up is significantly higher than simulated. The formation of local hot spots resulting from the gas flow distribution

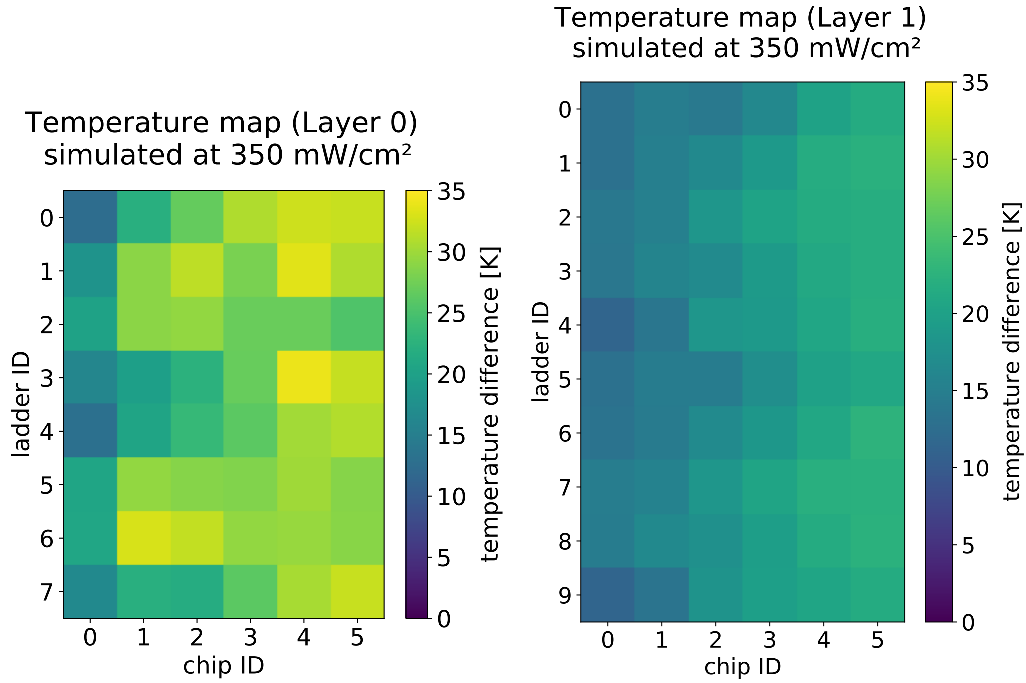


Figure 6.31: Simulated temperature maps for a uniformly heated Mu3e vertex detector with 350 mW/cm^2.

manifests in a different way for the measurement as for the simulation. Particularly for high heat loads, the latter is strongly relevant. The associated backflow regions define whether a chip crosses the temperature limit of 70 K or not. As a result, the temperature profile of the vertex detector has to be measured in the final realization to be able to estimate the maximum allowed heat dissipation of the chips.

6.4.7 Temperature dependence on mass flow

This section covers the dependence of the temperature on the mass flow. In the previous studies, only the baseline helium mass flow of 2 g/s was used. Here, lower values down to 1.4 g/s are studied. This helps to understand the thermal behavior of the detector in case a mass flow reduction has to be considered, e.g. for technical reasons. For this purpose, the temperatures of L0 Ladder 1 and L1 Ladder 7 are measured for different values between 1.4 g/s and 2.0 g/s. The results are displayed in Figures 6.32 and 6.33.

The relative temperature increase compared to the nominal mass flow of 2.0 g/s is shown in Figure 6.34. The system is operated in a regime where the temperature increases roughly by the same percentage as the mass flow is lowered. At 1.8 g/s, the temperature increases by less than 10 %. This might be considered as tolerable even for a heat dissipation of 295 mW/cm^2. Going to lower mass flows, like 1.6 g/s or 1.4 g/s, the temperature increases by 20 % or 30 % on average. The temperature

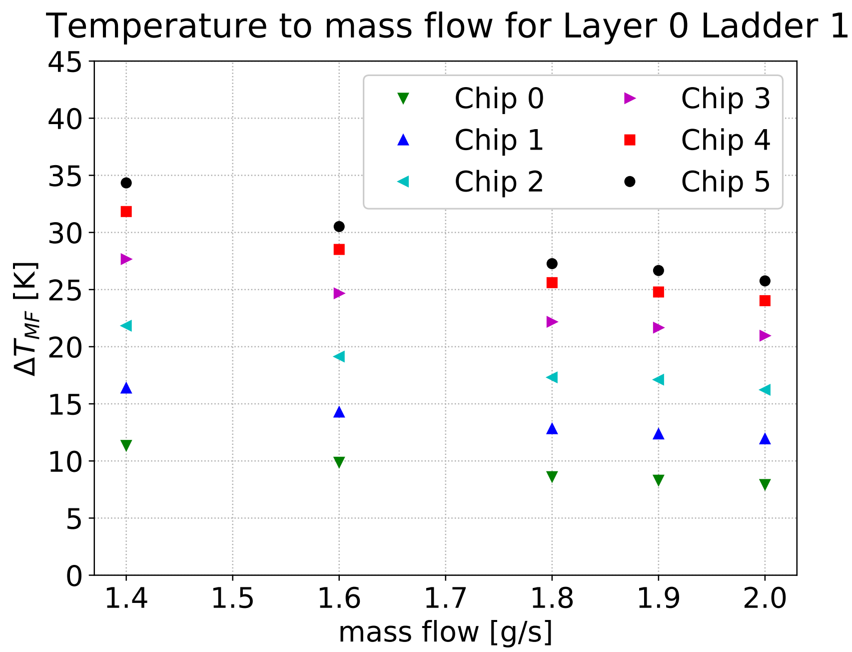


Figure 6.32: Temperature-to-mass flow relation for L0 Ladder 1.

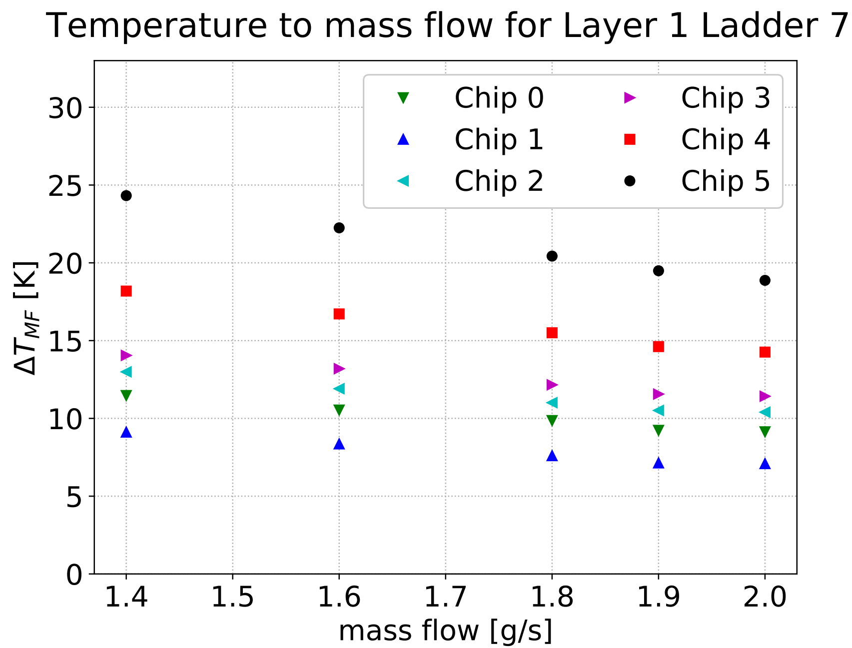


Figure 6.33: Temperature-to-mass flow relation for L1 Ladder 7.9.

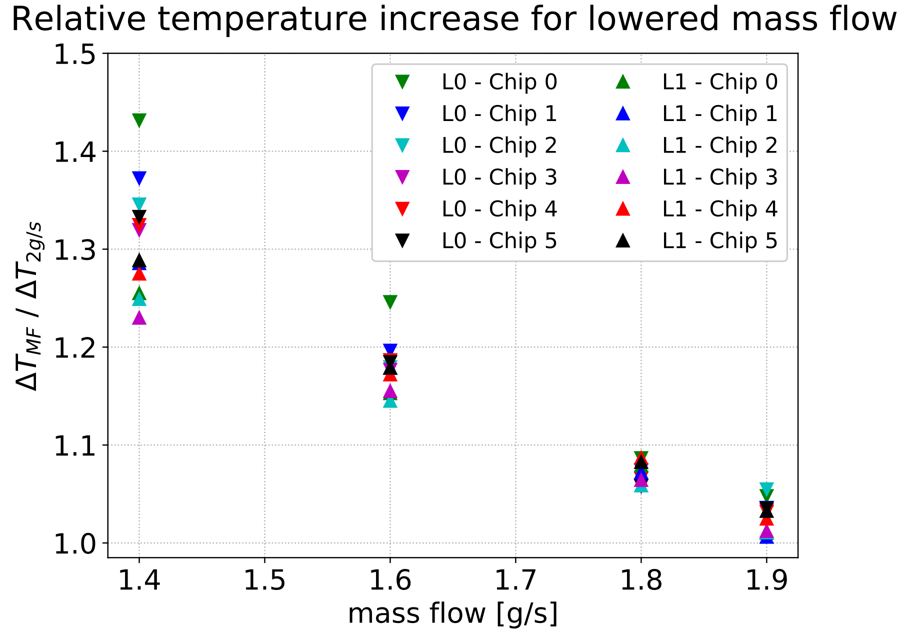


Figure 6.34: Relative temperature increase for lowered mass flow for L0 Ladder 1 and L1 Ladder 7.

change starts to spread for different chips and different ladders indicating that the flow distribution changes for lower gas velocities. Thus, the above temperature maps can not be translated directly for mass flows lower than 1.8 g/s.

6.4.8 Summary

Overall, the gaseous helium cooling system shows excellent performance. The average temperature difference to zero power applied is below 35 K for both layers, even for the conservative limit of 350 mW/cm^2. With a chip periphery that is 20 K warmer than the average temperature, every chip would be below the limit of $\Delta T < 70$ K for a heat dissipation of 215 mW/cm^2, which is the expected value for the MuPix10 chips. For the conservative limit of 350 mW/cm^2, the maximum chip temperature strongly depends on the formation of backflow regions. In case of such a prominent flow asymmetry as observed for the silicon heater mock-up, there is a danger that individual chips in L0 get too hot.

Thus, the measurements show that a better understanding of the formation of the backflow regions is beneficial to obtain more uniform chip temperatures within the vertex detector for the final experiment. Optimization approaches, like different mass flows inside the four helium ducts, can be studied in the near future by the used silicon heater mock-up, or by first pre-production modules of the vertex detector, which are expected to become available by the end of 2022.

Part IV

Vertex detector prototype

Vertex detector prototype for the integration run 7

The goal of the Mu3e integration run carried out in Summer 2021 is to first time operate detector prototypes inside the Mu3e magnet, with muons decaying on target. Specifically, the integration of services in and outside the magnet, the operation of the helium cooling plant prototype (section 6.1) under realistic conditions, and the DAQ are aimed to be tested.

The corresponding vertex detector prototype is based on the first full-scale MuPix chip, the MuPix10, described in section 4.3.1. Due to a design flaw, the MuPix10 can not be configured by the Mu3e slow control with a single differential line. The configuration is therefore realized via SPI instead. This implies that the prototype design has to be adapted and thus significantly deviates from the baseline design of the Mu3e vertex detector outlined in section 4.3.2.

This chapter motivates the design of the vertex detector prototype and presents the resulting consequences on the services, in particular the powering, readout, and cooling of the detector in section 7.1. It is followed by a summary of the prototype construction in section 7.2. Finally, the performance results of the prototype from laboratory tests are presented in section 7.3.

7.1 Conceptual design

To operate MuPix10 chips on ladders, SPI lines must be integrated on all flex circuits. This implies five additional single-ended lines per half-ladder holding three chips, namely MOSI, SPI_CLOCK, and a CHIP_SELECT for each chip. However, all interposer pins (cf. section 5.2.1) are already occupied in the baseline design. In addition, to integrate the additional lines on the HDIs, a full redesign is required. Thus, the realization of SPI within the baseline detector design would demand an enormous workload.

The requirements on the material budget and space constraints for services are less restrictive for the integration run compared to the final detector. It is not foreseen to fully reconstruct particles, which allows to loosen the constraints on the material budget of the tracking layers. Furthermore, only two SciFi modules and

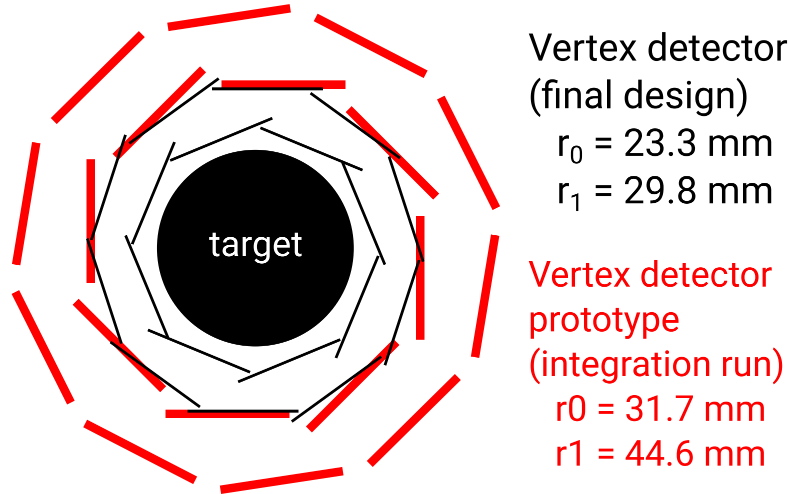


Figure 7.1: Comparison of vertex detector geometry: integration run vs. final design with the radius of the two layers given.

no SciTile or outer pixel layer modules are foreseen for the integration run, leaving more space for services.

The above considerations motivate a simplification of the detector design and using commercially available components for powering and readout. The adapted ladder design is presented in section 7.1.1. The modified cooling and electrical services are described in sections 7.1.2 and 7.1.3.

7.1.1 Vertex detector prototype design

The specific ladder design for the integration run is based on standard PCBs instead of HDIs. These PCB ladders integrate bond pads and connectors for the power and data cables, which makes other detector components like interposers and additional flex circuits obsolete. The ladders are larger in all dimensions and much stiffer compared to HDI-based ladders. Their size, particularly the height of the connectors, implies that the radii of both layers must be increased compared to the baseline design as sketched in Figure 7.1. L0 is therefore located at 31.7 mm and L1 at 44.6 mm compared to 23.3 mm and 29.8 mm for the final design. The polyimide foil confining the outer helium flow is only 5.7 mm away from the fiber ribbons compared to 20.4 mm in the baseline design, which increases the helium cooling volume. The prototype comes with less overlaps of the chips of the two layers due to the larger radii. This introduces gaps in L1, which are not covered by active detectors.

A bare ladder, which consists of a u-shaped PCB, is displayed in Figure 7.2. The six MuPix10 chips are first glued on a polyimide foil which is glued on the PCB such that the active matrix of every chip has no PCB material below it. The electrical connections from PCB to chips are established by conventional wire bonding instead of spTAB. Pictures of the assembled prototype are shown in section 7.2, which covers the construction of the detector.

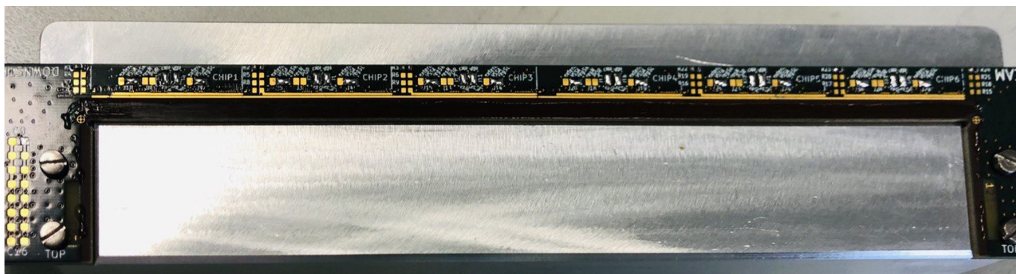


Figure 7.2: 6-chip-PCB on aluminum chuck before gluing of sensors. [61]

7.1.2 Helium cooling

The helium distribution is simplified for the vertex detector prototype compared to the final design. The direct connection of LV, HV, and data cables to each ladder increases the number of electrical cables originating directly from the detector compared to the final design (36 ribbon cables & 54 LV or HV cables compared to 10 end-piece flex circuit wings). This makes it extremely difficult to realize a distribution ring hosting all feedthroughs. In addition, the increased length of the ladders leaves almost no space for any distribution ring between the beam pipes. Therefore, the confined helium cooling volume is extended to the SciFi support structure (Figures 7.3 and 7.4). Thus, the helium flow distribution inside the detector differs to the baseline design due to the missing guidance. The overall mass flow remains at the baseline value of 2 g/s.

As all services, the supply lines for the helium are guided along the beam pipes. For the integration run, this is realized by PVC tubes that are fixed to the beam pipe by cable ties (Figure 7.5). The inlet and outlet tubes end beneath the SciFi supports blowing the helium into the confined detector volume and sucking it out. Eight tubes are evenly distributed in φ on the beam pipe to provide a uniform helium distribution to the detector (Figure 7.5b). The minimum total cross section for the helium channels is around $225\,\mathrm{mm}^2$, which is comparable to the final system with around $200\,\mathrm{mm}^2$. Toward the beam pipe ends, the inner tube diameter is increased from 6 mm to 14 mm to minimize the pressure drop on the lines.[1] The tubes are connected to the flange plates at the magnet doors via a 3D printed structure (Figure 7.6). The connection to the helium cooling plant outside the magnet is realized via 50 mm inner diameter PVC tubes with a length of 5 m and 10 m on the US and DS side, respectively.

7.1.3 Services and infrastructure

The experimental setup, including all services, is mounted on a cage, which carries the US and DS beam pipes. This cage can be inserted into the Mu3e magnet on a rail system. The vertex detector is located in the central part between the two

[1] The cross section increases from $\approx 200\,\mathrm{mm}^2$ to $\approx 1200\,\mathrm{mm}^2$.

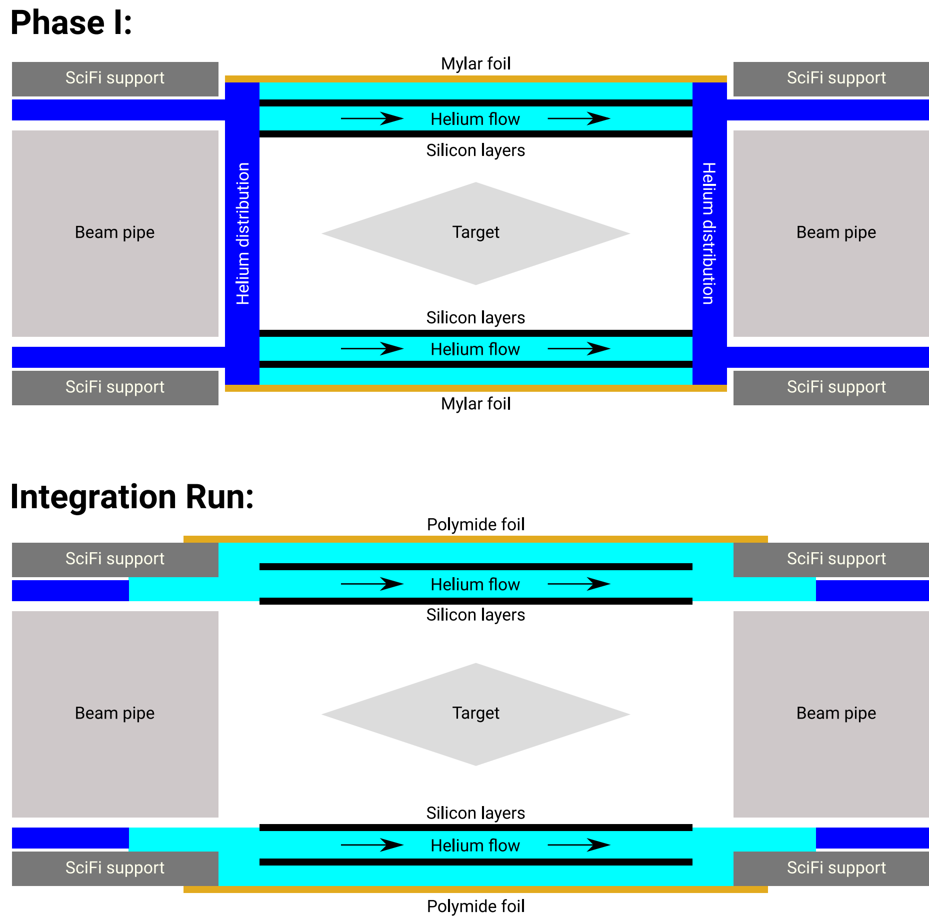


Figure 7.3: Sketch of the helium cooling volume of the vertex detector for the integration run and the final design.

beam pipes. Thus, all services of the vertex detector have to be guided along the beam pipes.

In the following sections, the individual services are described with an emphasis on the differences to the baseline design.

Sensor powering

In the final detector, groups of 4/5 half-ladders (L0/L1) are forming power partitions, which are supplied by a single channel. During the integration run, however, the low voltage supply for the vertex detector is realized by individual power connections for each half-ladder, resulting in 36 power channels. The power supplies are integrated into MIDAS and are controlled remotely. In contrast to the final experiment, the pixel detector is not powered by DC-DC converters, which are located at the experimental cage. Instead, the power is provided by HAMEG HMP4040 power supplies, which are located outside the magnet.

Figure 7.4: Helium flow volume of the vertex detector prototype confined by polyimide sheets.

The beam pipes used for the integration run are bare and not equipped with the copper rods providing the LV in the baseline design. Instead, cables with a cross section of 0.5 mm^2 are attached directly on the beam pipe. They are held in place by 3D printed support rings (Figure 7.7). Sense wires are implemented to compensate for the voltage drops on the cables, which are around 6 m long. As the power supplies come without an internal interlock connection, a relay is connected on each channel, which is enabled by the status of the helium cooling plant.

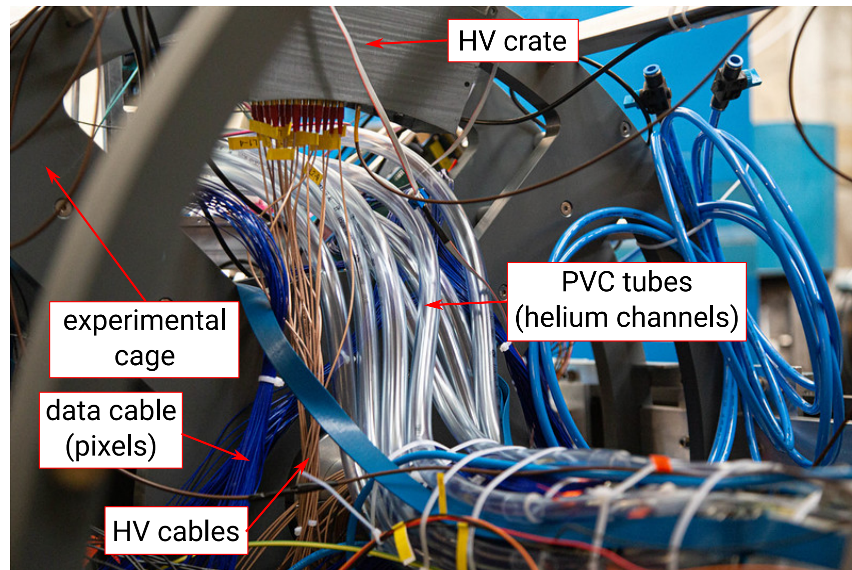
High voltage supply

The high voltage for the sensors is supplied by eight HV boards (4 US & 4 DS) equipped with small Cockcroft–Walton generators. They are able to generate voltages down to −120 V. For the integration run, the HV is kept at only −20 V. The boards are located inside the magnet at the support wheels of the cage (see Figure 7.5a). One board provides 4 channels, resulting in 16 channels on each side. Thus, on each side two pairs of half-ladders share one HV channel.

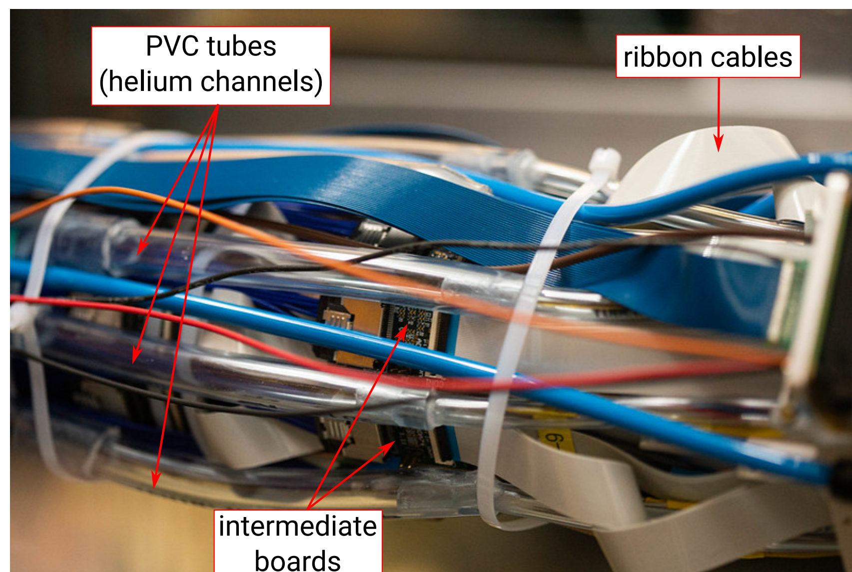
The HV connection is provided by coaxial cables with a diameter of 1.8 mm. They are mounted between the intermediate boards (see next section) and the support rings (Figure 7.8). Only the HV line is soldered to the detector, the shielding is not connected on the detector side to not introduce a ground loop. The HV ground is referenced on the supply line of the HV crate as described below.

Slow control, data and temperature readout

To configure the chips, send out the data, and read out the temperature diode of one chip of a half-ladder, 36 channels are connected to the outside:



(a) Helium tubing at the cage toward the beam pipe. On the top part, the gray HV crate hosting eight HV boards for both the pixel and SciFi detectors is visible.



(b) Helium tubing on the beam pipe.

Figure 7.5: Helium tubing providing the coolant to the vertex detector inside the Mu3e magnet. - Image courtesy N. Berger.

- 18 data lines (3 chips × 3 differential pairs)
- 4 lines (2 differential pairs) for the CLOCK and SYNC_RESET
- 5 single-ended SPI lines (3x CHIP_SELECT, MOSI, SPI_CLOCK)

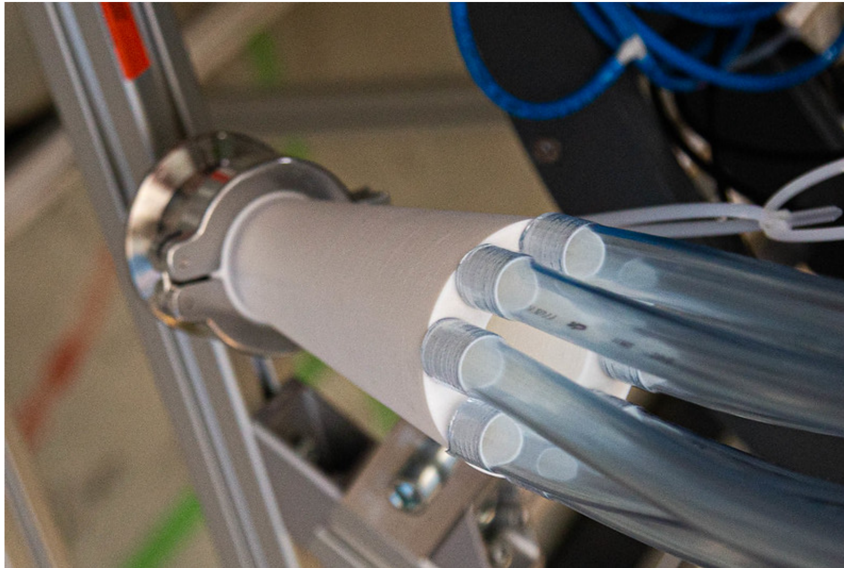


Figure 7.6: Helium distribution structure to distribute gas flow from magnet flange to eight PVC tubes. - Image courtesy N. Berger.

- 9 sense lines (3 per chip) for VDD, GND, and the temperature diode

Two short 33-pin ribbon cables guide these channels from the ladder to an intermediate PCB. These boards are attached to the 3D printed support rings that also hold the LV cables (Figure 7.8). The corresponding boards for L0 and L1 are arranged on separated rings with a distance of around 10 cm. Thus, the ribbon cable length for the two layers is different. The L0 ribbon cables are guided beneath the L1 intermediate boards (Figure 7.9). To guide the ribbon cables around the SciFi support, some cables have to be twisted. To reduce the number of channels, it jumpers select from which chip the voltage is sensed and the temperature is read out.

A commercial cable with 16 differential pairs[2] connects each intermediate PCB to the FEB via a so-called detector adapter board (DAB), which is a custom adapter board for each sub-detector.

Grounding scheme

The reference ground of the experiment is localized at dedicated metal plates on both sides of the experimental cage. The plates are connected together via 2.5 mm^2 copper cables. On one side of the magnet, the reference ground is guided outside the magnet and grounded to earth.

All ground lines of the LV supplies are connected to this reference ground. This includes not only the power lines for the MuPix chips but also the supply lines for the FEBs, the HV boards, and the SciFi detector.

[2]Samtec AcceleRate® Slim Cable Assembly, 0.635 mm Pitch

Figure 7.7: LV cables for the vertex detector prototype on the US beam pipe. 3D printed support rings in blue.

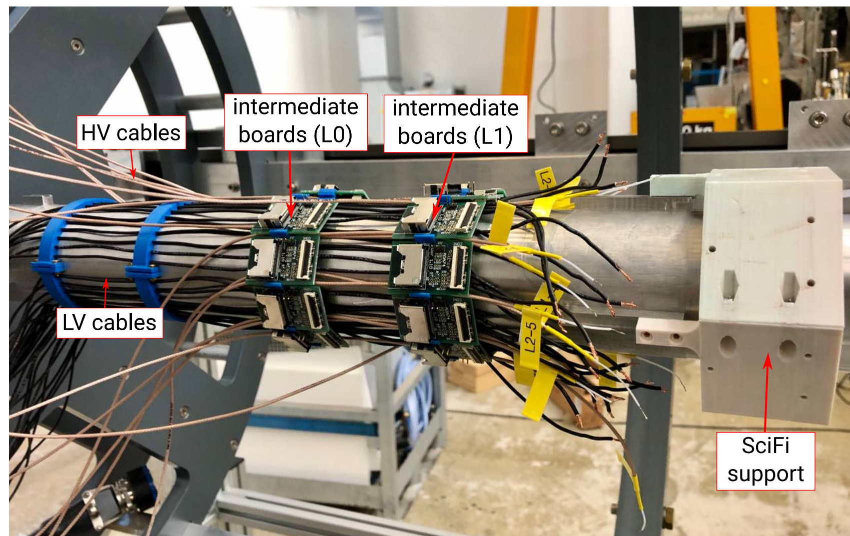


Figure 7.8: Intermediate boards mounted on the beam pipe, HV cables attached in the gap between boards and 3D printed support rings.

7.2 Construction of the Vertex Detector Prototype

The detector construction of the integration run prototype follows the same principles as the final design. It is modularized, with ladders forming layers as in the baseline design; however, here they are not grouped into modules. The main features of the detector construction and their implications on functionality and yield are described in the following sections.

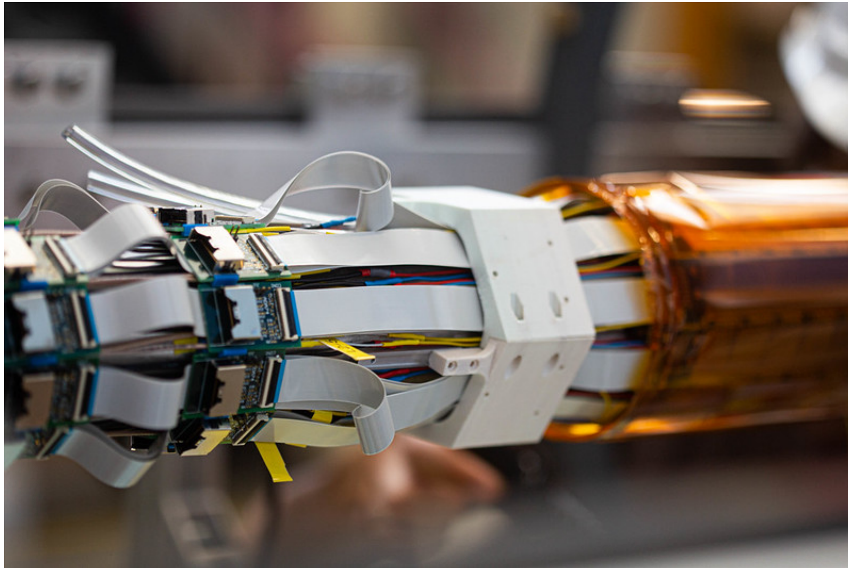


Figure 7.9: Finalized cabling of the vertex detector prototype on the beam pipe. L1 ribbon cables are connected to the first (right) ring of intermediate boards, L0 cables to the second ring. All cables are routed beneath the support ring of the SciFi detector (white). Curled ribbon cables originate from longer cables that are bent around the SciFi mounting points. - Image courtesy N. Berger.

7.2.1 Ladder assembly

The first step of the ladder assembly is similar to the baseline procedure (see description in section A.2). Six chips are positioned with a slightly larger gap of 100 µm (as opposed to the 40 µm gap size of the final design). Instead of an HDI, a bare polyimide foil serves as support and is glued to the backside of the chips. No interposer flex circuits are needed.

After glue curing, the bare ladder is flipped and glued on the u-shaped PCB. Alignment markers which are laser-cut on the polyimide foil are aligned with the PCB under the microscope. The wire bonding is done at the ASIC lab in the Kirchhoff Institute for Physics, Heidelberg.

Despite the analogous procedure, the ladder assembly is much more challenging for these ladders compared to the HDIs due to the bonding procedure. While for spTAB, the chip is located directly on the bond jig, here, the chips are on top of a stack of PCB, glue, polyimide, and another layer of glue. If glue is not filling the interface region uniformly, the stack acts like a spring absorbing the bonding force. Thus, a reliable electrical connection is challenging to make. Since the bond pads are located at the bottom side of the chip, the quincunx glue pattern, used e.g. for the silicon heaters, does not cover the area below the pads. Therefore, a line of glue below the pads is added to the gluing pattern, as visualized in Figure 7.10. This, in turn, increases the risk of spilling glue around the chip edge. The procedure requires

some practice for the correct application of glue concerning position and quantity. In section 7.3.2, the impact of this complication on the yield of the integration run ladders is discussed.

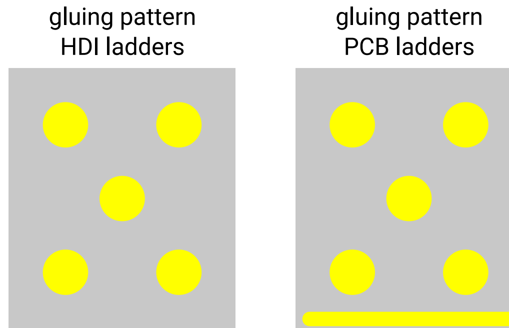


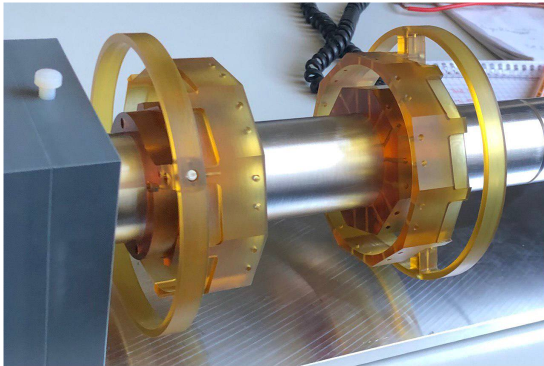
Figure 7.10: Comparison of the gluing pattern: HDI-based ladders vs. PCB-based. An additional strip of glue beneath the bond pads is added to the quincunx pattern for the PCB ladders.

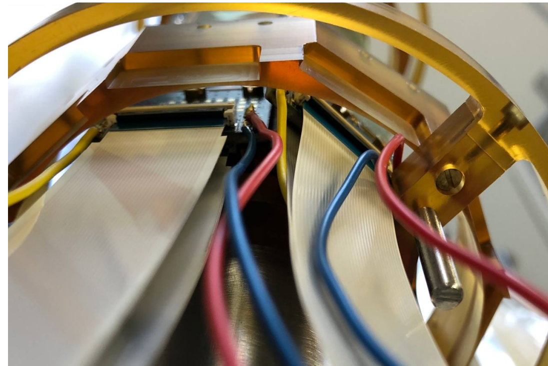
7.2.2 Barrel assembly

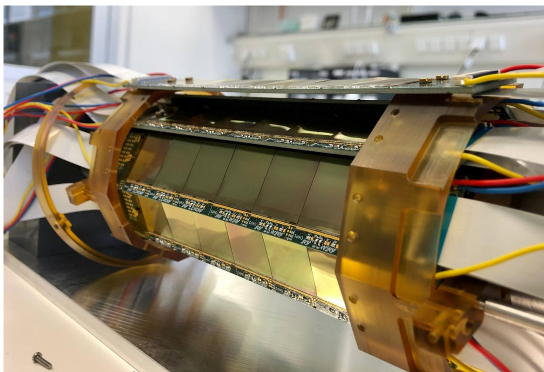
The support structure for the two barrel-shaped layers is manufactured in PEI. Two double-rings serve as mounts to attach the detector to the beam pipes and to hold the outermost polyimide foil that confines the helium flow. A hexagonal and a decagonal prism are connected to each double ring and serve as end pieces (Figure 7.11a). The ladders are mounted on the facets of these prisms.

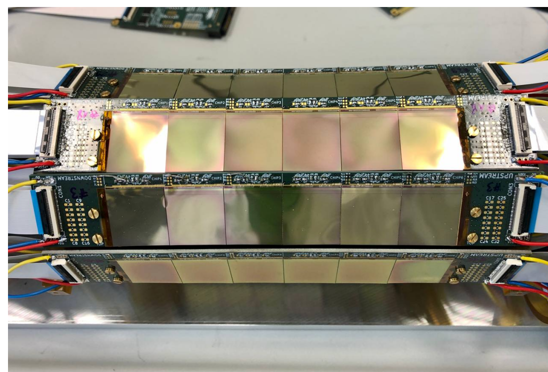
In the first step of the assembly procedure, the PEI parts are placed on the corresponding mounting tool (Figure 7.11a). The L0 end pieces are positioned with dummy aluminum ladders for the correct spacing. Then, the PCB ladders are mounted one by one. A major difficulty is that the 20-30 cm long ribbon and power cables are already attached to the ladders, since the bottom-sided connectors are not accessible anymore after mounting the ladders. All cables have to be guided through the L1 support and the double-ring while mounting (Figure 7.11b). Furthermore, the ladders have to be placed without touching neighbors. After the placement, the ladders are screwed onto the PEI end pieces. Each ladder is checked for potentially induced shorts by damaged bond wires and whether all chips are still configurable after mounting. Once L0 is completed, the PEI end pieces of L1 are brought into position (Figure 7.11c). The mounting procedure is the same as for L0.

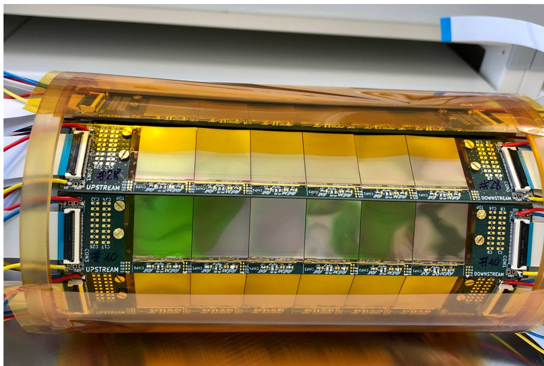
In the last step, the double-rings are fixed to the end pieces and six polyimide sheets are glued on the outermost rings to confine the helium volume (Figure 7.11e). The vertex detector prototype is mounted on the beam pipes as one piece. The PCB ladders provide sufficient stability, such that spring loading foreseen for the final design is not needed. There is a fixed mount on the US side as for the final detector but a loose mount on the DS side. Instead, the prototype is attached to a


(a) PEI end pieces and double-rings.


(b) Space for cable feedthrough.


(c) Full L0 assembled.


(d) Full L1 assembled.


(e) Mounting of the helium confinement.

(f) Fully assembled prototype.

Figure 7.11: Mounting procedure of the vertex detector prototype for the Mu3e integration run. The PEI pieces are placed on the mounting tool. First, all ladders of L0 are placed on the inner end-pieces. The readout and power cables are fed through the PEI rings. Second, all ladders of L1 are placed on the outer end-pieces. In the end, the detector volume is confined by polyimide sheets.

fixed mount on the US side as for the final detector but to a loose mount on the DS side.

7.3 Chip and ladder testing

For the vertex detector prototype, MuPix10 chips with nominal substrate resistivities of 20 Ω cm and 200 Ω cm are used. Chips are qualified on a probe station with a needle card before detector construction. Since this test setup was not fully functional during chip testing, the chips are tested again on the ladder.

7.3.1 Chip Testing

The chip testing with the needle card setup had limited high-frequency capabilities prior to the integration run, a problem that has been resolved in the meantime. High-frequency signals like the data stream were not transmitted, only the configuration signals with a lower frequency could be send to the chips. Thus, the only reliable tests were I–V curves for the substrate HV and whether the power consumption increases when a chip is configured. Results on the sensor performance for an injection signal or a radioactive source could not be obtained.

A chip is approved for the prototype if the supply currents increase to the expected level in the configured state and if the breakdown voltage is higher than 20 V. This value is the baseline HV for the integration run because the chips with a substrate sensitivity of 200 Ω cm have an early breakdown at around 25 V. In the end, 54.5 % of the tested chips are accepted for ladder production.

7.3.2 Ladder Testing

Visual Inspection

Each ladder is visually checked after assembly. In some cases damages on individual chips are observed. The reasons are manifold:

- Cracks that evolve with time after gluing
- Handling mistakes that damaged chips
- Glue spilled over a chip edge, hence, the chip broke after removal from tool

In total 52 % (14/27) of the ladders have at least one damaged chip for the PCB ladders. All 27 ladders are bonded without electrically connecting damaged chips.

The low mechanical yield originates mainly from the more difficult handling compared to the silicon heater ladders. Since the assembly procedure for the final vertex detector is not following the procedure used here, this low yield is not characteristic for the final production. The limited amount of parts implies, however, that ladders with non-functional chips have to be used for the integration run.

status	# chips
functional	88
non-functional	20
physically damaged	10
not configurable	4
8b10b errors	5
no HV connection	1

Table 7.1: Status of the functionality of the MuPix10 sensor installed in the vertex detector prototype.

Functionality test

The ladders are tested by configuration and readout via a FEB, as used in the integration run DAQ. Each half-ladder is tested separately. I-V characteristics of the substrate HV and the configuration of every chip are tested in the same ways as for single chips on the probe station outlined before. For every ladder, the data quality of all three data lines is monitored. The data stream is 8b10b encoded such that single-bit errors can be detected. If the 8b10b error counter increases for a data link, the corresponding third of the chip is considered as not functional.

The DAQ software and firmware to operate the 6-chip ladders via a FEB was under development during the detector construction. It was finalized just after barrel assembly. Thus, only some outer ladders are irradiated with a ^{90}Sr source to test their response. For all chips tagged as *functional*, these tests show a consistent hit map and timestamp distribution for beta irradiation.

For the vertex detector prototype, the 18 most functional ladders are selected. The results of their functionality tests after barrel assembly are summarized in Table 7.1 and Figure 7.12. A fraction of 81.5 % chips is classified as functional regarding data quality, configurability and breakdown voltage with no direct implication on the detection performance.

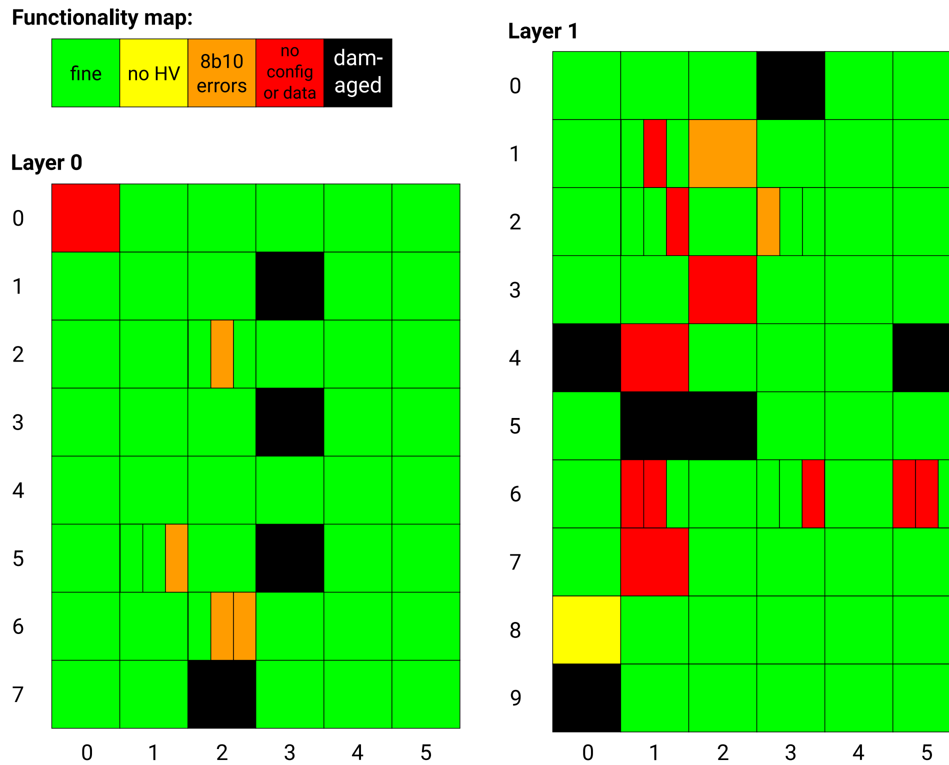


Figure 7.12: Functionality map of the vertex detector prototype; vertical axis: ladder ID; horizontal axis: chip ID. Chips divided into three parts have a different functionality for their corresponding sub-matrices.

The Mu3e integration run 8

The Mu3e integration run is the first time that detector prototypes are operated inside the Mu3e magnet at the πE5 beam line at PSI, which will also be used for phase I of Mu3e. The goals pursued in this campaign are to operate all prototypes under the final conditions like helium atmosphere, magnetic field, muon beam, etc. The DAQ system is operated for the first time for a high number of MuPix chips (larger than 8) recording particles emerging from muon decays on a stopping target.

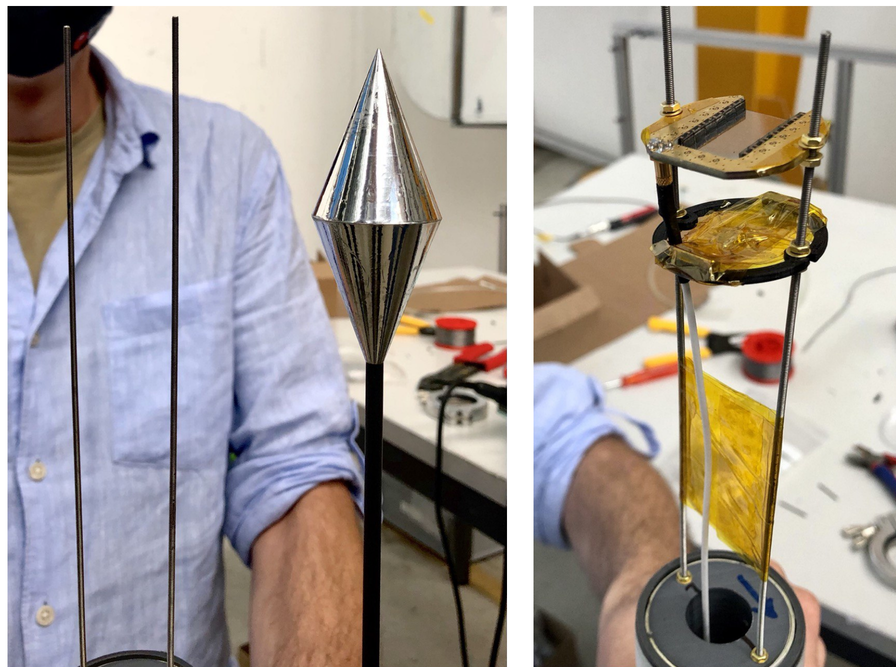
In this chapter, data obtained from the vertex detector prototype for two runs is presented. In the first run, the Mu3e target in the nominal magnetic field of 1 T is used. In the second run, a μSR target (magnetized silver sample paired with a scintillator located US) in absence of a magnetic field is used. Correlation data of hits in L0 and L1 demonstrate the functionality of the DAQ and give information about the target-to-detector alignment.

8.1 Measurement setup

The vertex detector prototype and its services are described in chapter 7. The πE5 beam line and the Mu3e solenoid are described in chapter 4. Here, specific conditions of the integration run are described, namely the used targets, the grouping of pixel ladders to FEBs and the chip configuration. Two SciFi modules were integrated around the vertex detector prototype but could not be fully configured in the integration run setup.

8.1.1 Beam rates and targets

During the integration run, a reduced beam rate of $1.5 \times 10^6\,\mu^+/\mathrm{s}$ on the target is exploited for the Mu3e solenoid on and $7 \times 10^5\,\mu^+/\mathrm{s}$ for the solenoid off. Two different targets are used (Figure 8.1). First, the double-cone stopping target designed for Mu3e phase I is deployed for runs with the magnetic field on, resembling the Mu3e conditions. Second, a μSR probe is used as stopping target, only for magnetic field off. It consists of two discs with a thin scintillator mounted on the US disc and a magnetized silver sample mounted on the DS disc. The scintillator of this target



(a) Double-cone target (right) next to bare mounting structure for μSR target.

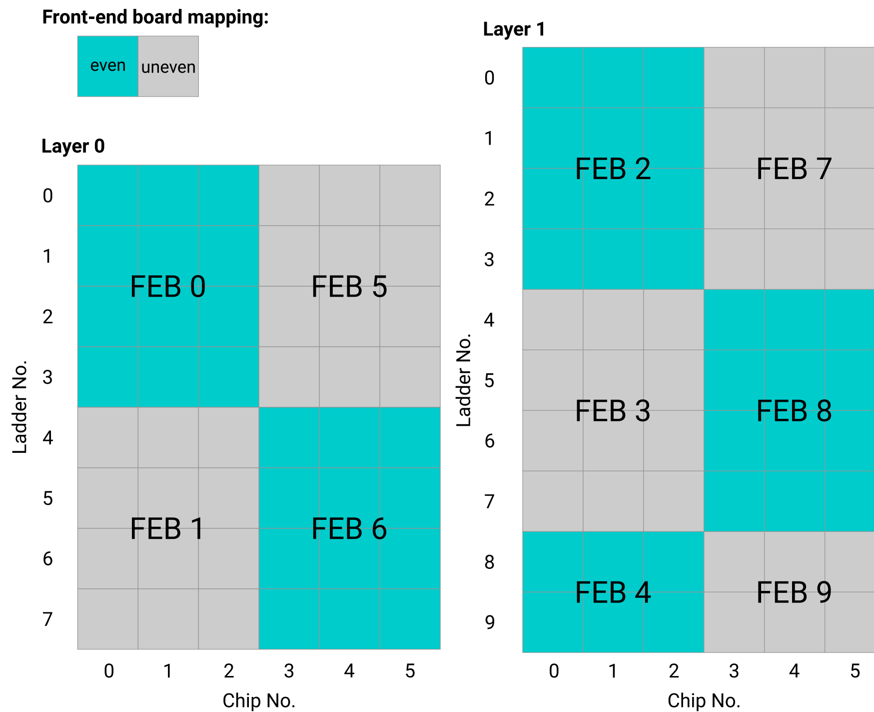
(b) μSR target with scintillator (1st disc, top) and silver target (2nd disc).

Figure 8.1: Targets used in the integration run.

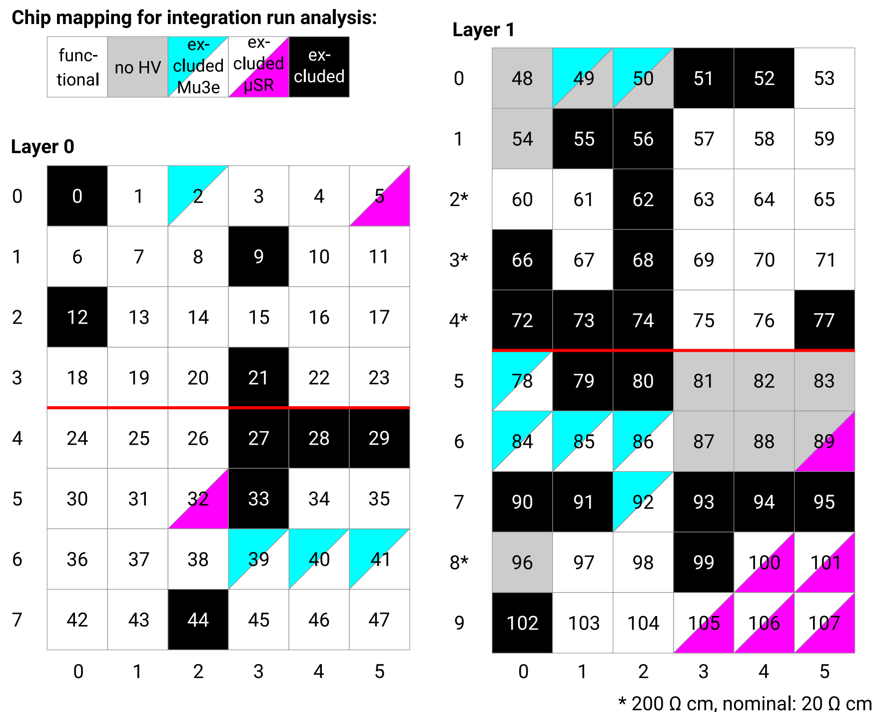
can be used to tag time frames when a muon enters the target region by passing the scintillator.

8.1.2 Ladder grouping and chip numbering

The data readout of the detector is connected to five FEBs on each side, US and DS. The chip numbering and the mapping to FEBs is shown in Figure 8.2. In the lower sketch, it is indicated if a chip is considered in the correlation data analysis in section 8.2. Chips are excluded when they are damaged, not connected or sending corrupted data. Some chips are excluded for individual runs mainly because they were not properly configured. For the analyzed run with magnetic field and Mu3e target, FEB 3 has been unreachable. For the run without magnetic field and the μSR target, FEB 9 has been unreachable. To recover the connection to a FEB, the inside of the magnet had to be accessed. Grey marked half-ladders are operated without biasing the substrate due to high leakage currents on the corresponding HV lines or shorts. The corresponding chips are included in the data taking but are expected to have a lower efficiency.



(a) FEB mapping of the vertex detector prototype. Odd and even FEB numbers colored for better visualization.



(b) Chip IDs of the vertex detector prototype inside the Mu3e solenoid; vertical axis: ladder number; horizontal axis: chip number. The red line separates the upper and lower hemisphere. Excluded chips for either both or individual target configurations are colored in black, pink and cyan, respectively. Chips without HV applied are colored in gray.

Figure 8.2: FEB and chip mapping of the vertex detector prototype.

8.1.3 Chip properties and configuration

All chips are powered with an external supply voltage of 2 V and their substrate is biased with −20 V as long as HV is not disabled as indicated in Figure 8.2. The supply voltage is sensed on the ladder PCB. Four ladders are equipped with chips with a resistivity of 200 Ω cm, namely Ladders 2, 3, 4, and 8 of L1. All other chips have a resistivity of 20 Ω cm.

During the integration run, around 90 % of the functional chips worked out-of-the-box. The chip configuration is set to the same default adjustable chip digital-to-analog converter values (chip DACs) for every chip. In the scope of the integration run, no chip tuning is performed. MuPix10 studies, which were on-going in parallel, have shown significant internal voltage drops on the chips and found optimized chip DACs. For the used settings, however, the expected detection efficiency for the individual chips of the vertex detector prototype is <50 %. Despite the loss of efficiency, correlation studies could still be done, as will be shown in the following section.

The temperature reading from the diode on the MuPix10 chips is not used in the analysis. The diode is located in the chip periphery, where very locally the chip temperature is comparably high. The purpose of this particular diode is to be integrated into the power interlock, not to give a representative measurement of the chip temperature. Calibration approaches to convert the values to the temperature of the active matrix, or to the average temperature of the periphery were inconclusive. Two additional temperature sensitive circuits specified to measure the temperature would be accessible if the chip could be operated via the Mu3e slow control, which is not possible for this module prototype, as described in section 4.3.1.

8.2 Correlation data

The correlation data analysis of the integration run is divided into two parts. First, general chip-to-chip correlations are analyzed that show which sensors are superposing for L0 and L1. In a more detailed analysis, the column-to-column correlations between the two tracking layers are studied. They correspond to the hit positions on the z-axis parallel to the beam. The resulting correlation patterns are compared to simulations and the target positions are determined from the data.

The hits recorded by the MuPix chips are sorted in time and assigned to 11-bit time frames[1]. These time frames are subdivided into 7-bit subheaders resulting in 4-bit (128 ns) time windows. The correlation plots are filled only for successive hits in time within the same subheader. Chips from the exclusion list (Figure 8.2b) as well as noisy pixels are excluded for the correlation plots. A noisy pixel is defined as having a hit rate 10 times higher than the average on the corresponding chip. In addition, a ToT cut is applied for small ToT as noise rejection.

[1] The timestamps are 8 ns apart, a time frame corresponds to 16.384 µs.

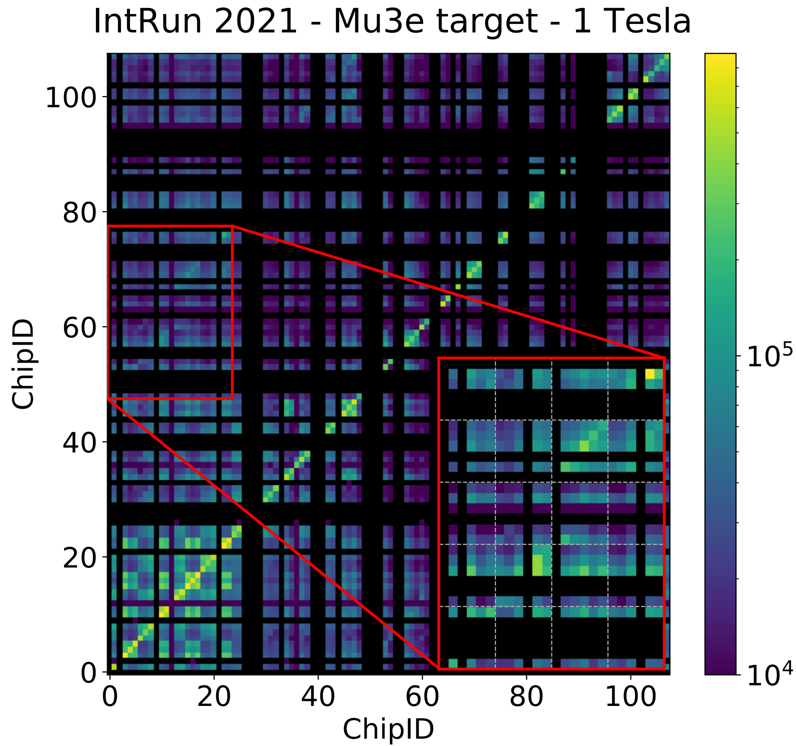


Figure 8.3: Chip-to-chip correlation for the Mu3e target with a 1 T magnetic field. The zoomed-in area shows a two-band structure of L0-to-L1 correlations.

8.2.1 Chip-to-chip correlations

The correlation data for the Mu3e target and the Mu3e solenoid providing a magnetic field of 1 T is shown in Figure 8.3. The self-correlations on the main diagonal originate from clusters and cross talk. The former are multiple hits detected by a chip on neighboring pixels due to charge sharing. The latter are fake hits caused by cross talk on the transmission lines from pixel cells to the periphery. Both effects cause an adjunctive hit in the same time frame, thus enhancing self-correlations on chipID level. The zoomed-in area in Figure 8.3 shows the correlation between chipIDs 0 to 23 and 48 to 77 with L0 on the horizontal and L1 on the vertical axis. This corresponds to L0-to-L1 correlations of all chips of the upper hemisphere. The grid in the area indicates the ladderID of each chip. A two-band structure in the L0-to-L1 correlation is visible. The band structure, however, is not very distinct. The bent particle tracks with varying radii disperse the chip-to-chip correlations. The origin of the pattern is discussed below for the μSR target data. During this run, the DAQ system favored data packages from individual FEBs while others were lost. In this case, the occurrence of data from FEB 5 is strongly enhanced resulting in the checkerboard pattern in the lower left corner of the correlation plot.

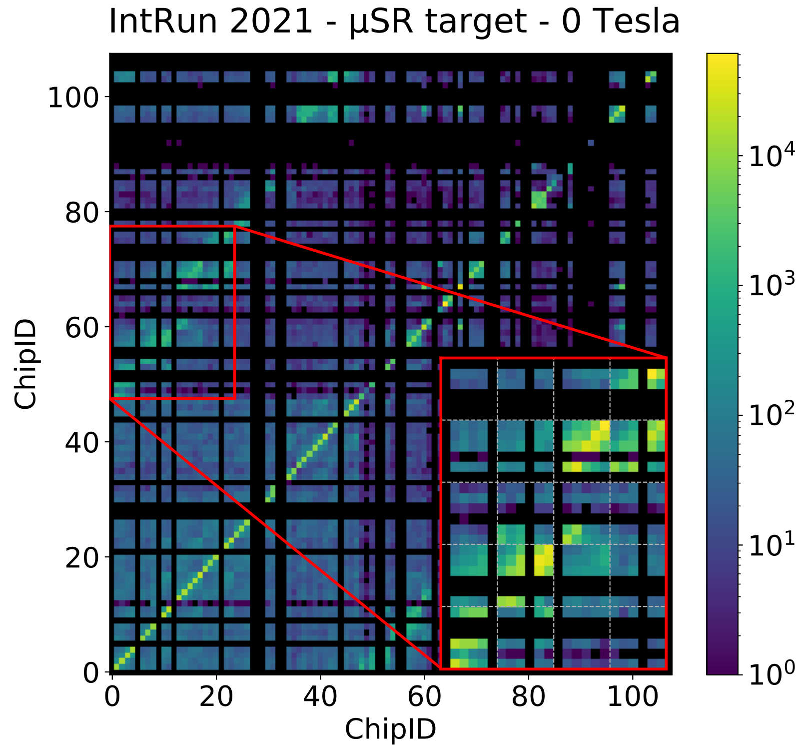


Figure 8.4: Chip-to-chip correlation for the μSR target without magnetic field. The zoomed-in area shows a two-band structure of L0-to-L1 correlations.

For the μSR target and no magnetic field, straight particle tracks originate from the target. Thus, more distinct chip-to-chip correlations are expected in contrast to the Mu3e target with a magnetic field with bent particle tracks. The correlation data for the μSR target is shown in Figure 8.4.

The same key features appear in the correlation data, like the main diagonal and the two-band structure on the secondary diagonal. No FEBs are favored by the DAQ in this run. On the secondary diagonal, the two-band structure is much more distinct. Ladders 0 & 1 of L0 correlate mainly to Ladders 0 & 1 of L1. For Ladders 2 & 3 of L0, correlations to two ladders each within L1 are clearly visible. The reason is the geometry of the vertex detector prototype, as sketched in Figure 8.5. Ladders 0 & 1 of L0 are superposing with Ladders 0 & 1 of L1. Ladders 2 & 3, the other L0 ladders of the upper hemisphere, are not explicitly superposing with one ladder of L1 but rather with two. This results in the observed two-band structure.

8.2.2 Column-to-column correlation (target position)

The column address of a hit corresponds to its z-position. For a particle hitting both tracking layers, the two column addresses can be used to point to the target/origin

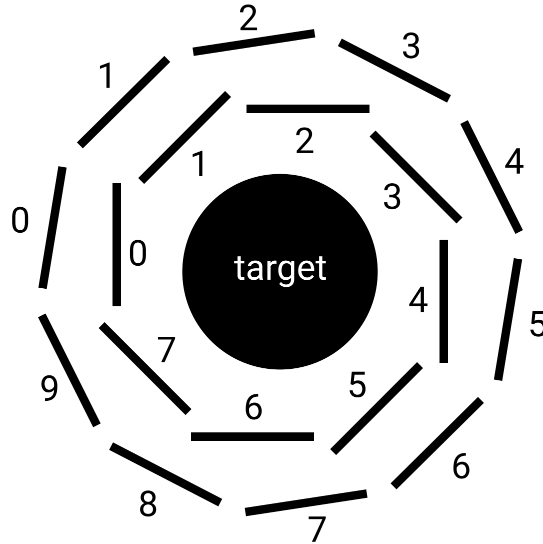


Figure 8.5: Sketch of the ladder positions for the vertex detector prototype in the x-y plane (deviates from Mu3e baseline design, cf. Figure 6.20).

of the particle. In this section, the column addresses are given as global addresses $\mathrm{col}_{\mathrm{global}}$, which are defined as:

$$\mathrm{col}_{\mathrm{global}} = (\mathrm{col}_{\mathrm{local}} + \ \mathrm{chipID} \cdot \mathrm{N}_{\mathrm{columns}})/\mathrm{N}_{\mathrm{columns}} \tag{8.1}$$

with $\mathrm{N}_{\mathrm{columns}} = 256$ the number of columns per chip, and the chipID taken from Figure 8.2b. For example, the 128th column on Chip 1 has the global address $\mathrm{col}_{\mathrm{global}} = 1.5$, including information about the corresponding chip and its relative position on the chip.

For both target geometries, a 2D simulation realized in Python of the expected pattern of the column-to-column correlations is performed. The target position and the tracking layer radii are defined and drawn in the y-z plane. For simplification, only the upper hemisphere is considered and the radius is kept at the minimum radius of a chip (cylindrical approximation). The target and detector thicknesses are assumed to be zero and no scattering is considered. Particles are "generated" as lines by assigning their intersection with the target and their slope based on a random generator. For a magnetic field, the bending radius of the particles needs to be considered. Thus, the momentum of the decay particles is assigned by a random generator weighted by the Michel spectrum[2]. The intersection of the generated particle tracks with the tracking layers is then calculated and plotted in a 2D histogram. The column addresses assigned in the simulation ($\mathrm{col}_{\mathrm{Layer0/1}}$) are also defined as global addresses (cf. equation 8.1), ranging from 0 to 6:

[2]The probability distribution follows: $P(x) = x^2((3-2x) - P_\mu \cos\vartheta(1-2x))$ for x from 0 to 1, with $P_\mu = 0.9$ as muon polarization, and ϑ as decay angle. (cf. equation 1.1)

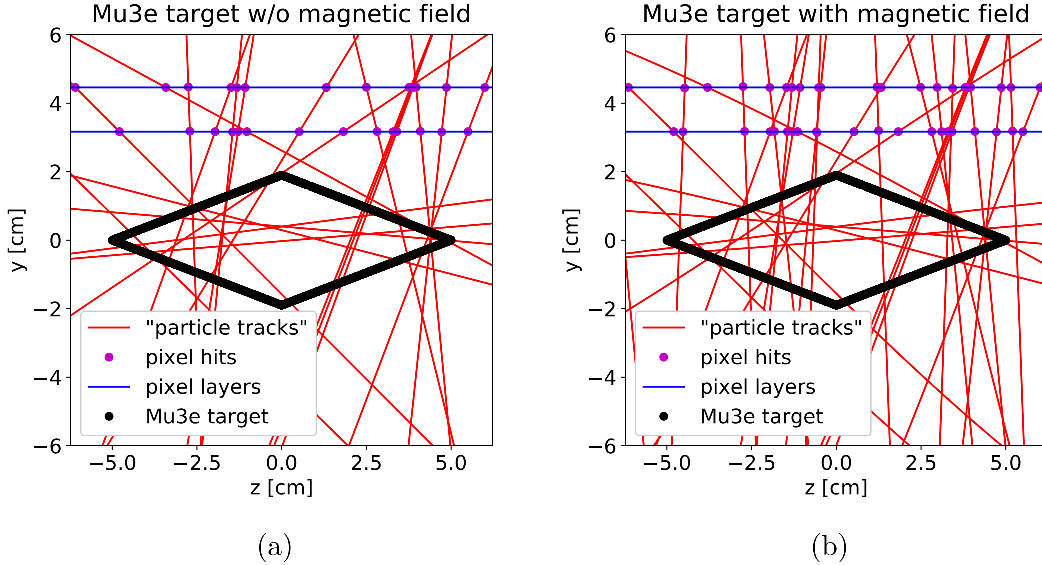


Figure 8.6: Event display of simulated muon decays for the MU3E target, a) without and b) with a magnetic field of 1 T applied. In Figure C.1, a zoomed-out version of (b) is shown to visualize the recurling tracks.

$$\mathrm{col}_{\mathrm{Layer0/1}} = (z_{0/1} - b_{US})/\mathrm{chip\ pitch} \tag{8.2}$$

with $z_{0/1}$ the z-positions where the "particle track" crosses L0/L1, $b_{US} = -62.23$ mm the US border of the active pixel area, and a chip pitch of 20.76 mm for the vertex detector prototype.

In Figure 8.6, the event display of simulated muon decays for the MU3E hollow double-cone target is displayed with and without magnetic field. 20 "particle tracks" from the same seed are shown. The enhanced occupancy for the magnetic field due to recurling tracks is clearly visible.

The event display of simulated muon decays for the μSR target is shown in Figure 8.7, this time for 50 generated "particle tracks". The disc spacing d_z is chosen to be 2.5 cm, the disc radius is 1.9 cm analogous to the MU3E target.

For the 2D correlation histograms, 100,000 particles are generated. In the case of a magnetic field, the maximum number of recurlers for a particle track is limited to 10 in order to reduce the occupancy from a single particle with an inclination angle $\vartheta \approx 90°$. In the real detector, the particle will lose energy due to scattering, particularly when hitting the PCB material, which justifies this assumption.

The simulated column-to-column correlations between L0 and L1 for the MU3E target are shown in Figure 8.8. In the absence of a magnetic field (Figure 8.8a), the plot shows simply the geometrical acceptance for two hits recorded by the tracking layers. The side bands indicate the z-position of the target. They originate from the geometrical acceptance for particles emerging from the cone tips. Shifting the target in US or DS direction shifts the crossing point of the side band with $\mathrm{col}_{\mathrm{Layer\ 1}} = 0$.

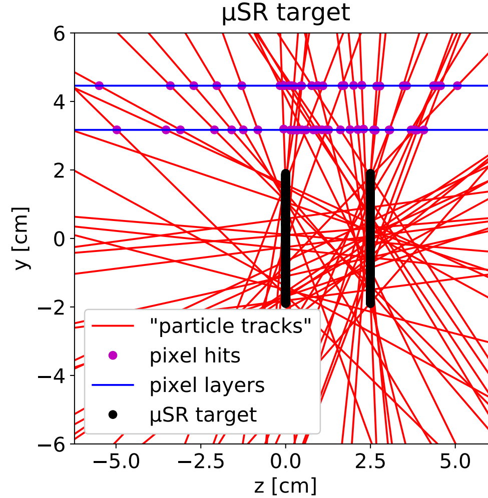


Figure 8.7: Event display of simulated muon decays for the μSR target.

For the μSR target , no simulation with a magnetic field is carried out, since the magnetized silver sample can not be used inside a magnetic field.

In Figure 8.9, the simulated column-to-column correlations for the μSR target are shown. A distinct two-band pattern is visible. The crossing points of the two bands with the main diagonal (Figure 8.9b) correspond to the z-position of the two target discs. Translating the global column address to the z-coordinate, this gives $z_0 = 0.0\,\mathrm{cm}$ and $z_0 = 2.5\,\mathrm{cm}$, which matches the geometry shown in Figure 8.7.

Now, the measured column-to-column correlations from the integration run are discussed and compared to the simulation. The correlations shown in Figure 8.10 are obtained for Ladder 2 of L0 and Ladders 2 and 3 of L1. They are chosen because they visualize the correlation pattern the best. Correlation plots from other areas of the detector can be found in the appendix C.

In Figure 8.10a, the correlations are displayed for the Mu3e target within a magnetic field. The main diagonal in the upper half and a side band for $\mathrm{col}_{\mathrm{global}} = 67 - 68$ are clearly recognizable. Also for $\mathrm{col}_{\mathrm{global}} = 60 - 62$, the side band and a part of the main diagonal can be recognized. The data fits the simulated correlation pattern for the Mu3e target. The distinct main diagonal clearly points to the presence of recurlers due to the magnetic field.

In Figure 8.10b, the correlations are displayed for the μSR target for the same ladder combination. The predicted two-band structure originating from the scintillator and the silver target planes can be recognized. The crossing points of the bands with the main diagonal (cf. Figure C.2) are at $\mathrm{col}_{\mathrm{global}} \approx 15.7$ and $\mathrm{col}_{\mathrm{global}} \approx 16.9$. Thus, the location of the μSR target has not been centered inside the vertex detector, which would correspond in this case to $\mathrm{col}_{\mathrm{global}} = 15.0$, but in the DS direction for the integration run. The distance of the two target planes can be determined by:

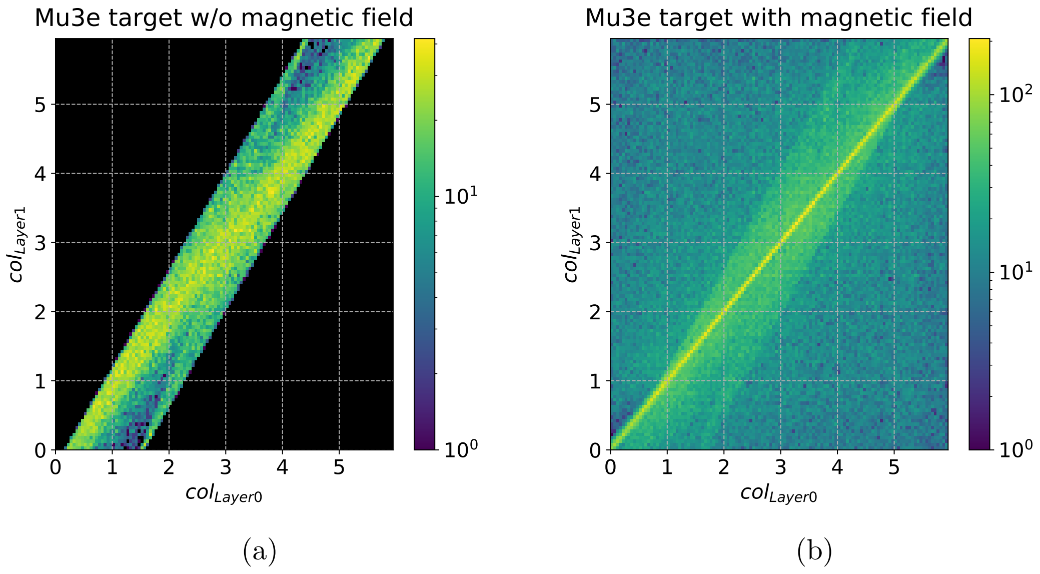


Figure 8.8: Simulated column-to-column correlations for the Mu3e target with and without magnetic field. $\mathrm{col}_{\mathrm{Layer0/1}}$ are defined as global column addresses (cf. equation 8.2).

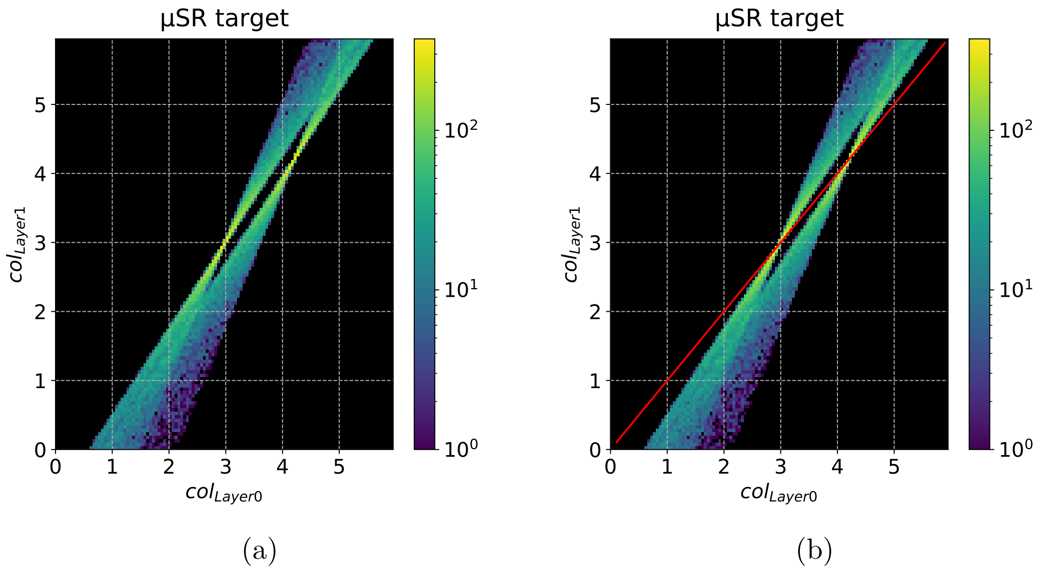
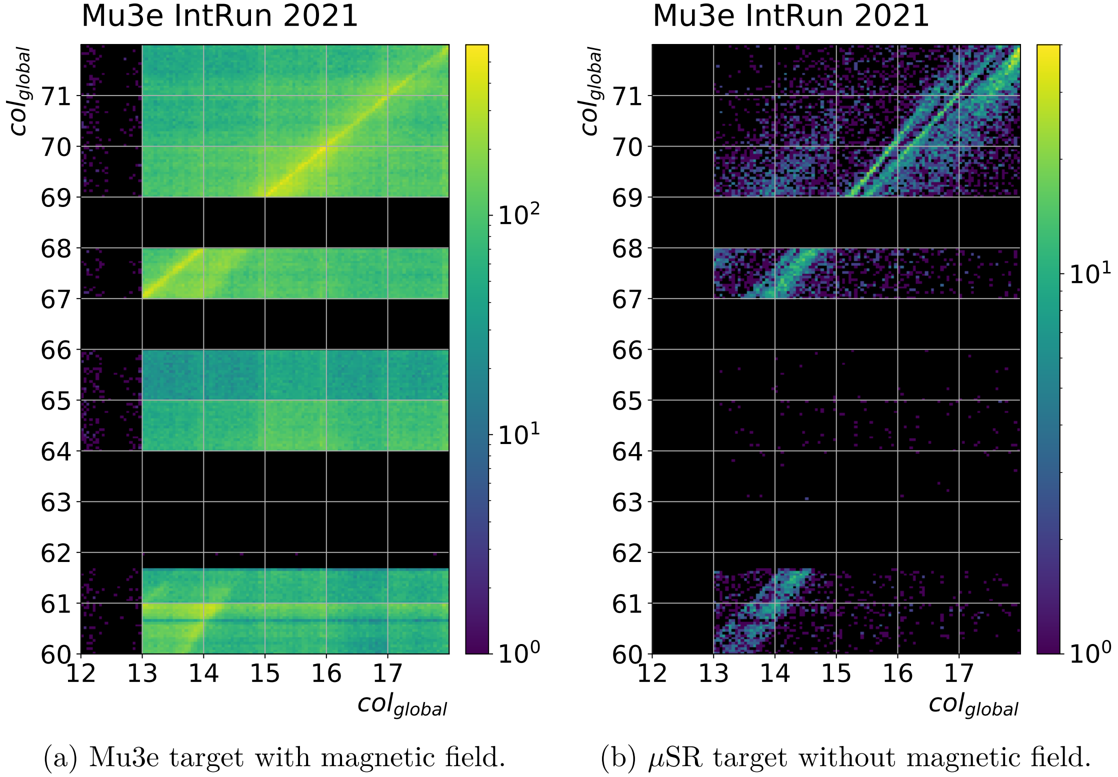


Figure 8.9: Simulated column-to-column correlations for the μSR target. In (b), the main diagonal is visualized by a red line. Its crossing points with the two bands correspond to the z-positions of the target discs. $\mathrm{col}_{\mathrm{Layer0/1}}$ are defined as global column addresses (cf. equation 8.2).



(a) Mu3e target with magnetic field.

(b) μSR target without magnetic field.

Figure 8.10: Measured column-to-column correlations between Ladder 2 of L0 to Ladders 2 & 3 of L1 for both targets. The global column address $\mathrm{col_{global}}$ is defined in equation 8.1.

$$d = (\mathrm{col_{global,sci}} - \mathrm{col_{global,Ag}}) \cdot \text{chip pitch} \approx 2.5\,\mathrm{cm} \tag{8.3}$$

Analogously, the longitudinal Mu3e target position can be determined from the correlation data. First, the simulation in Figure 8.8b is repeated for target displacements from -2 cm to $+2$ cm in z-direction. The position of the side band maximum at $\mathrm{col_{Layer\ 1}} = 0$ is determined for every position of the target. The result is shown in Figure 8.11.

The side band maximum for the measured correlation data is displayed in Figure 8.12. It shows the same data as in Figure 8.10a, however only the first two bins on the y-axis are filled into the histogram. $\mathrm{col_{global}}$ is converted to modulo 6. This way, only the relevant z-position of the column is displayed. The peak position is found to be at $\mathrm{col_{global}}\%6 = 1.7$, which translates to a target displacement of $+0.5$ cm to the central position (displaced toward the DS direction).

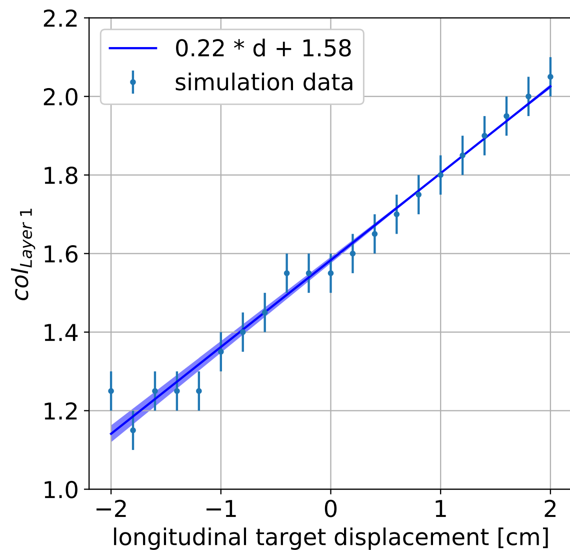


Figure 8.11: Simulated longitudinal target displacements in cm vs. position of the side band maximum in $\text{col}_{\text{Layer 1}}$ for the Mu3e target.

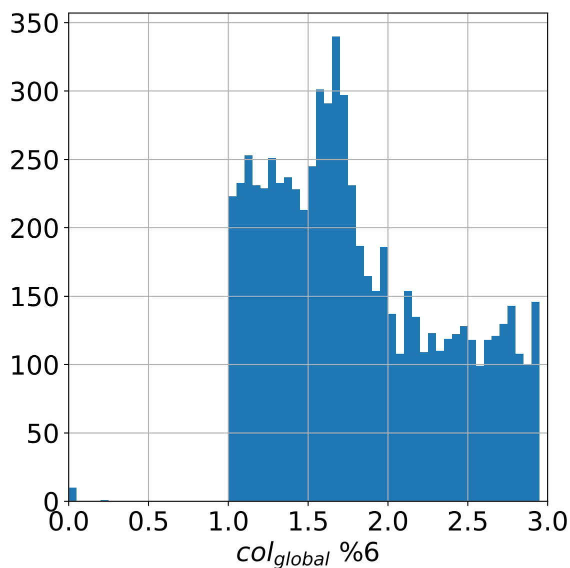


Figure 8.12: Histogram of data from Figure 8.10a, with only the first two y-axis bins considered. Longitudinal Mu3e target position can be retrieved from the peak position of the correlation side band with help of Figure 8.11.

8.3 Summary and outlook

The integration run was the first time a detector prototype was operated in Mu3e-like conditions. The vertex detector prototype produced functioning data. The consistency of the measured correlation data between the two tracking layers and simulation studies have successfully demonstrated the vertex detector readout. Chip-to-chip correlation as well as correlations on sub-chip level result in the expected geometrical effects. The longitudinal target positions can be determined from the data. Unfortunately, a detailed time analysis like the measurement of the muon lifetime has not been possible. The assignment of timestamps for hits in the target scintillator is corrupted for the obtained data.

In the near future, a repetition of the integration run is planned with functional prototypes of the SciFi and SciTile detectors. By reordering the PCB ladders on the vertex detector prototype, the amount of superposing chips of L0 and L1 will be increased. By adjusting the chip powering and the chip DACs, the detection efficiency is expected to increase well $>90\,\%$, which would strongly promote tracking for recurling tracks that hit the two pixel layers twice. In addition, a setup is under construction to provide services for the Mu3e detectors for weeks outside the beam area such that measurements detecting cosmics with the vertex detector prototype over a long time period are in reach for 2022.

Part V

Conclusion

Conclusion 9

The search for physics beyond the SM motivates a variety of experiments at the high-intensity frontier of particle physics. The Mu3e experiment aims to search for the CLFV decay $\mu^+ \to e^+e^-e^+$ in the near future. This decay is heavily suppressed in the SM with an expected branching ratio of $< 10^{-54}$.

CLFV searches like Mu3e are motivated by the lepton-flavor violations observed in the neutrino sector and lepton flavor asymmetries observed in boson decays at the b-factories LHCb and Belle-II. An observation of $\mu^+ \to e^+e^-e^+$ would be a clear signature of new physics, while no observation would lead to strong limits on allowed models beyond the SM.

Mu3e aims to exploit the branching ratio of $\mu^+ \to e^+e^-e^+$ down to $2 \cdot 10^{-15}$ in phase I. This would improve the current limit of 10^{-12}, set by SINDRUM in 1988, by almost three orders of magnitude. To reach this sensitivity, the detector needs to be fast and granular enough to distinguish events from 10^8 muon decays per second. In addition, an extremely low material budget in the order of 0.1 % of a radiation length per detection layer is required. The momentum and vertex resolution is dominated by multiple Coulomb scattering for the low-energetic decay products emerging from muons decaying at rest. Four pixel layers equipped with HV-MAPS are used as an ultra-thin tracking detector. The corresponding MuPix sensors, with an active size of $\sim 2 \times 2\,\text{cm}^2$, were specifically developed for this experiment. They are thinned to 50 µm and provide a high detection efficiency paired with an excellent time resolution of (6 ± 1) ns. To keep the material budget at a minimum, HDIs made of aluminum-polyimide laminates serve as only support structure and guide power and signal lines.

This thesis focuses on the Mu3e vertex detector made of the inner two pixel layers with 108 chips in total. The presented studies comprise the construction of detector mock-ups, thermal studies verifying the novel gaseous helium cooling system, and the construction and operation of a first functional detector prototype.

Within the scope of this thesis, two types of detailed thermal-mechanical mock-ups of the vertex detector have been constructed by the author to study the realization of the helium cooling system. First, the tape heater mock-up is made of

structured aluminum-polyimide tapes that are resistively heated. To resemble the final detector, the tapes are equipped with 50 µm thin steel plates. Second, the silicon heater mock-up consists of silicon heater chips, which are thinned to 50 µm. The chips are powered and read out via HDIs like the pixel chips in the final experiment. The heater chips are heated resistively and equipped with a resistive aluminum thermometer. The vertex detector has an expected heat dissipation of around 220 mW/cm^2. The cooling system is designed to handle a heat dissipation on the chips of up to 350 mW/cm^2. The components of the vertex detector are graded for temperatures up to 70 °C.

The thermal studies using the tape heater mock-up have been carried out by Marin Deflorin at FHNW. They show that a single gas flow between the two layers is insufficient. This has led to a geometrical change of the gas supply, such that an additional gas flow surrounding the second layer is introduced.

The detailed thermal studies exploiting the silicon heater mock-up have been carried out by the author. The transient temperature behavior for powering on and off the detector is studied. The temperature curves can be described mainly by a dominant time constant τ_0 of 2 s to 3 s. The fast response of the detector temperatures enables a safe operation. A thermalized detector can be obtained with a safe and reliable turn-on procedure in less than 5 min. Temperature maps of the silicon heater mock-up are obtained for heat loads of 215 mW/cm^2 and 350 mW/cm^2. In both cases, every chip has a temperature difference to the inlet temperature well below 70 K. The maximum reached is around 55 K. The average temperature differences for the two heat dissipation values are 20.5 K and 32.2 K for L0, and 14.9 K and 24.2 K for L1, respectively, for the nominal flow direction. The average temperatures reached, when the flow direction is inverted, agree within 1.1 K to the nominal flow configuration. The temperature map measurements are compared to CFD simulations for the conservative scenario of 350 mW/cm^2. The average temperatures of the simulations are lower by 6 K. The maximum temperature differs by 26 K for L1 and by around 18 K for L0, with the warmer temperatures reached in the measurements. The simulation assumes an idealized detector geometry and neglects the thermal properties of the detector support. Imperfections in the detector geometry might enhance non-uniformities in the flow distribution. Regions with reduced gas flow are expected to form hot spots. The results show that their formation is difficult to predict by simulations. Thus, the characteristics and the severity of local hot spots have to be always tested with the physical detector.

The dependence of heat load and temperature is found to be linear for each chip position in both tracking layers. This enables the possibility to estimate the temperature change when the chip configuration in the experiment has to be adjusted. The nominal helium mass flow of 2.0 g/s can be reduced to 1.8 g/s with a resulting temperature increase of less than 10 %. Going to an even lower mass flow, the flow distribution inside the detector begins to change. This affects in particular the flow distribution between L0 and L1.

The detailed thermal-mechanical mock-up studies successfully verified the functionality of the novel helium cooling concept for the Mu3e vertex detector. All

temperatures are well inside the specifications. However, before operating the final detector close to the specification limit of 350 mW/cm^2, the manifestation of the gas flow distribution needs to be measured to exclude any chip passing the temperature limit. Similar studies for the outer pixel layers are in preparation in Liverpool/Oxford for which the author manufactured the dedicated tape heater ladders. The corresponding results, which will conclude the thermal studies of the Mu3e pixel detectors, are expected in the near future.

Beside the thermal studies, the silicon heater mock-up serves also as a proof-of-concept for the final detector construction. The used components can be regarded as mechanical equivalents to the final parts. The assembly procedure is foreseen to be the same as for the final detector. The main challenge is to construct the sensor ladders with high precision in a simple and reproducible way. The low number of only 18 ladders that form the vertex detector triggered the decision to construct the detector in a manual approach. The tooling to position and glue chips to the ladder, and to construct modules have been developed/refined by the workshop at the Physics Institute Heidelberg and the author.

The chip placement precision can be summarized with a chip gap size of (80 ± 4) µm, and a lateral displacement of (9 ± 3) µm between the chips. The values agree with the maximum allowed variation of 5 µm on the chip gap, as well as the maximum allowed lateral displacement of 13.5 µm. The average glue thickness of the silicon heater ladders is measured to be (5.3 ± 1.7) µm without any systematic irregularities. This corresponds to the aimed value of 5 µm, which is motivated to keep the material budget of the detector at a minimum. The ladder construction is verified to be highly precise using a cost-effective manual assembly procedure. Next to the ladder assembly, also the module assembly has been validated.

The spTAB bonding procedure has been established on a semi-automatic bonding machine in Heidelberg. The production has revealed issues in the bonding process. Micro-cracks on the chip's backside are induced by the bonding process. Furthermore, the bonding parameter optimization has been insufficient and resulted in lift-offs of individual bonds. Both observations have to be tackled prior to the final detector production to ensure a high quality of the ladders.

The silicon heater project successfully demonstrates that the manual production approach fulfills all requirements. Beside the outstanding optimization of the spTAB process, the vertex detector production is ready to start as soon as the final chip, MuPix11, is produced. The construction procedure allows the production of one ladder per working day. Considering an overproduction of 100 % to account for spare modules and limited yield, a working time of only 9 weeks is expected for a full vertex detector.

In the last part of this work, a vertex detector prototype has been constructed by the author. It has been operated in a test beam campaign inside the Mu3e magnet at the final beam line of the experiment, the CMBL at the πE5 beam line at PSI. This integration run aimed to test the DAQ and the integration of the vertex

detector and its services inside the magnet. The experience gained from the silicon heater mock-up construction and parts of the tooling are used for the realization of this prototype. The main difference to the final detector is that PCBs ladders are used instead of the HDIs. In the integration run, many conceptually important operations have been demonstrated for the first time, including multiple MuPix chips operated on a single PCB, MuPix chips operated in a 1 T magnetic field, and an HV-MAPS detector cooled by gaseous helium during full operation.

The collected data has been analyzed focusing on correlations between the two detection layers. The correlation data between chips of L0 and L1 shows the expected pattern that results from overlapping chips of the two layers. The collected data includes two different target configurations: the Mu3e hollow double-cone target and a μSR target that can be described as two discs. Both target geometries and their positions along the beam axis are successfully reconstructed by chip column-to-column correlations. These correlations are compared to simulation results, which show the same pattern and help to find the target positions in the measurement data. The successful communication with the vertex detector prototype under Mu3e-like conditions verifies the relevant parts of the Mu3e DAQ. The pixel data has been collected with a continuous readout and stored successfully time-sorted.

The combination of thermal-mechanical mock-up studies and vertex detector prototype measurements demonstrate that the vertex detector cooling and the mechanical integration of the detector are ready for production. The detector production procedure has been established together with a QC procedure for the mechanical quality of the modules. In the next months, first final MuPix11 ladders are expected to be produced. This will be accompanied by the development of a detailed electrical QC procedure for the individual chip performances. With the electrical chip and ladder characterization as the last steps ahead, the work within the scope of this thesis paved the way for the detector production in 2022.

Part VI

Appendix

Tooling and manufacturing of the Mu3e vertex detector

This chapter describes the assembly procedure of the silicon heater mock-up used for the cooling studies described in chapter 6. It resembles the assembly procedure for the final Mu3e vertex detector. In the scope of this thesis, custom tooling for chip placement, ladder and module assembly has been developed and/or tested. The working steps to reach the Mu3e requirements (cf. section 5.1) regarding spatial precision and material budget have been defined and evaluated.

In this chapter, the focus is on the custom tooling. The main functionalities and the manufacturing procedure are described and presented for the silicon heater mock-up. The associated quantitative analysis of the silicon heater mock-up construction can be found in chapter 5. It shows that the detector construction could be successfully verified. A partially modified manufacturing procedure was used to construct the vertex detector prototype, as described in chapter 7.

A.1 Conceptual tooling design

The production of the vertex detector differs from large-scale projects, like for example the production of the outer pixel layers for Mu3e, due to its small number of chips and ladders. While for the outer layers the chip placement and ladder production is realized on a semi-automatic gantry, the vertex detector components are manufactured manually. The upsides of a manual production are cost-efficiency and less required resources to establish the production. However, quality and yield have to be assured by a clever design of the tooling and the manufacturing procedure.

As outlined in section 4.3.2, the vertex detector consists of: pixel chips forming ladders and ladders forming modules. For both ladder and module assembly, custom tooling has been designed, manufactured, and tested. For the final detector construction only minor changes on the tooling have to be realized, mainly due to the different dimensions of silicon heater chips and MuPix chips

All tools and working steps presented are developed in close collaboration with the mechanical workshop at the Physics Institute Heidelberg.

Figure A.1: Ladder assembly tool with a manufactured silicon heater ladder on the pedestal. Each chip has an individual vacuum channel. The micrometer screw rail is visible in the back. [22]

A.2 Ladder assembly

The design of the ladder assembly tool is motivated to be simple, precise and to reduce the chance of human error. It consists of a vacuum chuck with a pedestal for the pixel chips and a rail to attach a micrometer screw (Figures A.1 and A.2). On the pedestal, there are pin holes to fix the interposer flex circuits, and double-cross shaped vacuum holes for each chip. The vacuum for each chip is controlled individually by a valve. The individual working steps are described in more detail in the sections below.

Chip placement as well as gluing of the ladders is done on this tool. The alignment of all components is monitored using a digital microscope with an optical resolution of 1.5 µm.

A.2.1 Chip placement

An L-shaped brass slide for the chip placement is moved along the pedestal (Figure A.2). The slide is pressed to the steel base by a strong magnet. Each chip is pushed toward its final position with the slide. This way, the longitudinal position of the chip is determined by the slide wall. During chip placement the assembly tool is tilted by 30°. The slide is spring-loaded in lateral direction on the pedestal

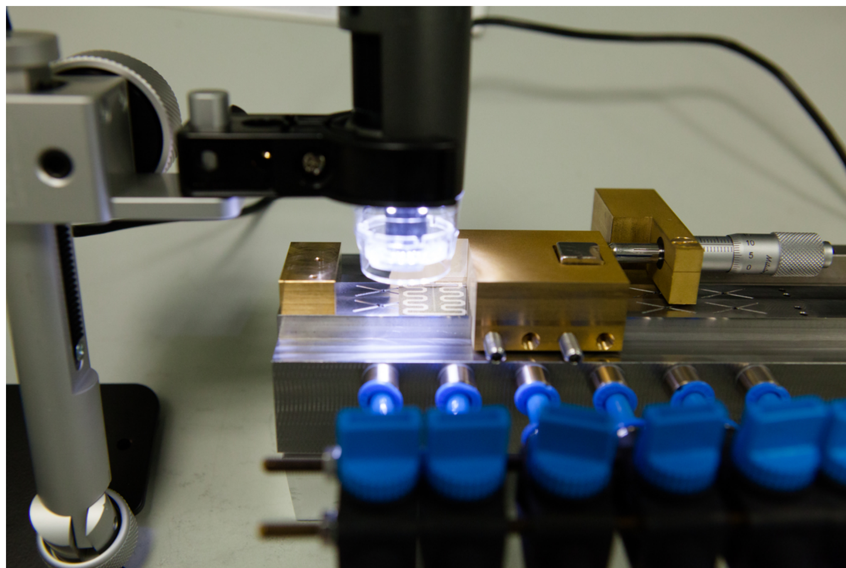


Figure A.2: Ladder assembly tool with silicon heater chip that is pushed into position by a brass slide using a micrometer screw. The brass stopping edge is visible on the left. A digital microscope monitors the chip position. [22]

(Figure A.3). This way, the horizontal bar of the slide is aligned with the pedestal edge. The slide confines therefore the longitudinal and lateral position of the chip.

When approaching the neighboring chip, the gap size is monitored with a digital microscope. The slide is moved by a micrometer screw that is attached to the rail parallel to the pedestal. When the aimed gap size is reached, the chip is fixed by vacuum and the slide is moved back to the initial position. When placing the first chip, a stopping edge is attached on the pin holder for the interposer flex circuits. The slide is moved until its horizontal bar touches the stopping edge. This way, all chips are positioned relative to the interposer flex circuit positions, which are determined by the pins on the tool. The overall procedure is visualized in detail in Figure A.4.

Intrinsic limitations on the precision

The ladder assembly tool has one main weak point. A non-perfect right angle at the L-shaped slide leads to slightly rotated chips. This results in small lateral displacements, as discussed in section 5.4.1.

Extensive metrology during pre-production is required to detect systematic effects. The production of a set of slides and choosing the one with the best alignment is foreseen for the final tooling.

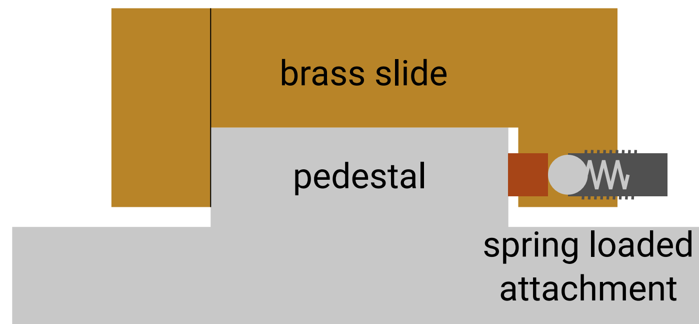


Figure A.3: Side view on the ladder assembly tool to illustrate spring loaded attachment of brass slide.

Risk prevention

Dust particles and scratches on the pedestal are considered as main risks for the ladder production. In the worst case, they can lead to cracks in the thin chips when fixing them by vacuum or when the weights are applied to distribute the glue. Before the assembly of a ladder, the tool has to be inspected for irregularities on the pedestal and cleaned such that no remnants are present. Also every chip has to be inspected for remnants that originate from the wafer cutting and thinning process or the chip testing procedure.

A.2.2 Chip gluing

The next working step is the gluing of the six chips, the interposer flex circuits, and the HDI. The ladder assembly tool is brought from tilted into planar position. Epoxy glue (Araldite 2011) is applied manually on the chips and flex circuits. The glue is distributed in small dots in a quincunx pattern on the chips (Figure A.5). This provides a more or less uniform glue distribution without covering the chip edges. This is particularly important since the bond pads are not allowed to be covered by glue. Spilled glue at the chip edge would glue the chips to the assembly tool, which must be prevented.

To obtain glue dots of similar size, a toothpick is dipped in epoxy and a few glue dots are first made on a sheet of paper or a foil. When the dots approach a constant size, the glue is applied with the toothpick onto the chips until the dot size starts to decrease again. This technique results in an average glue thickness of around 5 µm (cf. section 5.4.2), which corresponds to the aimed value.

For the interposer flex circuits, glue is applied in each corner with an acupuncture needle as a single very small dot. It is crucial to not cover any bond pads, which leaves only 1 mm clearance for gluing.

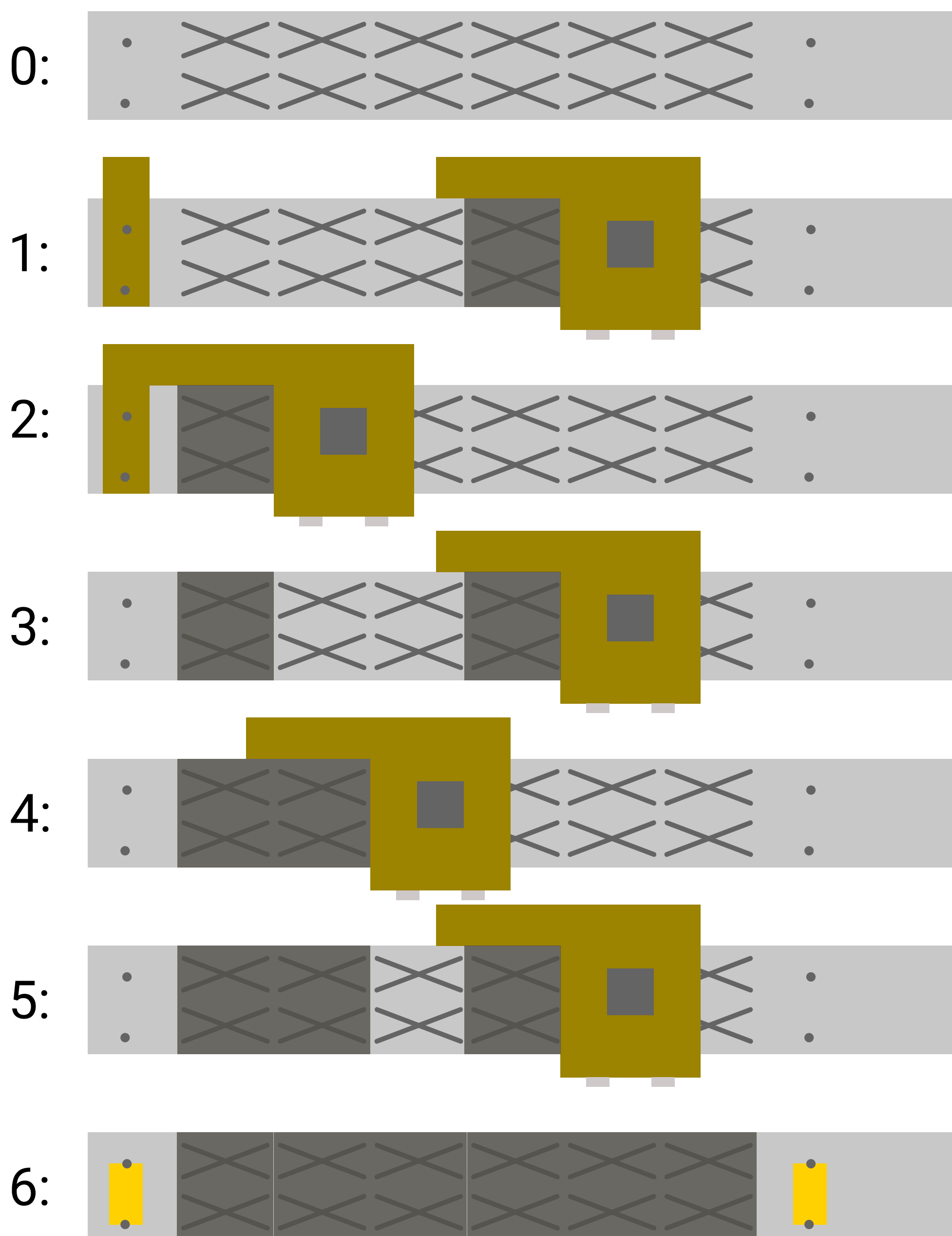


Figure A.4: Chip placement procedure:
(1) Stopping edge, chip & slide placement **(2)** Slide pushed to stopping edge, Chip #0 at final position **(3)** Slide pulled back, next chip placed **(4)** Chip #1 at final position **(5)** Slide pulled back, next chip placed **(6)** All chips placed, interposer flexes (yellow) attached to pins

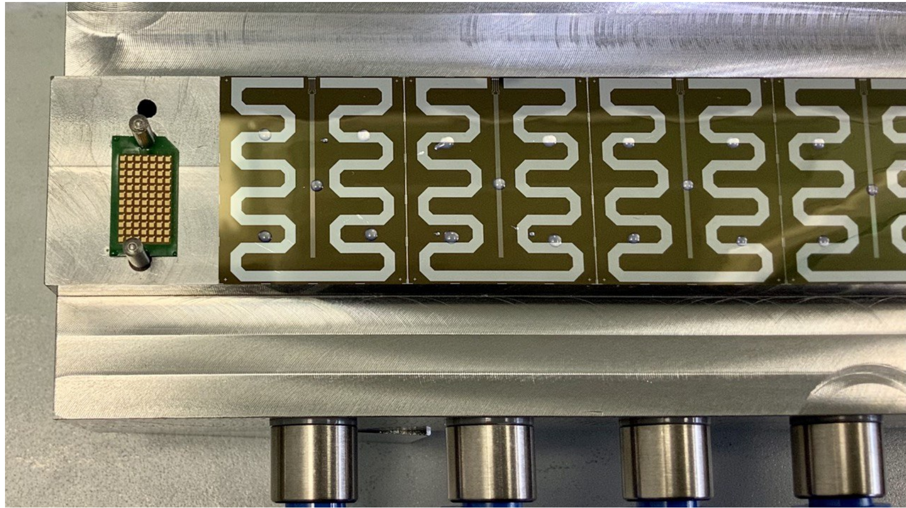


Figure A.5: Glue dots applied in a quincunx pattern on silicon heater chips and glue applied in small dots on the corners of an interposer flex circuit.

After gluing, the HDI is placed on the chips and interposer flex circuits. A coarse alignment is given by the cutouts of the HDI and the pin holders. The HDI is pressed carefully onto the chips.

For the silicon heater ladders the fine alignment has been performed manually by hand. The procedure works as follows: Fiducial marks on the HDI and the first heater chip are brought into superposition on one side of the HDI. The alignment is monitored with the digital microscope. A small aluminum cube is then placed on the HDI at the position of the aligned chip. This fixes to some extent the HDI position. The alignment of the fiducial marks is stepwise done for the remaining chips. Due to the small aluminum weights on parts of the HDI, moving the HDI by either the hand or a toothpick results in only small changes in position, which allows for a very precise stepwise alignment.

After aligning all six chips, the aluminum cubes are carefully removed and the alignment of all fiducial marks are re-checked. In case of a misalignment, the above procedure is re-done. If the alignment is satisfying, the aluminum weights are put back on the HDI. Additional brass weights are applied to reach a uniform and thin glue distribution (Figure A.6).

The ladder remains on the mounting tool overnight. After the curing time of the glue of around 12 h, the ladder is taken off and visually inspected.

Risk prevention

The manual gluing procedure implies the risk of damaging chips by direct contact or by spilling glue over the chip edges. Both limited the yield for the silicon heater ladder production. A few chips were broken, for example, by an aluminum cube that slipped off the hand and fell onto the HDI, or by a toothpick that was pressed on a chip. In two cases, the application of too much glue on a chip resulted in a

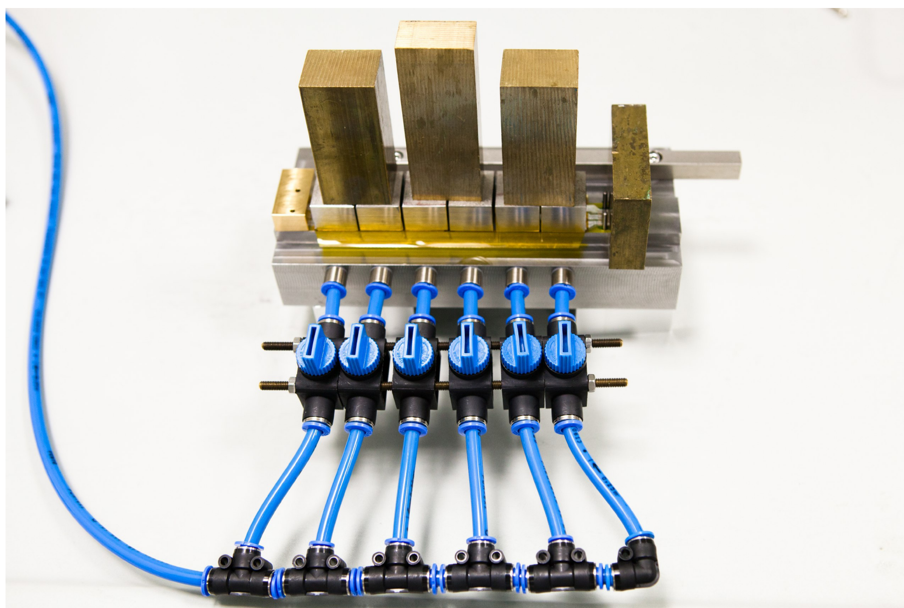


Figure A.6: Glue curing on the ladder assembly tool with weights applied to distribute the glue uniformly.

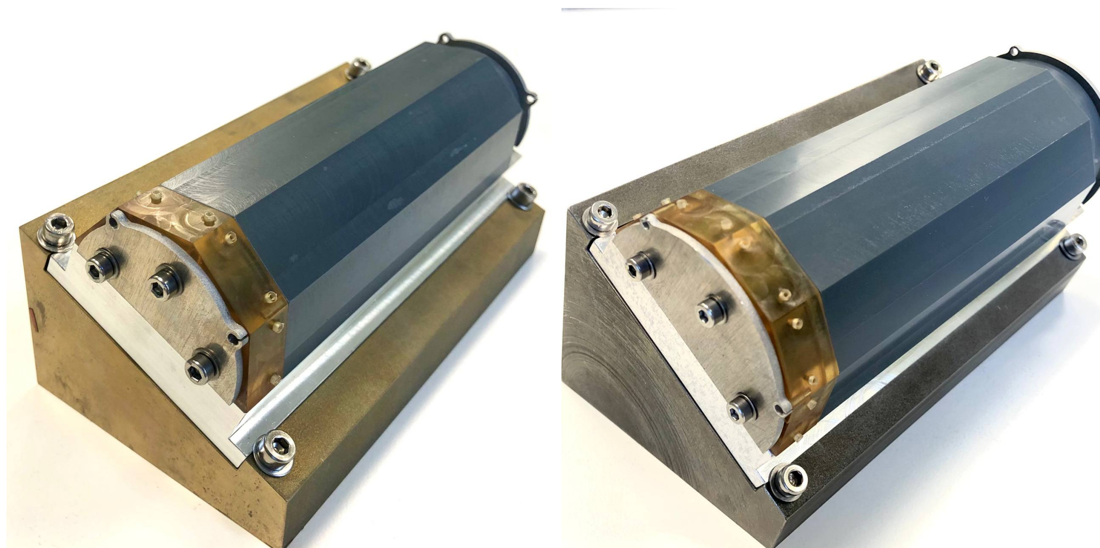
loss of a ladder. The glue spilled over the chip edge when the weights were applied. When removing the ladder from the assembly tool, the affected chips were broken. Both sources of errors are impossible to be fully circumvented but are considered to be controllable with sufficient training.

The described incidents occurred in the early stage of the silicon heater production. Handling the weights and applying a more uniform amount of glue were well under control after the full production. For the final detector production, the yield is considered to be acceptable despite the present risks (cf. the yield calculation in section 5.4.4).

A.2.3 Single-point Tape Automated Bonding

The electrical connection of the HDI to the interposer flex circuits and to the chips is established by spTAB (see Figure 5.25). The procedure is performed on a conventional wire bonding machine by replacing the bond wedge. On the HDI, there are cutouts in the polyimide layer at the bond pad positions of the chip. There, the aluminum traces can be pressed down on the bond pad by the bond wedge. By applying a defined bond force and ultrasonic power the trace and the pad form a junction.

After bonding, the quality of all connections on a ladder is tested. If a non-contacting bond is detected, the trace can be rebonded by repeating the bonding process. When a ladder passes the electrical test, the spTAB bonds are covered with epoxy glue for protection. This working step is foreseen for the final production but was not integrated in the manufacturing process of the silicon heater ladders.



(a) L0 module assembly tool. (b) L1 module assembly tool.

Figure A.7: Module assembly tools for L0 and L1. By rotating the base and the sliding block each facet of the detector module can face upwards.

A.3 Module and barrel assembly

A.3.1 Module assembly tools

Similar to the ladder assembly tool, the module assembly tools are designed to be simple and to ensure safe handling. In Figures A.7a and A.7b, the assembly tools for L0 and L1 modules are displayed. The tools consist of a solid base and a slidable block where the ladders are glued together. Each facet of the block can face upwards by either rotating the base, or moving out the sliding block and inserting it back after turning it around. Thus, for each working step the relevant parts are best accessible.

A.3.2 Module assembly procedure

In Figure 5.3, the relevant parts of the module assembly are visualized. During module assembly, the ladders are glued together with the passive gluing flaps integrated on the HDIs. On the two ends of each ladder, an interposer stack is constructed (Figure A.8), which establishes the electrical connection to the outside via the end-piece flex circuit.

The assembly works as follows: First, the PEI end pieces are attached to the assembly tool. The first ladder is placed with the gluing flap facing inward. The interposer flex circuits holds the ladder in place due to the circular cutouts matching the pins integrated in the end pieces.

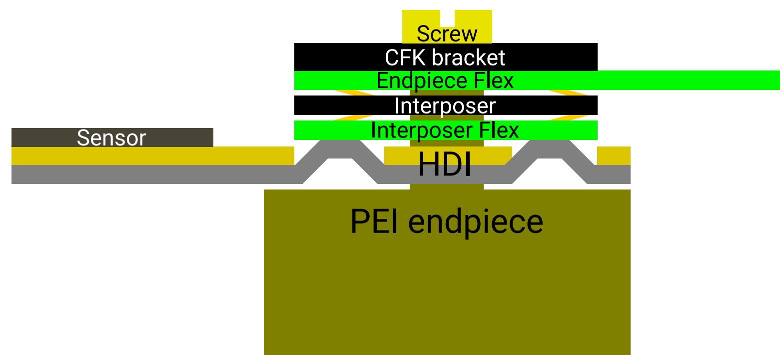


Figure A.8: Sketch of the stack at the vertex detector end pieces. Electrical connections are established from HDI to interposer flex by spTAB, and from interposer flex circuit to end-piece flex circuit by an interposer. The stack is compressed by a CFK bracket fixed by M1.2 brass screws. [22]

The next step is to mount the interposers (cf. section 5.2.1), one on each side, and place the end-piece flex circuits on top of the interposer stacks. This is followed by attaching the CFK brackets with M1.2 brass screws to the end piece. These brackets compress the interposer stack. After mounting the ladder, the end-piece flex circuit has to be bent back to make space for the next ladder to be mounted.

After the first ladder is mounted, the base of the tool is rotated and the sliding block is turned by 180° such that the second facet is pointing upwards. Glue is applied manually in small dots on the gluing flap of the first ladder. The gluing dots are kept at the same size as for gluing the chips. The second ladder is placed on the mounting tool. On one side, the interposer flex circuit is clipped to the end piece. Then the ladder is lowered slowly onto the gluing flap and the interposer flex on the other side is clipped as well.

To obtain a uniform glue distribution, as for the ladder assembly, weights are applied onto the ladder. Since in this case the silicon is facing upwards, PVC cubes are used as buffer material for the brass weights to avoid scratches on the substrate (Figure A.9). The curing time of around 12 h implies that one ladder is placed per day, resulting in an assembly time per module of 3 and 4 days for L0 and L1, respectively.

While taking off the assembled module, it is stabilized by an aluminum support including a handle. The module is placed until the integration into the experiment in a 3D printed transportation container, as shown in Figure A.10.

Risk prevention

The highest risk during module production is the screwing of the M1.2 screws into the end piece using a torque screwdriver. When the sharp tip slips off the screw and touches the chip, the silicon substrate can easily crack, which damages the overall

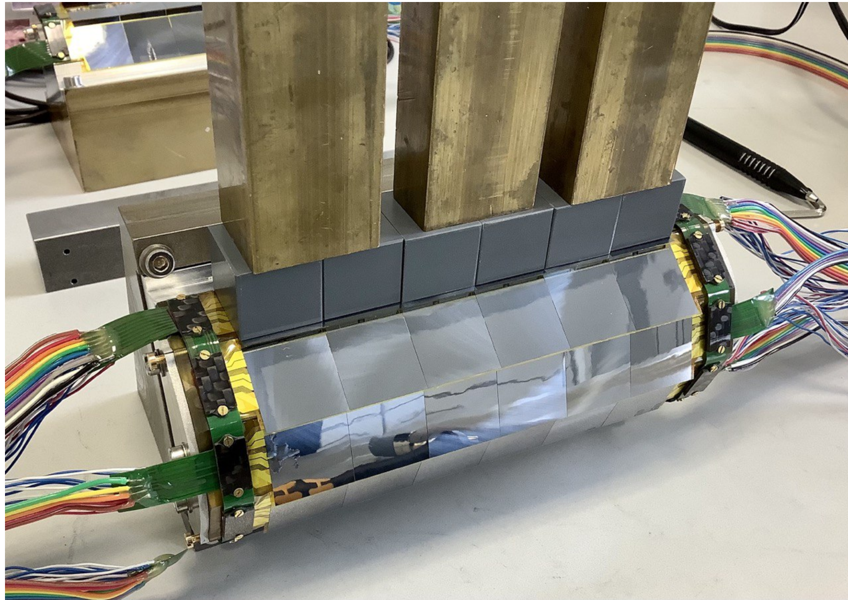


Figure A.9: Gluing of the last silicon heater ladder on a L1 module. PVC cubes are placed on the chips, additional brass weights are applied on top. The HDI of the ladder is glued to the gluing flap of the neighboring ladder. All interposer stacks are manufactured for this module.

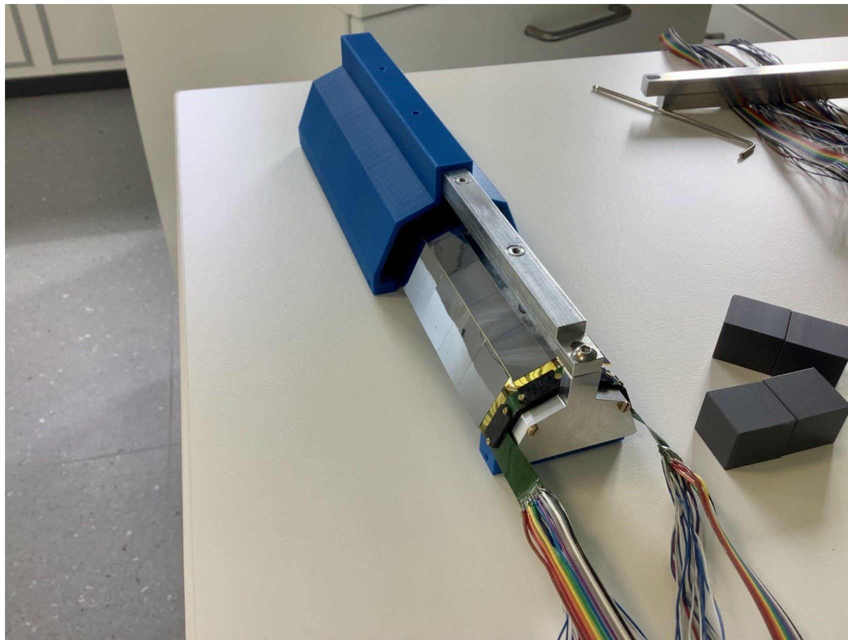


Figure A.10: 3D printed transport container for a L0 silicon heater module. The 3D printed base and cover assure stable and safe transport. The mounted aluminum handle is screwed to the end pieces and stabilizes the module.

module. For the final production, a holder to fix the screwdriver will be integrated into the assembly process. In addition, a PVC cube is placed on the chip next to the end piece to shield the delicate silicon from light material like the screws.

A.3.3 Barrel assembly

The pixel modules are mounted to the barrel-shaped detector directly on the beam pipe. As shown in Figure A.11a, first the mechanical support of the vertex detector has to be attached to the beam pipes. It consists of 3D printed gas distribution rings that guide the helium into the two flow channels, and a PEI end ring. The fixation of the distribution rings differs for US and DS: There is a fixed mount on the US side (left in Figure A.11a), and a spring loaded mount on the DS side (right), which tensions the detector modules. During detector mounting both mounts are not fixed and thus the support rings are movable along the beam axis. The modules are inserted onto the rings using a stabilizing carrying handle (Figure A.11b). This handle is mounted directly onto the end pieces by replacing two M1.2 screws of the interposer stacks.

The module is fixed to the support rings by brass screws that run parallel to the beam pipe. As visible in Figure A.11b, there is only little space in the gap between the beam pipe and support rings to attach these screws. Thus, the module is slided back and forth to maximize the space for screwing. The stress on the module is minimized by the carrying handle attached during the mounting procedure.

For the second module (Figure A.12), the experimental cage (or mini-cage for mock-ups) is rotated by 180°. The second module is lowered on the gas distribution ring. Special attention is paid to chips not touching the first module. The module is again fixed to the distribution rings and the handle is removed.

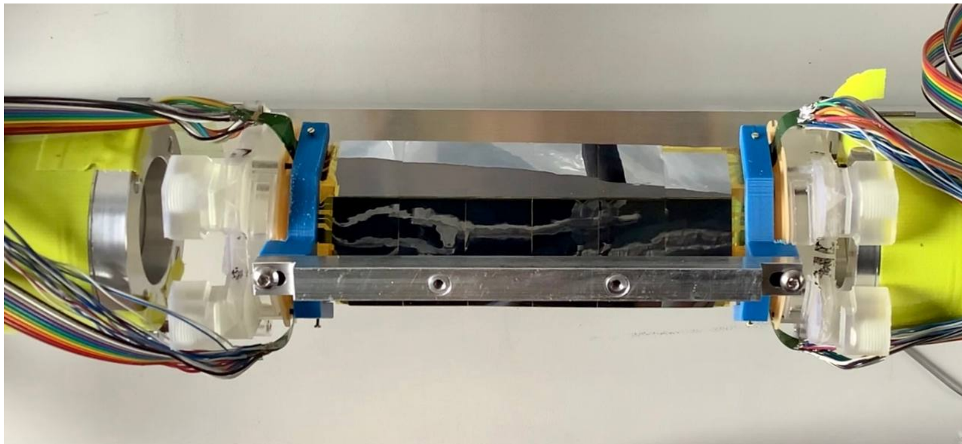
The same procedure is performed for the L1 modules. While placing these modules, the end-piece flex circuits of the inner layer need to be guided through the gap between the distribution rings and the L1 end pieces.

After all modules are mounted, only the confinement for the helium flow around L1 is missing. Two 3D printed hollow half rings, which guide the helium in axial direction, are clamped around each gas distribution ring As the last step, a 1-2 µm thin Mylar foil is wrapped around the vertex detector, glued on the hollow half rings (Figure A.13). For the silicon heater mock-up, a 25 µm thin polyimide foil was used instead of the Mylar, since it is easier to handle and the material budget plays no role for the mock-up.

Clearance issue

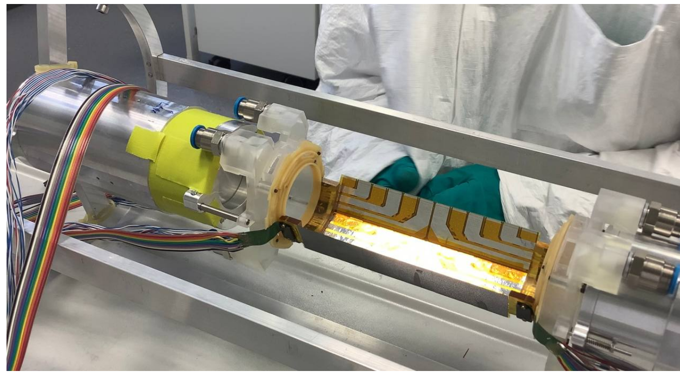
For the silicon heater barrel assembly, a chip of L0 was damaged while inserting a L1 module. Some silicon at the chip corner broke off since it got in contact with the L1 end piece, as shown in Figure A.14. During the barrel assembly, the vertex detector is not spring-loaded but stabilized by the carrying handles for module insertion. As

(a) Dummy beam pipe equipped with the 3D printed helium distribution rings that serve as mechanical support for the vertex detector.

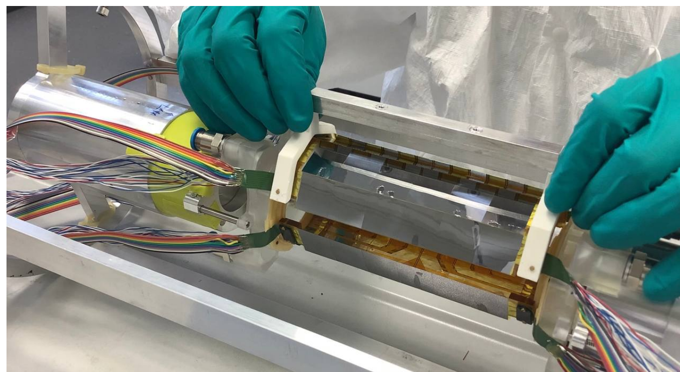


(b) A L0 silicon heater module, with a carrying handle attached, mounted to the helium rings.

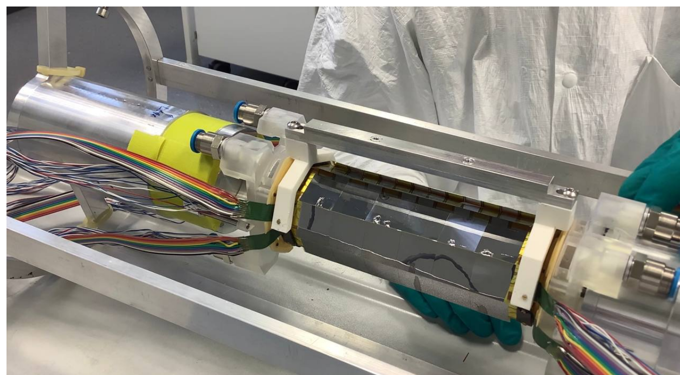
Figure A.11: Assembly of a silicon heater module onto the beam pipes.



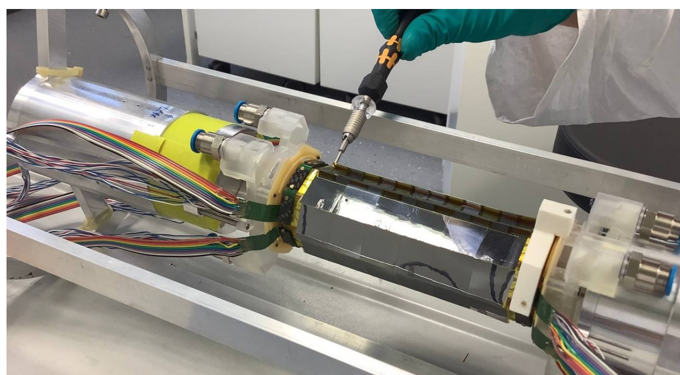
(a) First L0 module upside down in mini-cage.



(b) Lowering of second L0 module.



(c) Second L0 module in place.



(d) Removal of carrying handle.

Figure A.12: Assembly sequence of the L0 silicon heater barrel.

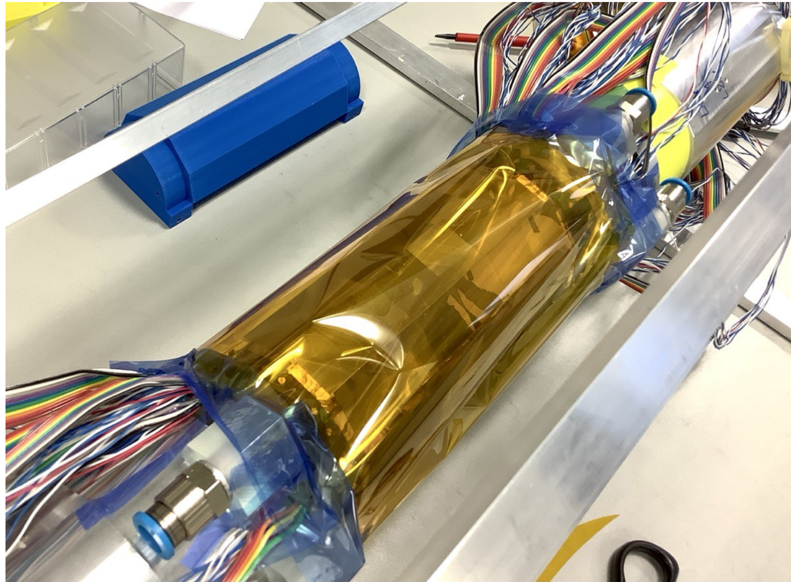


Figure A.13: Silicon heater mock-up with polyimide foil confining the helium flow.

visible in Figure A.14, the ladders are not strained. This was not considered for the clearance between L0 and L1, which leads to potential overlaps of chips and end pieces of the two layers. Two solutions can be approached: First, the cutout in the L1 end piece is made larger to fit the chips below. Second, a spring-loaded attachment of the vertex detector while barrel assembly is realized. The latter has to account for the mounting of the screws that connect the end rings and end pieces together. These screws, however, are only accessible on both sides when moving the vertex detector DS and US is possible. Both options will be evaluated prior to the final detector production.

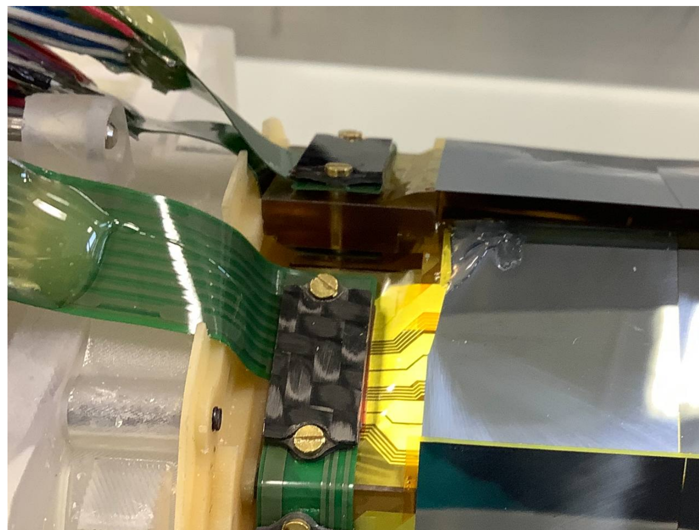


Figure A.14: Damage of a heater chip due to missing clearance between L0 and L1.

Silicon heater mock-up studies: additional plots and tables

B

In this chapter, additional plots of the helium cooling studies exploiting the silicon heater mock-up of the Mu3e vertex detector are presented. This includes:

- The temperature maps originating from the raw data in Figure B.1 and B.2. In contrast to the plots presented in section 6.4.4, the inactive chips are marked in red. (Section B.1)
- The corrected temperature maps originating in Figure B.3 and B.4. In contrast to the plots presented in section 6.4.4, the inactive chips are marked in red. (Section B.1)
- The polynomial fits of the temperatures measured for each ladder for the nominal flow in Figure B.5. They are needed for the correction described in section 6.4.1. (Section B.2)
- Temperature curves of for the power scan discussed in section 6.4.5. Figures B.6, B.7 and B.8 show exemplary the temperature data and the corresponding exponential fits for chips 0 to 5 of L0 Ladder 1. The results are used to obtain Figures 6.27 and 6.28 after applying corrections outlined in section 6.4.1. (Section B.3)

In addition, the raw data of the uncorrected temperature maps is given in section B.4.

B.1 Temperature maps with inactive chips marked

The corresponding plots are shown on the following pages.

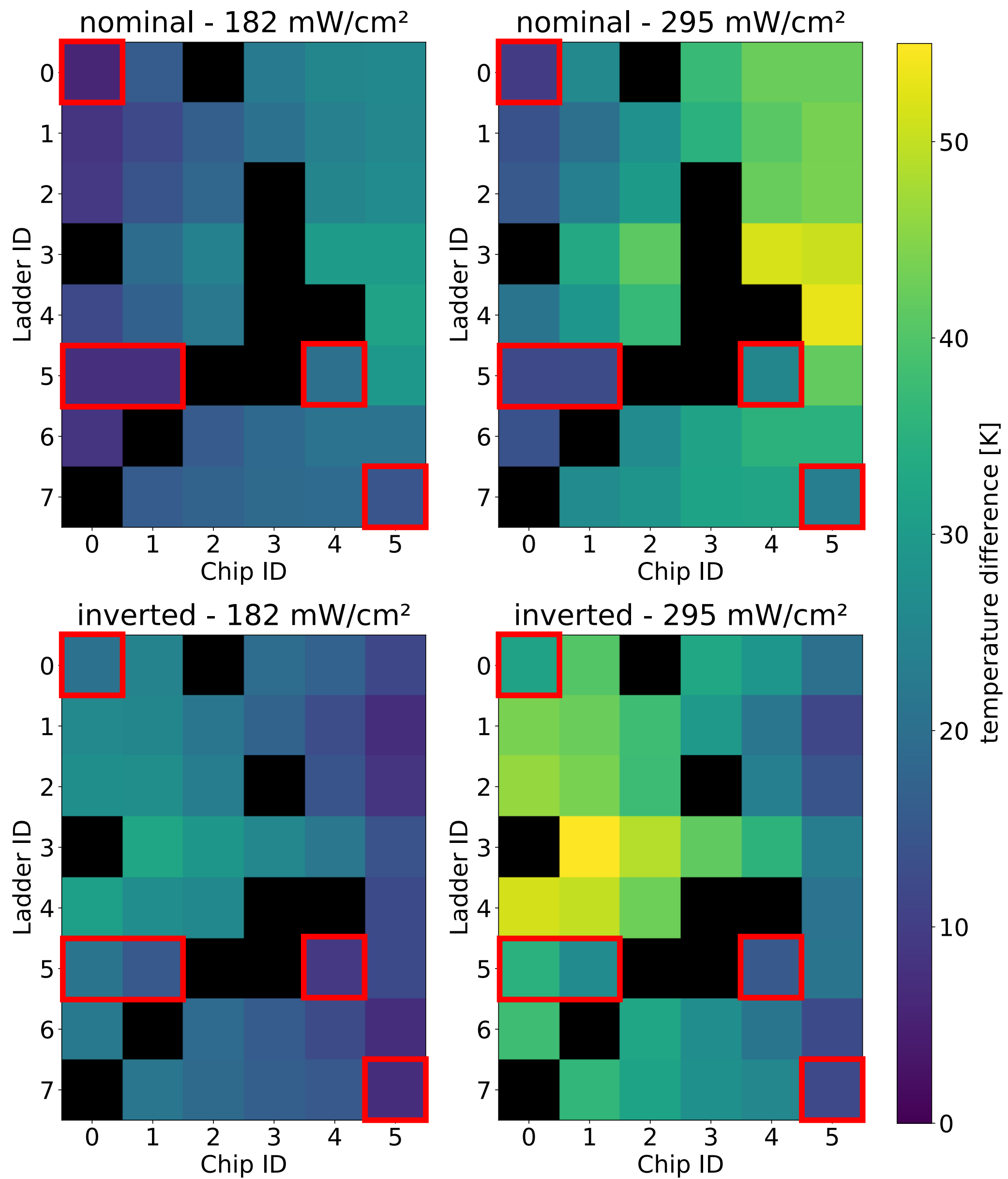


Figure B.1: Temperature maps of L0 of the silicon heater mock-up for nominal and inverted flow and heat loads of $182\,\mathrm{mW/cm^2}$ and $295\,\mathrm{mW/cm^2}$. Chips without temperature readout are marked black. Inactive chips are marked in red.

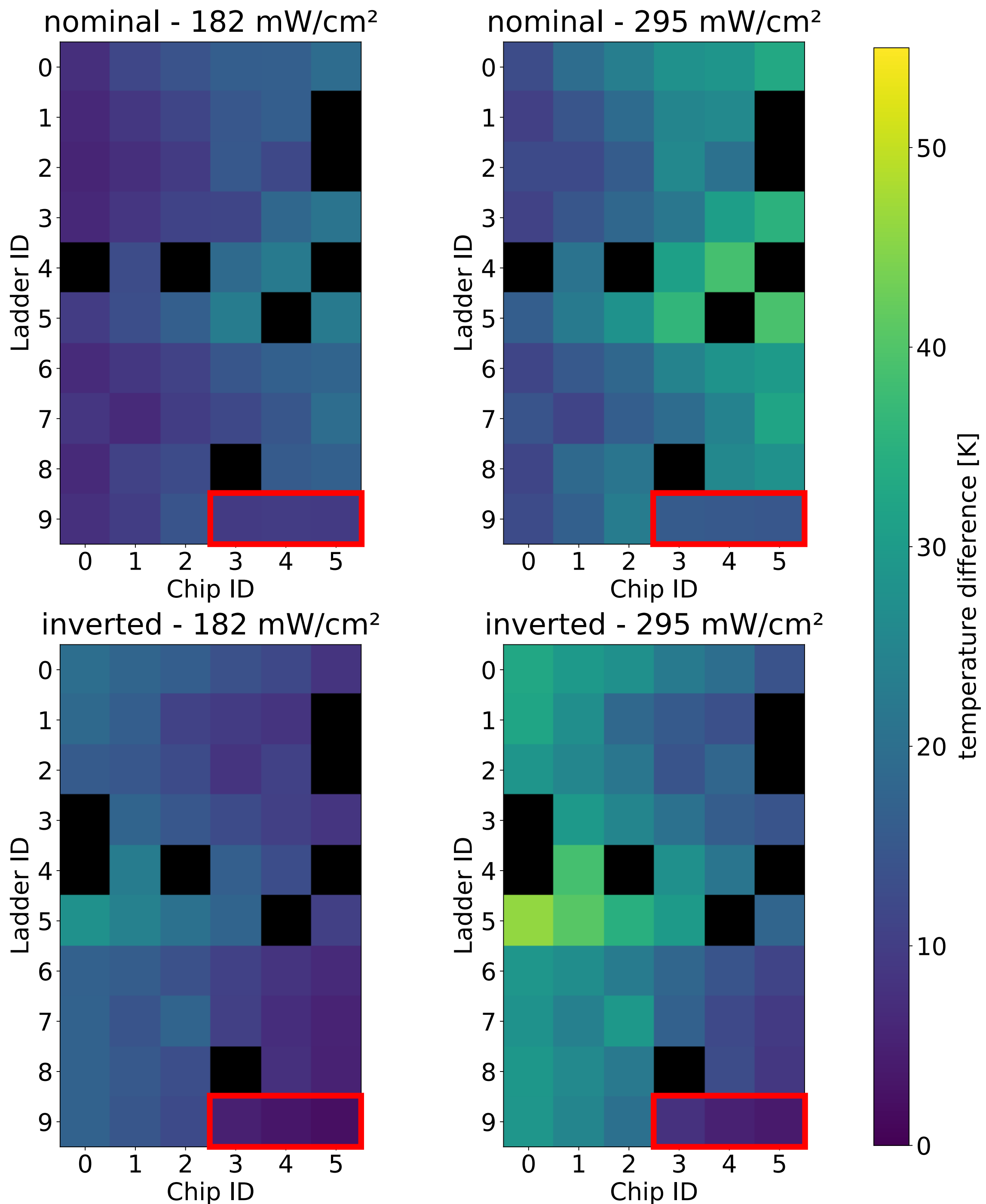


Figure B.2: Temperature maps of L1 of the silicon heater mock-up for nominal and inverted flow and heat loads of 182 mW/cm^2 and 295 mW/cm^2. Chips without temperature readout are marked black. Inactive chips are marked in red.

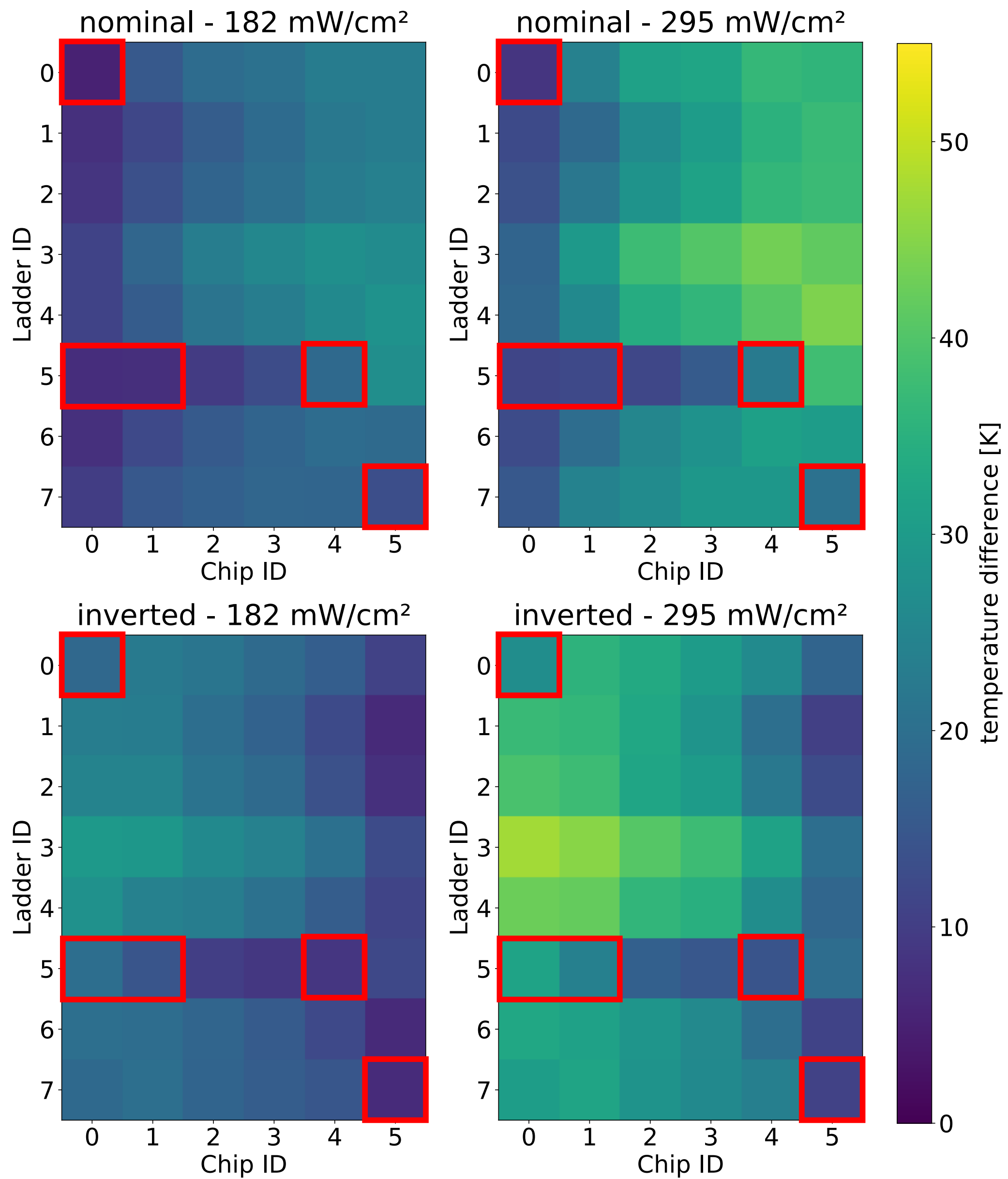


Figure B.3: Corrected temperature maps and interpolated results for chip without working readout of L0 of the silicon heater mock-up for nominal and inverted flow and heat loads of 182 mW/cm^2 and 295 mW/cm^2. Inactive chips are marked in red.

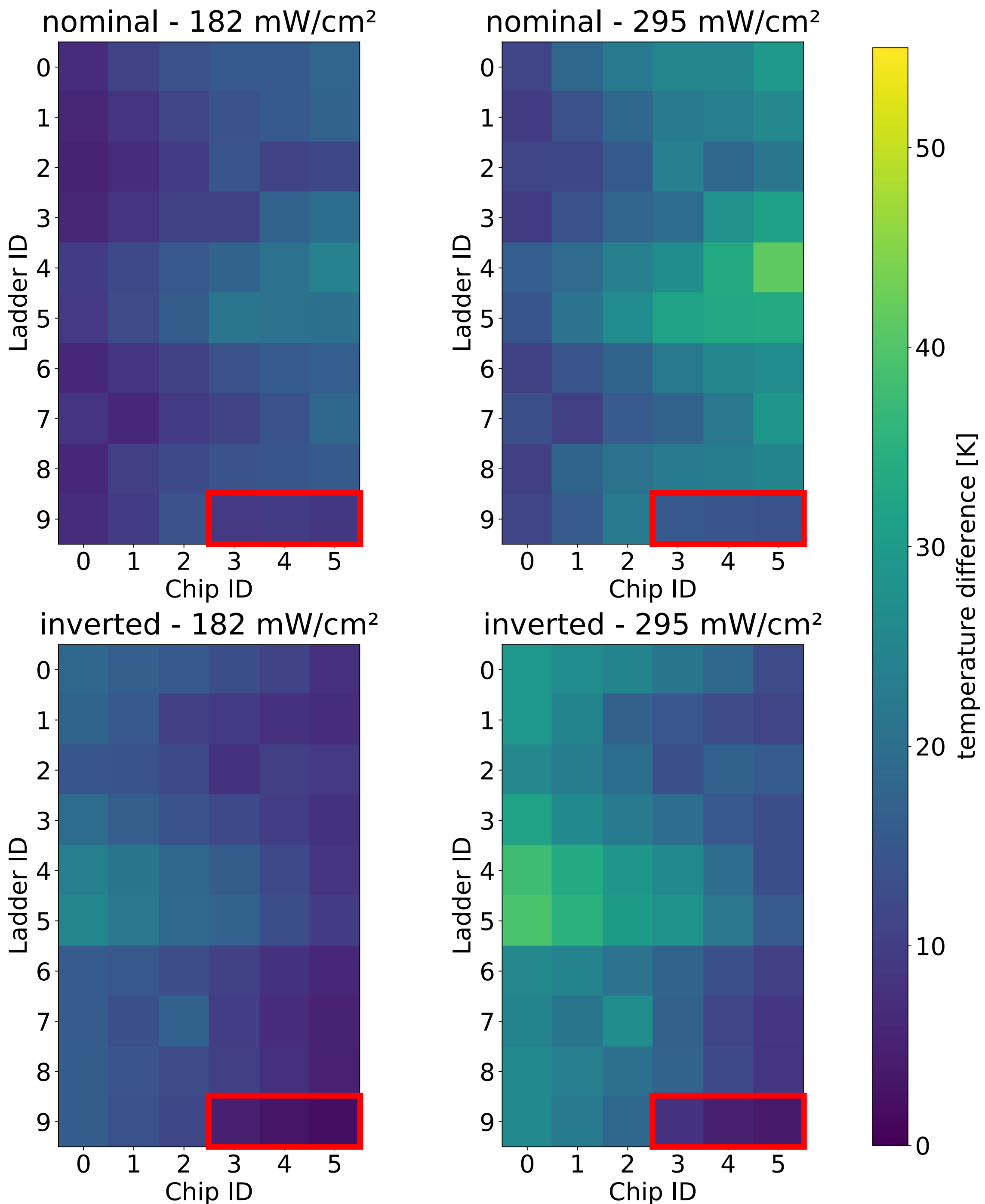


Figure B.4: Corrected temperature maps and interpolated results for chip without working readout of L1 of the silicon heater mock-up for nominal and inverted flow and heat loads of $182\,\mathrm{mW/cm^2}$ and $295\,\mathrm{mW/cm^2}$. Inactive chips are marked in red.

B.2 Polynomial fits to estimate the missing chip temperatures

The corresponding plots are shown on the next page.

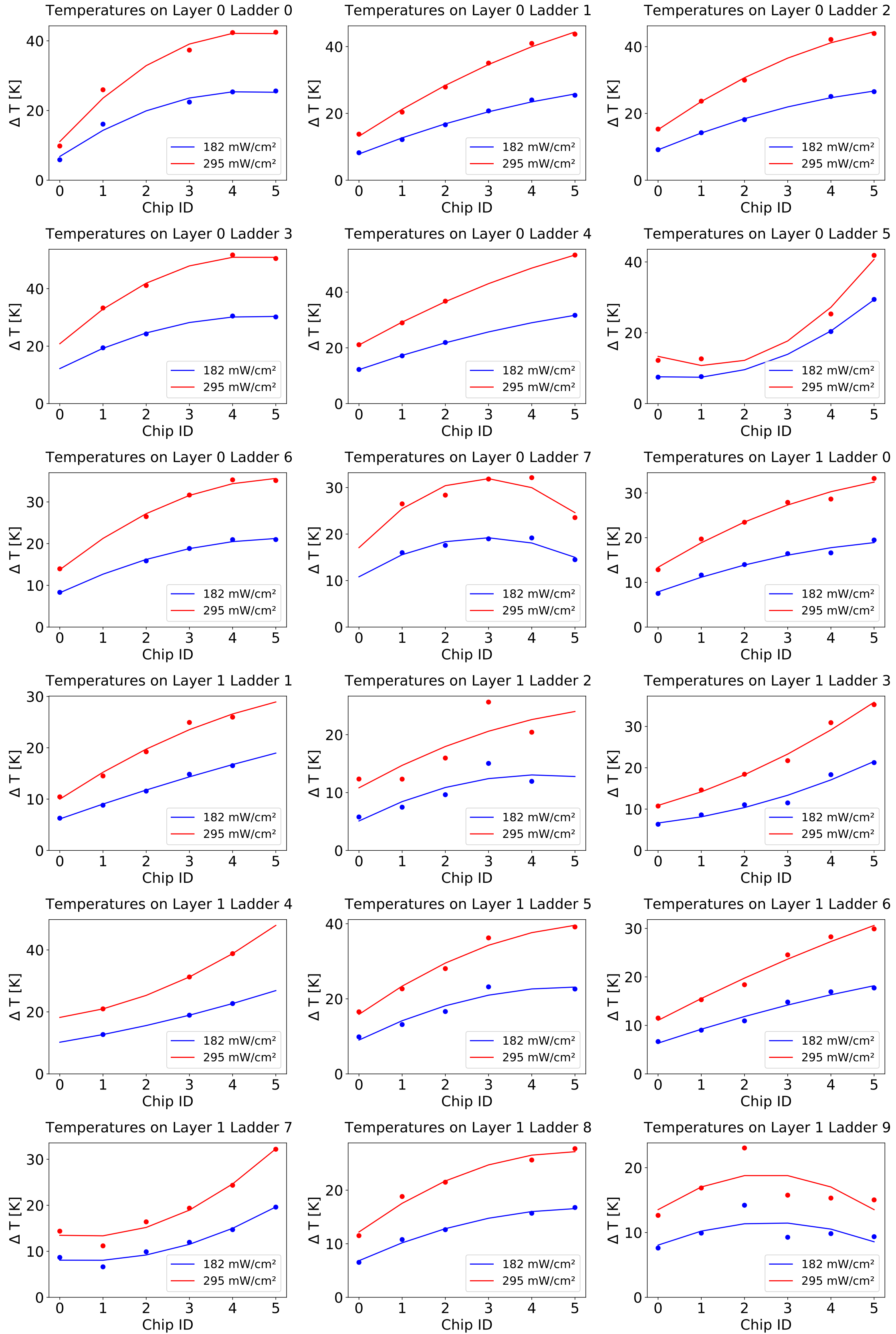


Figure B.5: 2-dimensional polynomial fit (solid line) to estimate temperatures of heater chips with a non-functional thermometer. Data is shown exemplarily for the nominal flow configuration.

B.3 Raw data of the power scan

The corresponding plots are shown on the following pages.

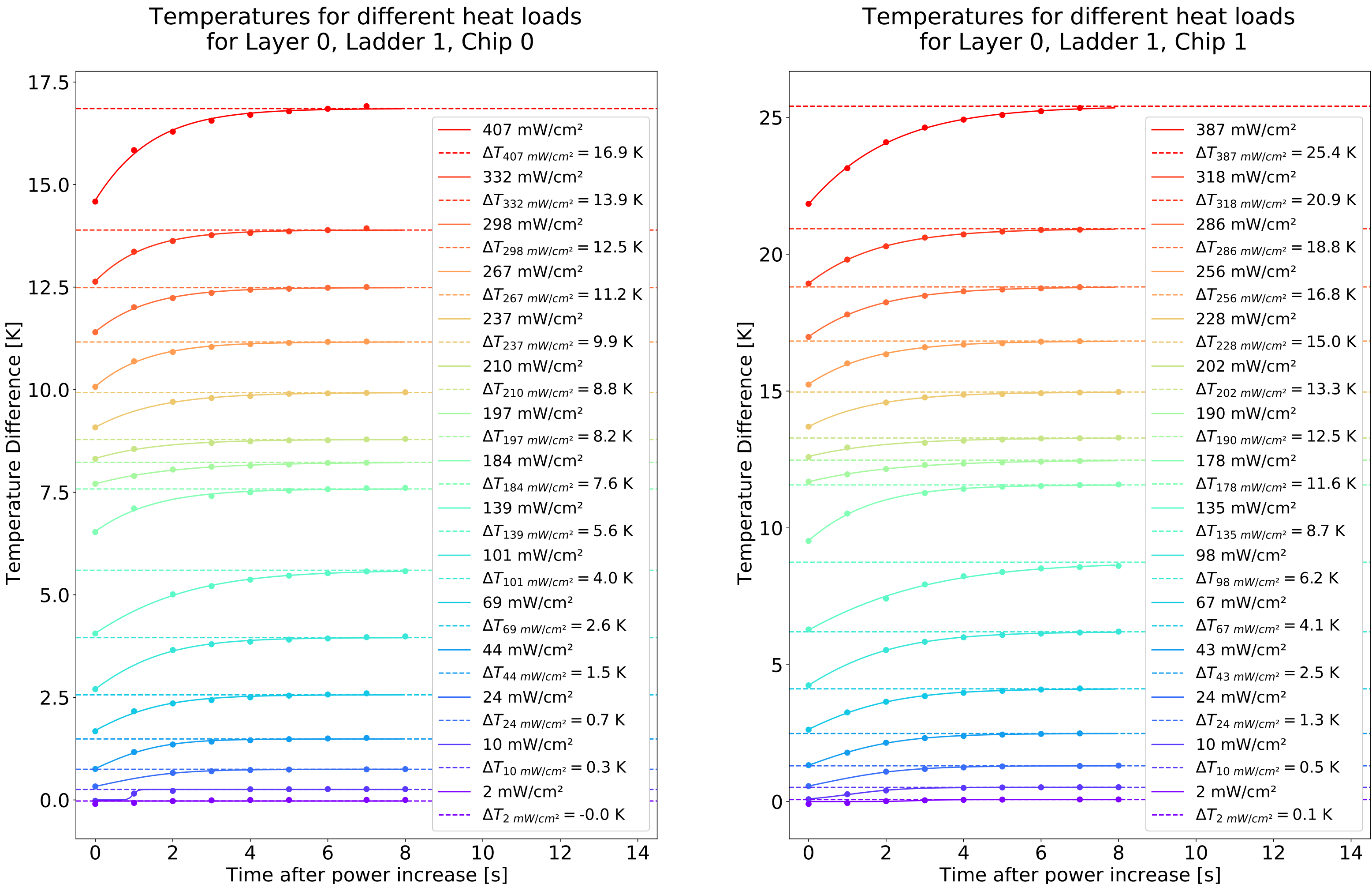


Figure B.6: Temperature differences to zero power for Chip 0 & 1 of L0 Ladder 1.
Current provided by power supply was scanned in steps of 0.2 A, 0.4 A, 0.6 A, 0.8 A, 1.0 A, 1.2 A, 1.4 A, 1.6 A, 1.65 A, 1.7 A, 1.8 A, 1.9 A, 2.0 A, 2.1 A, and 2.3 A. Heat dissipation corrected for effects described in section 6.4.1.

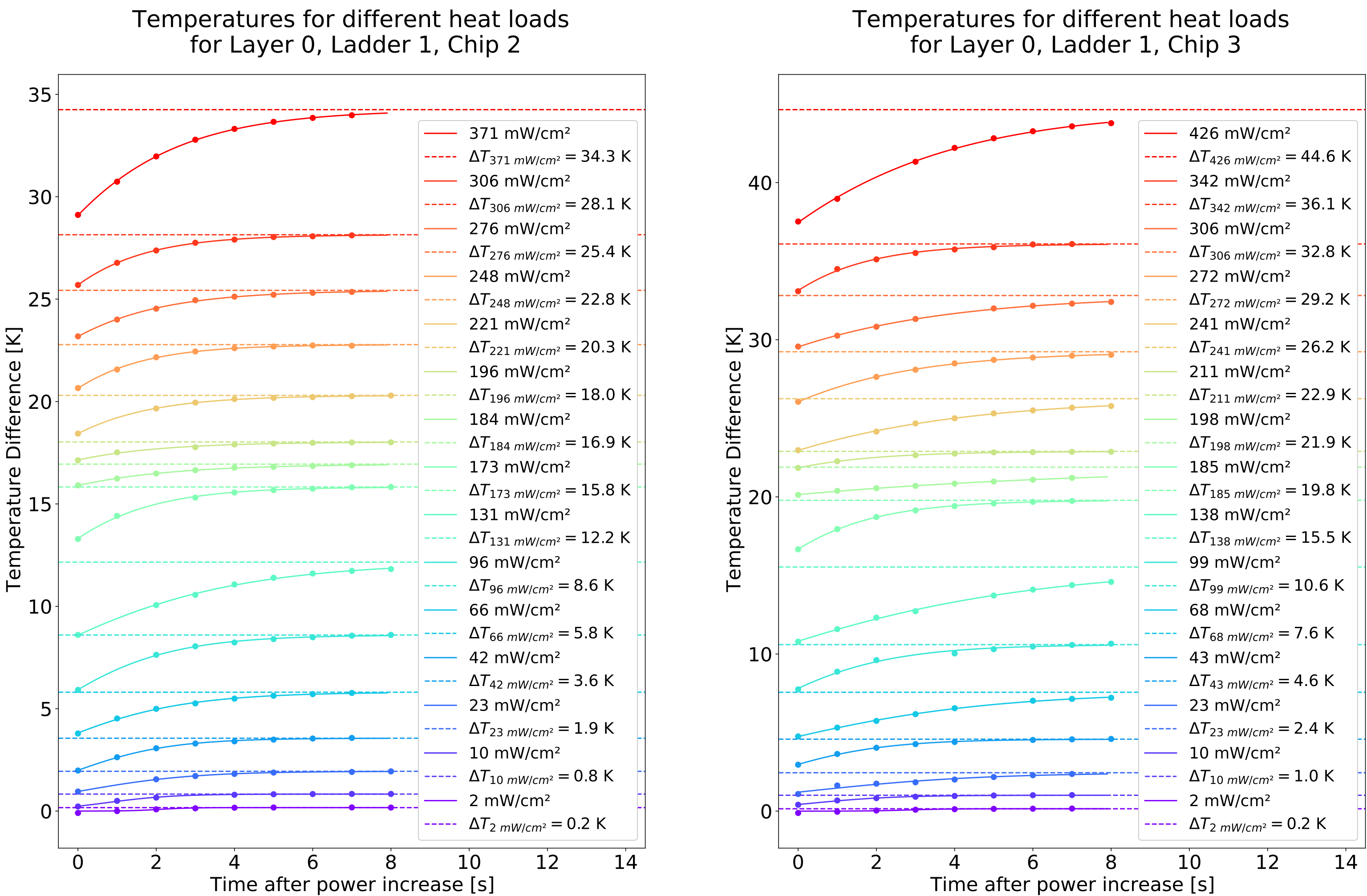


Figure B.7: Temperature differences to zero power for Chip 2 & 3 of L0 Ladder 1.
Current provided by power supply was scanned in steps of 0.2 A, 0.4 A, 0.6 A, 0.8 A, 1.0 A, 1.2 A, 1.4 A, 1.6 A, 1.65 A, 1.7 A, 1.8 A, 1.9 A, 2.0 A, 2.1 A, and 2.3 A. Heat dissipation corrected for effects described in section 6.4.1.

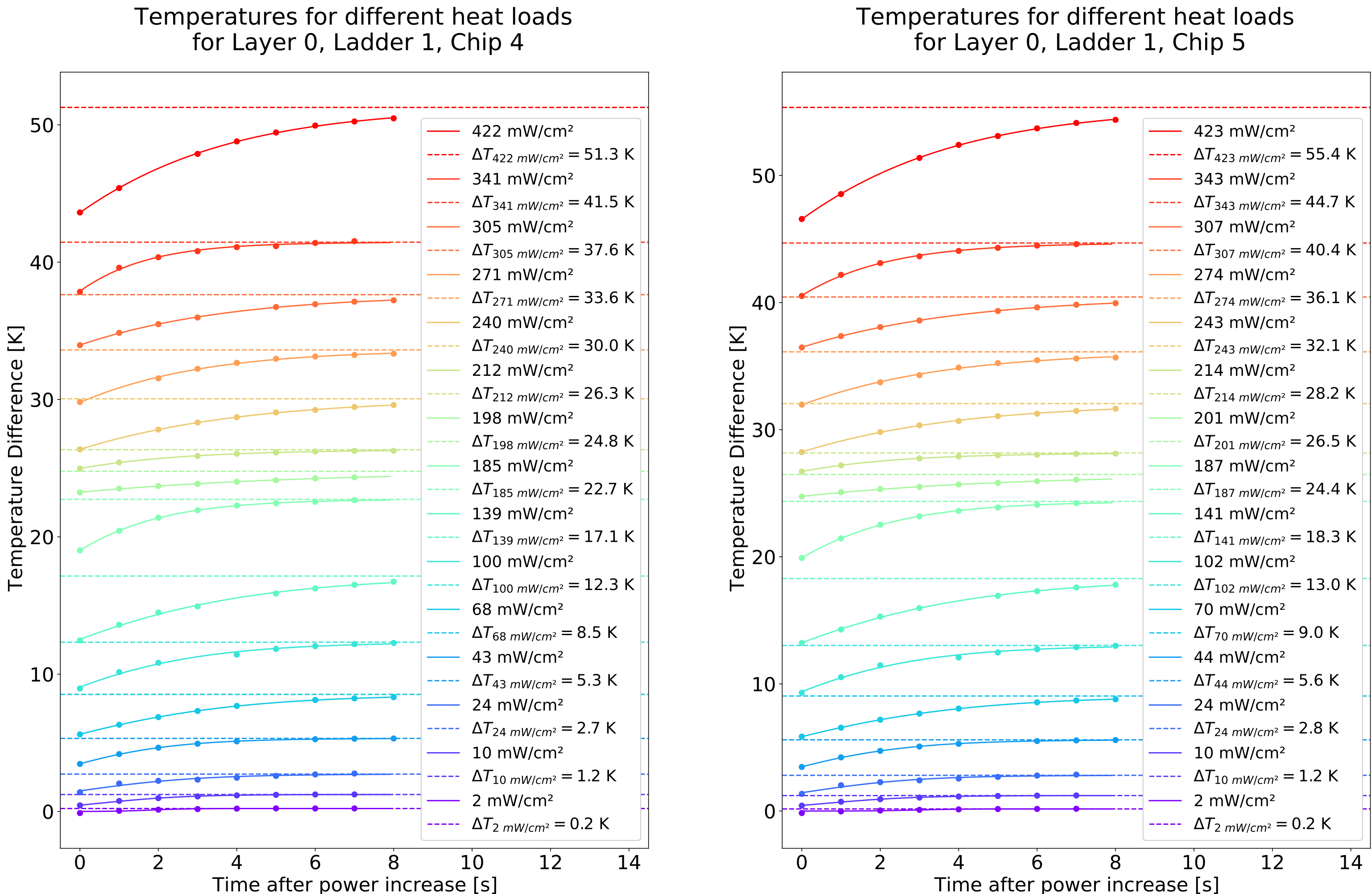


Figure B.8: Temperature differences to zero power for Chip 4 & 5 of L0 Ladder 1.
Current provided by power supply was scanned in steps of 0.2 A, 0.4 A, 0.6 A, 0.8 A, 1.0 A, 1.2 A, 1.4 A, 1.6 A, 1.65 A, 1.7 A, 1.8 A, 1.9 A, 2.0 A, 2.1 A, and 2.3 A. Heat dissipation corrected for effects described in section 6.4.1.

B.4 Temperature maps raw data

Table B.1: Uncorrected silicon heater temperature difference to the inlet temperature, given in kelvin, for L0 with nominal flow and 182 mW/cm^2 heat load.

Chip	0	1	2	3	4	5
Ladder 0	5.9	16.1	NaN	22.4	25.3	25.6
Ladder 1	8.2	12.2	16.6	20.8	24.0	25.4
Ladder 2	9.1	14.2	18.1	NaN	25.1	26.5
Ladder 3	NaN	19.4	24.2	NaN	30.5	30.2
Ladder 4	12.2	17.1	21.9	NaN	NaN	31.7
Ladder 5	7.5	7.6	NaN	NaN	20.3	29.4
Ladder 6	8.3	NaN	15.9	18.8	21.0	21.0
Ladder 7	NaN	16.0	17.6	19.0	19.2	14.5

Table B.2: Uncorrected silicon heater temperature difference to the inlet temperature, given in kelvin, for L0 with nominal flow and 295 mW/cm^2 heat load.

Chip	0	1	2	3	4	5
Ladder 0	9.8	26.0	NaN	37.3	42.4	42.5
Ladder 1	13.8	20.4	27.9	35.1	41.0	43.7
Ladder 2	15.3	23.7	30.0	NaN	42.2	44.0
Ladder 3	NaN	33.3	41.1	NaN	51.7	50.5
Ladder 4	21.1	29.0	36.7	NaN	NaN	53.3
Ladder 5	12.2	12.6	NaN	NaN	25.3	41.8
Ladder 6	14.0	NaN	26.5	31.7	35.3	35.1
Ladder 7	NaN	26.5	28.4	31.8	32.1	23.5

Table B.3: Uncorrected silicon heater temperature difference to the inlet temperature, given in kelvin, for L0 with inverted flow and 182 mW/cm^2 heat load.

Chip	0	1	2	3	4	5
Ladder 0	20.8	24.7	NaN	19.7	17.4	11.9
Ladder 1	25.9	25.2	21.6	17.5	13.0	7.1
Ladder 2	27.5	27.1	23.0	NaN	14.3	8.4
Ladder 3	NaN	32.6	29.2	25.4	21.7	14.0
Ladder 4	31.1	27.0	25.8	NaN	NaN	12.5
Ladder 5	21.2	15.4	NaN	NaN	9.2	12.4
Ladder 6	22.2	NaN	19.2	16.0	12.6	7.2
Ladder 7	NaN	21.6	19.0	16.7	15.3	7.3

Table B.4: Uncorrected silicon heater temperature difference to the inlet temperature, given in kelvin, for L0 with inverted flow and 295 mW/cm^2 heat load.

Chip	0	1	2	3	4	5
Ladder 0	31.8	40.3	NaN	32.7	29.0	20.2
Ladder 1	44.0	42.4	37.9	29.6	21.7	11.7
Ladder 2	46.3	44.0	37.7	NaN	23.8	14.3
Ladder 3	NaN	54.8	48.9	41.6	35.7	23.4
Ladder 4	51.5	49.9	42.8	NaN	NaN	21.0
Ladder 5	35.2	26.5	NaN	NaN	15.3	21.2
Ladder 6	37.8	NaN	32.5	27.0	21.3	12.4
Ladder 7	NaN	36.3	31.9	27.5	25.5	12.2

Table B.5: Uncorrected silicon heater temperature difference to the inlet temperature, given in kelvin, for L1 with nominal flow and 182 mW/cm^2 heat load.

Chip	0	1	2	3	4	5
Ladder 0	7.5	11.6	14.0	16.4	16.6	19.5
Ladder 1	6.3	8.8	11.6	14.8	16.5	NaN
Ladder 2	5.8	7.5	9.6	15.0	11.9	NaN
Ladder 3	6.3	8.6	11.1	11.5	18.3	21.2
Ladder 4	NaN	12.7	NaN	18.9	22.7	NaN
Ladder 5	9.9	13.1	16.6	23.2	NaN	22.6
Ladder 6	6.7	9.0	10.9	14.8	16.9	17.7
Ladder 7	8.7	6.6	9.9	12.0	14.7	19.6
Ladder 8	6.5	10.8	12.6	NaN	15.7	16.8
Ladder 9	7.6	9.9	14.2	9.3	9.8	9.4

Table B.6: Uncorrected silicon heater temperature difference to the inlet temperature, given in kelvin, for L1 with nominal flow and 295 mW/cm^2 heat load.

Chip	0	1	2	3	4	5
Ladder 0	12.8	19.7	23.5	27.9	28.6	33.3
Ladder 1	10.4	14.5	19.2	24.9	26.0	NaN
Ladder 2	12.3	12.3	16.0	25.6	20.4	NaN
Ladder 3	10.7	14.6	18.4	21.7	30.9	35.3
Ladder 4	NaN	21.0	NaN	31.3	38.8	NaN
Ladder 5	16.5	22.7	28.1	36.2	NaN	39.2
Ladder 6	11.5	15.3	18.4	24.5	28.3	29.9
Ladder 7	14.4	11.2	16.4	19.4	24.3	32.2
Ladder 8	11.5	18.8	21.5	NaN	25.6	27.7
Ladder 9	12.6	16.9	23.0	15.8	15.3	15.0

Table B.7: Uncorrected silicon heater temperature difference to the inlet temperature, given in kelvin, for inverted flow and 182 mW/cm^2 heat load.

Chip	0	1	2	3	4	5
Ladder 0	19.9	17.8	16.4	13.5	11.8	8.3
Ladder 1	18.9	16.3	11.0	9.5	8.2	NaN
Ladder 2	15.8	15.0	12.7	8.3	10.7	NaN
Ladder 3	NaN	17.8	14.9	12.5	10.3	8.6
Ladder 4	NaN	23.2	NaN	16.6	12.9	NaN
Ladder 5	27.8	24.1	20.6	17.8	NaN	10.5
Ladder 6	17.2	16.1	13.6	10.7	8.3	6.5
Ladder 7	17.3	14.4	17.8	10.3	7.2	5.5
Ladder 8	17.4	15.3	13.2	NaN	7.6	5.2
Ladder 9	17.4	14.7	12.3	4.8	3.2	2.2

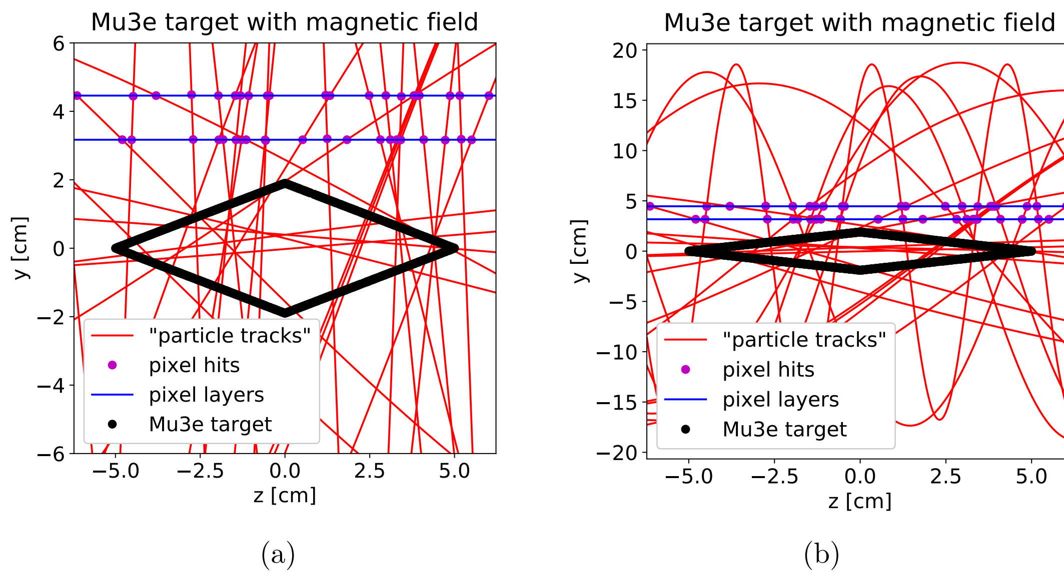
Table B.8: Uncorrected silicon heater temperature difference to the inlet temperature, given in kelvin, for L1 with inverted flow and 295 mW/cm^2 heat load.

Chip	0	1	2	3	4	5
Ladder 0	33.1	29.7	27.6	22.4	19.8	14.0
Ladder 1	32.4	27.2	18.6	15.5	13.4	NaN
Ladder 2	28.7	25.3	21.7	14.2	18.1	NaN
Ladder 3	NaN	29.6	25.1	20.5	16.1	14.4
Ladder 4	NaN	38.8	NaN	27.5	21.4	NaN
Ladder 5	46.1	40.7	34.7	29.9	NaN	17.8
Ladder 6	28.9	27.0	22.9	18.1	14.2	11.2
Ladder 7	28.0	23.9	29.2	17.1	12.2	9.3
Ladder 8	29.2	25.9	22.2	NaN	12.7	8.9
Ladder 9	28.9	25.0	20.3	7.9	5.0	3.9

Integration run analysis: additional plots

C

C.1 Recurling particles in the Mu3e target simulation



(a) (b)

Figure C.1: Event display of simulated muon decays for the Mu3e target with a magnetic field of 1 T applied: a) only central area as in Figure 8.6b, b) zoomed out to visualize recurling tracks.

C.2 Column-to-column correlations with main diagonals visualized

In Figure C.2, the same column-to-column correlation between L0 and L1 as in Figure 8.10b are displayed. To better recognize the crossing points of the two bands with the main diagonal, the main diagonals are visualized in red.

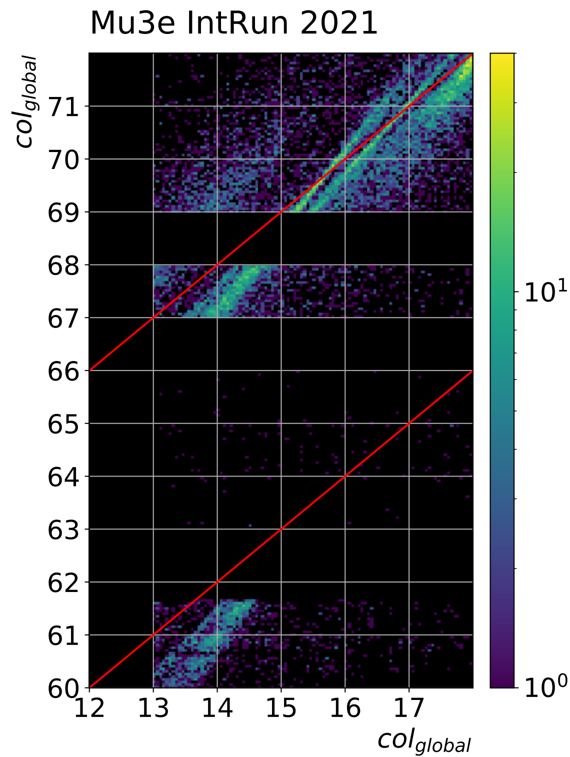
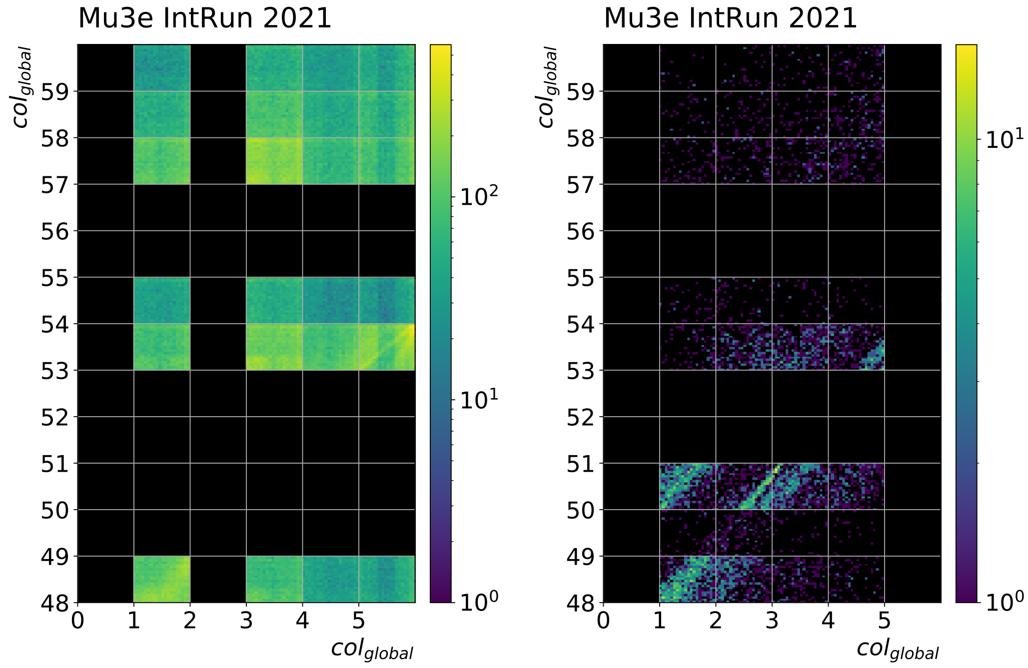


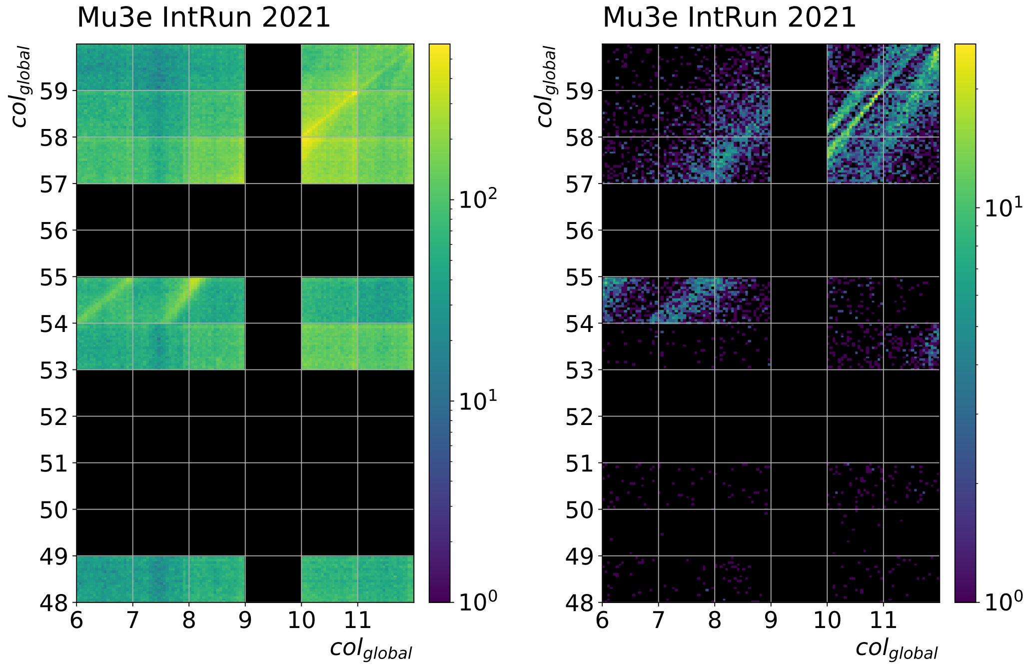
Figure C.2: Measured column-to-column correlations between Ladder 2 of L0 to Ladders 2-4 of L1 for the μSR target. Main diagonals are drawn in red.

C.3 Remaining column-to-column correlations



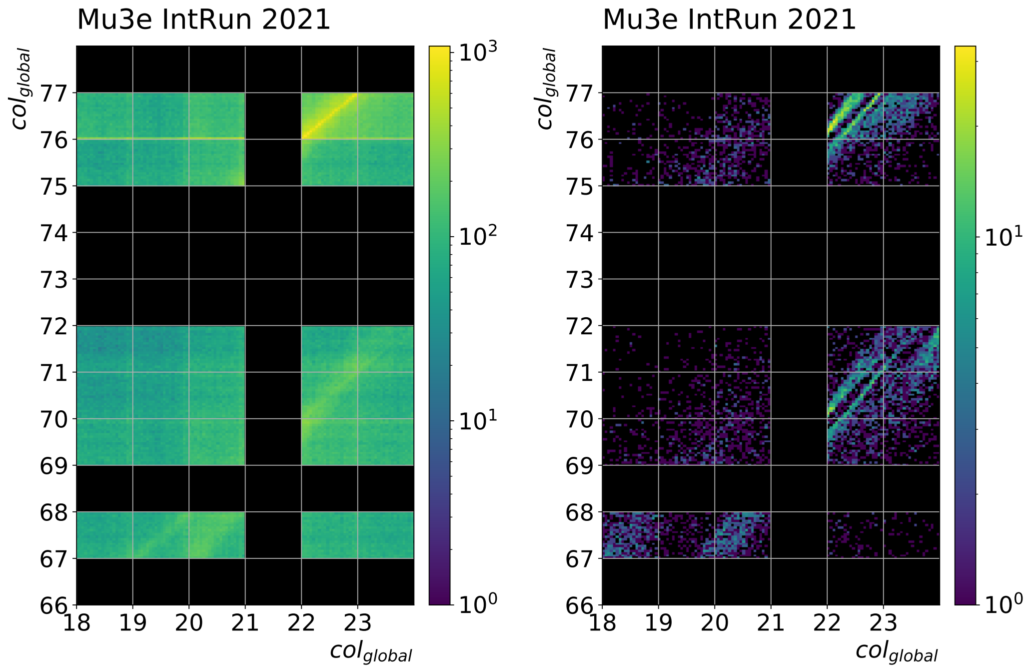
(a) Mu3e target with magnetic field. (b) μSR target without magnetic field.

Figure C.3: Measured column-to-column correlations between Ladder 0 of L0 to Ladders 0 & 1 of L1 for both targets.



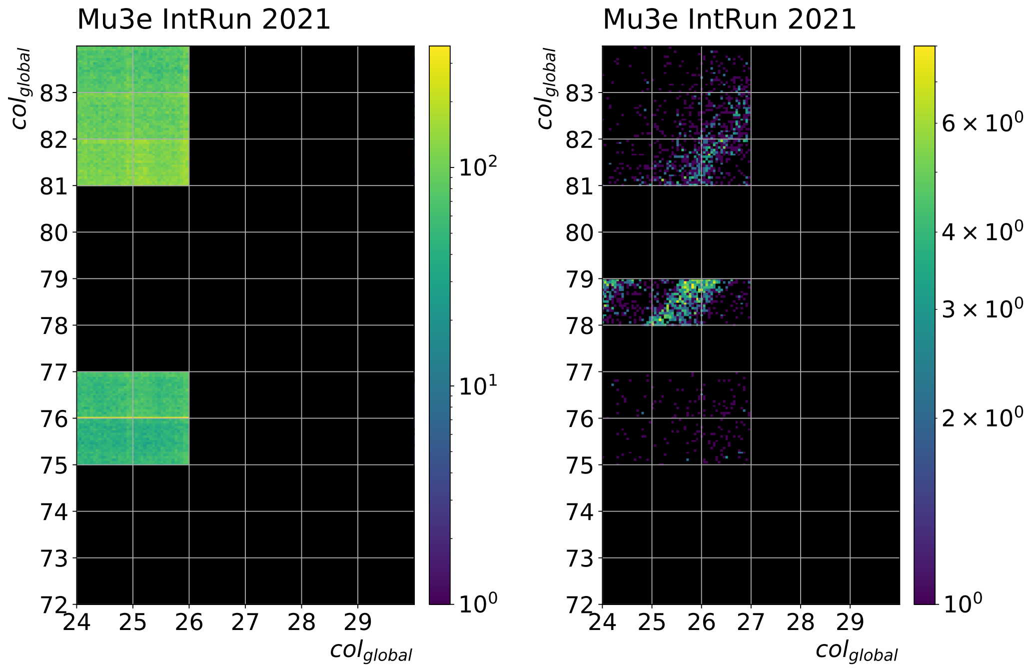
(a) Mu3e target with magnetic field. (b) μSR target without magnetic field.

Figure C.4: Measured column-to-column correlations between Ladder 1 of L0 to Ladders 0 & 1 of L1 for both targets.



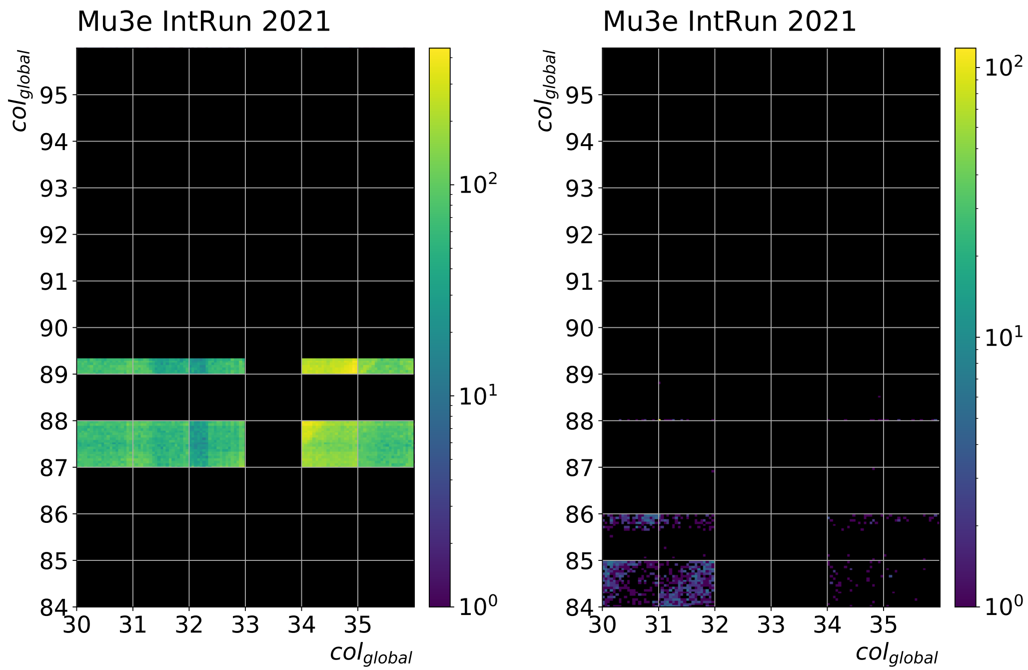
(a) Mu3e target with magnetic field. (b) μSR target without magnetic field.

Figure C.5: Measured column-to-column correlations between Ladder 3 of L0 to Ladders 3 & 4 of L1 for both targets.



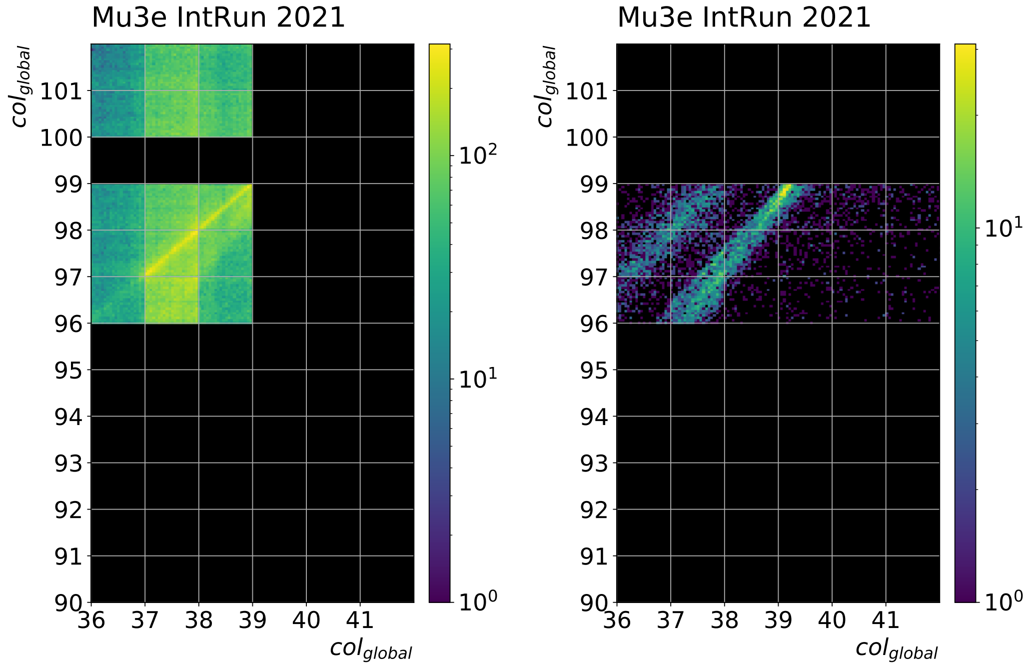
(a) Mu3e target with magnetic field. (b) μSR target without magnetic field.

Figure C.6: Measured column-to-column correlations between Ladder 4 of L0 to Ladders 4 & 5 of L1 for both targets.



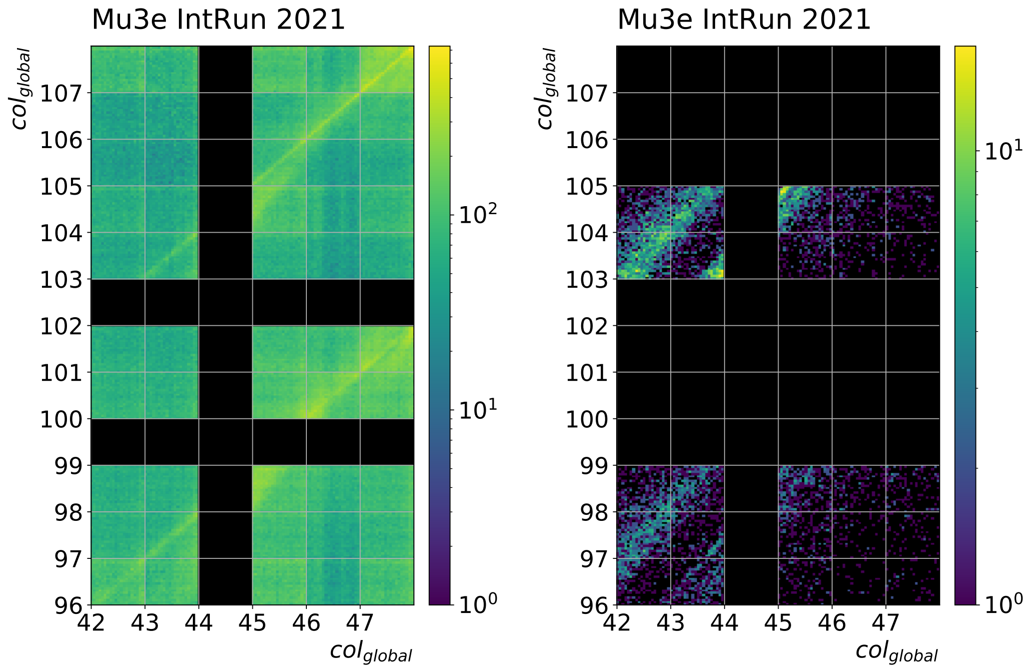
(a) Mu3e target with magnetic field. (b) μSR target without magnetic field.

Figure C.7: Measured column-to-column correlations between Ladder 5 of L0 to Ladders 6 & 7 of L1 for both targets.



(a) Mu3e target with magnetic field. (b) μSR target without magnetic field.

Figure C.8: Measured column-to-column correlations between Ladder 6 of L0 to Ladders 7 & 8 of L1 for both targets.



(a) Mu3e target with magnetic field. (b) μSR target without magnetic field.

Figure C.9: Measured column-to-column correlations between Ladder 7 of L0 to Ladders 8 & 9 of L1 for both targets.

Publications D

Parts of the presented concepts, ideas, and work have appeared previously or will be published in the following journal articles and conference proceedings:

The Mu3e experiment: Toward the construction of an HV-MAPS vertex detector
T. Rudzki et al.
Proceedings of the International Workshop on Future Linear Colliders 2021
arXiv: 2106.03534[physics.ins-det]

Proof of concept for cooling a pixelated tracking detector with gaseous helium
F. Meier Aeschbacher et al.
to be published

Technical design of the phase I Mu3e experiment
K. Arndt et al.
In: *Nucl. Instrum. Meth. A* 1014 (2021), 165679. DOI: 10.1016/j.nima.2021.165679.

MuPix and ATLASPix – Architectures and Results
A. Schöning et al. (2020)
arXiv: 2002.07253[physics.ins-det]

Performance of the large scale HV-CMOS pixel sensor MuPix8
H. Augustin et al.
In: *JINST* 14 (2019), C10011. DOI: 10.1088/1748-0221/14/10/c10011.

The following publications are related to the work prior to the doctoral studies:

The upgrade of the ALICE TPC with GEMs and continuous readout
ALICE TPC collaboration et al.
In: *JINST* 16 (2021), P03022. DOI: 10.1088/1748-0221/16/03/p03022/.

Particle identification studies with a full-size 4-GEM prototype for the ALICE TPC upgrade
M.M. Aggarwal et al.
In: *Nucl. Instrum. Meth. A* 903 (2018), p. 215-223. DOI: 10.1016/j.nima.2018.06.084.

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