Clock Transmission for the Data Acquisition System of the Mu3e Experiment

by

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Bachelor Thesis in Physics
submitted to the Faculty of Physics
Institute of Nuclear Physics, Johannes Gutenberg-Universität
Mainz
February 4^{th} 2019

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Abstract

The Mu3e experiment is set out to search for the lepton flavour violating muon decay $\mu^+ \to e^+e^-e^+$ using high voltage-monolithic active pixel-sensors. A target sensitivity is to measure one in 10^{16} decays at a stopped muon rate of 1×10^8 Hz. In order to achieve such ambitious sensitivity goals, good momentum, time and vertex resolution is needed. This is especially important as combinatorical background and internal conversion processes ($\mu \to eee\nu\nu$) cannot be avoided. Consequently, the main motivation for the construction of a low jitter clock distribution network for the triggerless Mu3e data acquisition system are the timing detectors where the clock must not contribute more than 10 ps jitter RMS to the timing signal. A global clock signal is distributed to all components of the readout system optically. Track reconstruction and selection will then be done by computers in the filter farm.
For this thesis, the Clock Transmission Board was developed. It will be applied as an optical to electric signal manipulator and jitter attenuator for the filter farm PCs. Corresponding to the signal quality requirements set by the readout system the Si5344 jitter attenuator and clock multiplier was chosen as the heart of the Clock Transmission Board. After the design of the schematic the PCB layout was created. In the second part of this thesis the Clock Transmission Board's signal characteristics were quantified. The output jitter was measured as (310.61 ± 1.14) fs and rise time as (99.91 ± 0.01) ps for differential signals. Thus, the Clock Transmission Board achieved values comparable to the ones reached by the Si5344 Evaluation Board taken as reference. Further measurements included phase stability, eye diagram and spectrum analysis. It was concluded that the Clock Transmission Board fulfills the requirements set for the Mu3e readout system to meet the sensitivity goal for the experiment.

Zusammenfassung

Das Mu3e Experiment zielt auf die Messung des leptonenzahlverletzenden Zerfalls $\mu^+ \to e^+e^-e^+$ mit einer Genauigkeit von einem in 10^{16} Zerfällen bei einer Myonenrate von 1×10^8 Hz ab. Dazu kommen pixelbasierte Hochspannungssensoren zum Einsatz. Sehr gute Impuls-, Zeit- und Vertexauflösung sind nötig, um die für das Experiment notwendige Sensitivität zu erreichen. Insbesondere können Zerfälle durch innere Konversion ($\mu \to eee\nu\nu$) und kombinatorischer Hintergrund nicht abgeschirmt werden. Für das triggerlose Mu3e DAQ wird ein Um die Unterscheidung der Daten zu ermöglichen werden Detektoren mit einer hohen Zeitauflösung verwendet. Dazu benötigt die triggerlose Mu3e Datenerfassung ein globales Taktsignal mit einem Jitter von weniger als 10 ps im Mittel. Dieses wird verlustarm mit optischen Fasern übertragen. Die letztendliche Datenauswertung wird von den filter fam PCs ausgeführt.
Im Zuge dieser Arbeit wurde das Clock Transmission Board entwickelt. Es wird als Signalfilter für die filter farm PCs eingesetzt werden. Der Si5344 Jitter Abschwächer und Taktsignal Erzeuger wurde auf Grund seiner Signaleigenschaften, welche den Anforderungen des Mu3e Datenauslese Systems entsprechen, als Hauptbaustein ausgewählt. Sowohl das Erstellen Schaltplan als auch die Platzierung der Bauelemente auf der Leiterplatine wurde vorgenommen. Im Zweiten Teil dieser Arbeit werden die Signaleigenschaften des Clock Transmission Boards ermittelt. So wurde am Signalausgang ein Jitter von (310.61 ± 1.14) fs und eine Flanken Anstiegszeit von (99.91 ± 0.01) ps für differenzielle Signale gemessen. Damit erreicht das Clock Transmission Board nicht nur zum Si5344 Evaluation Board vergleichbare Werte, sondern genüg auch den Anforderungen des Mu3e Datenauslese Systems. Weiterhin wurden Messungen zur Phasenstabilität, zu Augendiagrammen und zur Frequenzanalyse durchgeführt.

Chapter 1

Introduction

Humans are fundamentally driven by the desire to explore. As such, understanding the world created for us lies at the core of human nature. On the most fundamental level, the current status of human understanding of nature is represented by the Standard Model of Particle Physics. This Standard Model has proven itsself over decades with experimental results backing the theory. However, 95% of all matter is neither explored nor explained. Thus, the need for physics beyond the Standard Model arises. With theories like neutrino oscillation extensions of the Standard Model can be formulated and need to be proven experimentally.
The Mu3e experiment is set out to search for the lepton flavour violating muon decay $\mu^+ \to e^+e^-e^+$ using high voltage-monolithic active pixel-sensors. The current limit on the upper limit of the branching ratio of $BR < 1 \cdot 10^{-12}$ was set by the SINDRUM II experiment in 1985. Mu3e aims at improving this limit with a measuring sensitivity of one on 10^{16} decays for a muon at rest rate of 1×10^8 Hz. Thus, the detection of such a decay would be a clear sign for physics beyond the Standard Model. At the heart of the Mu3e detector are the high voltage-monolothic active pixel-sensors which provide excellent momentum and vertex resolution. Furthermore, scintillating tiles and fibres are added to improve time resolution.
Central to the concept of a high-sensitivity experiment with a high data rate due to the triggerless architecture of the detector is a low jitter data acquisition system. For Mu3e experiment, the clock signal which synchronises the components of the readout system is generated centrally and then distributed using multimode optical fibres. The final stage of the readout system is represented by the filter farm, where vertex reconstruction is done

by PCs equipped with field programmable gate arrays and graphical processing units. The clock signal needs to be converted back to electrical signals and jitter cleaned for these computers. This role will be fulfilled by the Clock Transmission Board.
In this thesis the design process and testing of the Clock Transmission Board will be outlined. Therefore, the conception of the schematic and the design of the printed circuit board layout will be shown. Furthermore, measurements characterising the signal quality performance will be analysed and hence the compatibility of the Clock Transmission Board to the Mu3e readout systems requirements shown.

Chapter 2

The Standard Model of Particle Physics and Beyond

As of today, most experimental discoveries in high energy physics can be described by the Standard Model of Particle Physics (SM). Combining the electroweak theory with quantum chromodynamics, three of the known four fundamental interactions can be described using the methods of quantum field theory. Gravitation is the only interaction not included. In the SM, matter consists of fermions with spin $\frac{1}{2}$, fundamental interactions are carried out via the exchange of vector bosons of spin one. Additionally the SM predicts a spin zero particle which couples proportionally to mass, the Higgs boson. The discovery of the Higgs particle [1] emphasises the success of the SM, as for nearly fifty years no experiment could produce experimental results pointing at different theories. As shown in fig. 2.1, the constituents of the SM can be categorised by charge, mass and spin. Consequently fermions and their anti-particles can be split into three generations depending on their flavour and into six quarks and six leptons depending on their charge. While the first generation can be found in every atom, the other generations have very short lifetimes. Bosons couple to charge (color, weak or electric) or mass. Of those only the photon cannot interact with itself since it does not carry the charge its representative force couples to. For each fundamental interaction all affected fundamental particles are shown inside a respective box (fig. 2.1). While the electromagnetic force possesses unlimited range due to its massless vector boson, the effective range for the strong force is limited by self-interaction of the gluon, which is also massless. Since the vector bosons of the weak force are very heavy, the range for this interaction is

of the order 1×10^{-18} m [2]. For all fundamental interactions, conservation laws can be formulated. Energy, momentum, angular momentum, electrical charge, color charge, baryon number and lepton number are conserved, however the charged current of the weak interaction violates P-symmetry through coupling exclusively to left handed fermions and right handed anti-fermions. Whether or not a particle interacts via a certain force is determined by whether the particle carries a charge the force couples to. Furthermore, the graviton is only proposed theoretically as gravitation was not yet combined with the SM successfully.

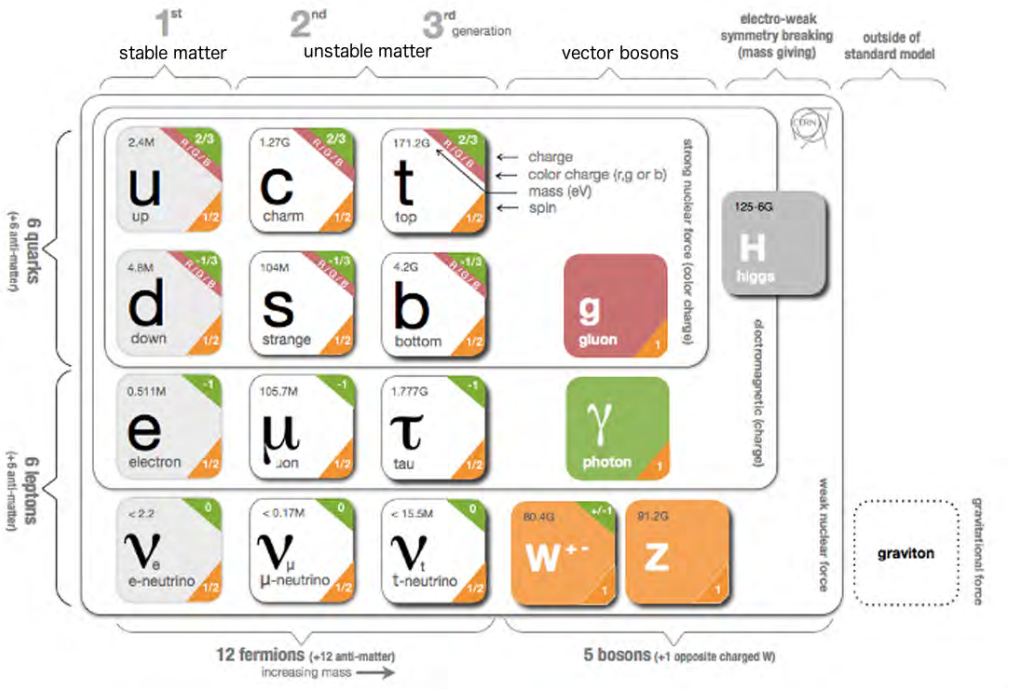


Figure 2.1: The fundamental particles and interactions described by the Standard Model of Particle Physics. Adapted from [3].

Signs for physics beyond the SM can be found. Famously the Cosmic Microwave Background recorded by the Planck space observatory [4] leads to the conclusion that the energy matter density of the universe consists of 5% baryonic matter (SM particles), 26% dark matter and 69% dark energy; 95% cannot be explained by the SM. The need for dark matter can also be justified by the rotational speeds of galaxies. Furthermore, neutrinos in

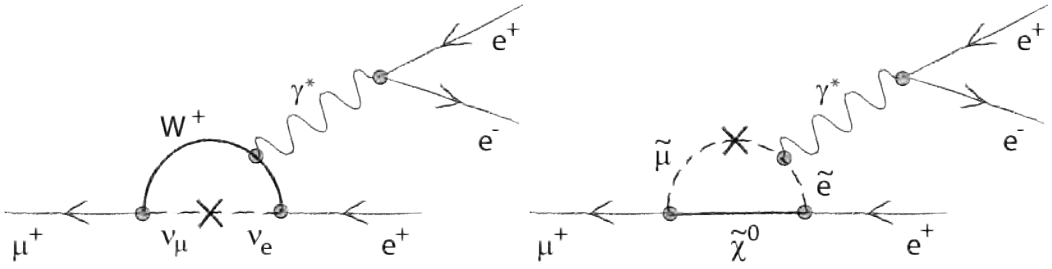
the SM are assumed to be massless. However, neutrino oscillation and the resulting lepton flavour mixing can be described analogously to quark flavour mixing. The superposition of neutrino flavours was observed in the Sudbury Neutrino Obervatory (SNO) and the Super-Kamiokande experiment and thus the ability of neutrinos to change between flavours was proven [5], [6]. Hence neutrinos do have a mass. Through experiments like KATRIN [7] upper bounds on the neutrino mass will be set. Through a massive neutrino this effect can possibly be incorporated into the SM. Theories beyond the SM are needed to provide explanations for dark matter and dark energy.

2.1 Muon Decay and Lepton Flavour Violation

In the SM three generations of leptons exist. For each, the electron, the muon and the tau, a charged particle and an uncharged particle called a neutrino make up one generation. The same is true for antiparticles in which case all charges change their sign. Furthermore, each lepton is assigned a lepton number which is either $+1$ for particles or -1 for antiparticles. For all interactions in the SM, the sum of lepton numbers in the initial and the final state have to be equal. With the measurement of neutrino oscillation, lepton flavour violation LFV was detected for the first time, which gave support to theories suggesting the addition of massive neutrinos to the SM [8]. No charged lepton flavour violation was observed yet.

The anti-muon is a lepton of charge e, mass $105.658\,\mathrm{MeV}/{c_0}^2$ and lifetime $2.197\,\mu$s [2]. Furthermore, it decays almost exclusively via the Michel decay $\mu^+ \rightarrow e^+\nu_e\bar{\nu}_\mu$ with a branching ratio (BR) of nearly one. However, other decays like $\mu \rightarrow e\nu\bar{\nu}\gamma$ or $\mu \rightarrow eee\nu\bar{\nu}$ are possible, yet strongly suppressed. While it is clear that lepton flavour violating decays exist, the production of sufficiently high rates for the detection of such decays proves challenging in the SM. One way to describe such decays is via neutrino mixing as in fig. 2.2a. Neutrino mixing however strongly depends on neutrino masses and lepton mixing angles. As such the theoretical BR are very small in the SM [9]:

$$BR(\mu \rightarrow e\gamma, \mu \rightarrow e, \mu \rightarrow eee) \propto \left| \sum_{i=2,3} U^*_{\mu i} U_{ei} \frac{\Delta m^2_{il}}{M^2_W} \right| < 10^{-54} \quad , \qquad (2.1)$$



(a) Decay via neutrino oscillation. (b) Decay via SUSY.

Figure 2.2: Lepton flavour violating muon decay channels.

where $U^*_{\mu i}, U_{ei}$ are elements of the neutrino mixing matrix, Δm^2_{il} is the squared mass difference of two neutrinos ($m_\nu \leq 0.26\,\mathrm{eV}/{c_0}^2$ [10]) and $M_W = 80\,\mathrm{GeV}/{c_0}^2$ is the W-boson mass.
Theories extending the SM however can give such LFV decays much higher BR.

2.2 Current Limits

Previous experiments provided upper bounds on the existence of lepton flavour violating muon decays as shown in fig. 2.3. Charged lepton flavour violating decays (cLFV) are very strongly suppressed in the SM, however well within reach for theories extending the SM. Forthcoming experiments like Mu3e can directly provide proof for the extension of the SM.

- SINDRUM II
  SINDRUM II was an experiment conducted in 1985 at the Paul Scherrer Institute (PSI). Using a muon beam where each muon possessing a momentum of 28 MeV/c was stopped, 5 multiwire proportional drift chambers were used for the detection of the decay products. The whole setup was inside a magnetic field of 0.334 T and the detector was triggered using a hodoscope. An upper limit on the branching ratio (BR) of $\mu \to eee$ was set as $BR < 1 \cdot 10^{-12}$ with a confidence level (CL) of 90% [12].

- MEG
  Also at PSI, the MEG experiment set an upper bound on the BR of

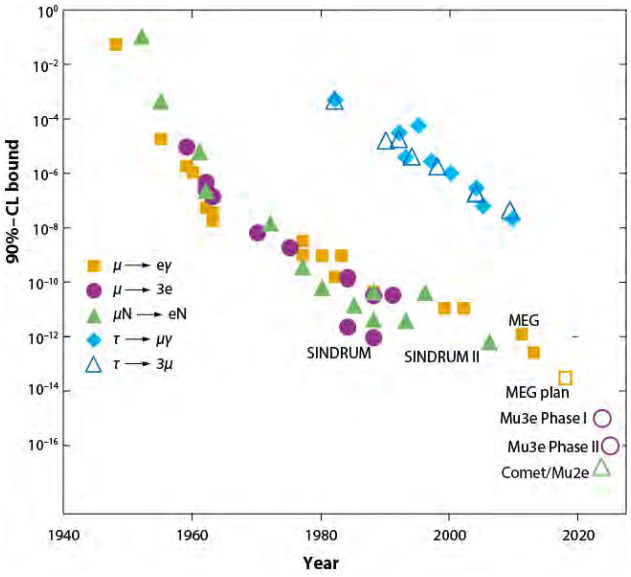


Figure 2.3: Upper bounds on the branching ratio of charged lepton flavour violating decays at 90% CL as measured by several experiments during the last decades. Adapted from [11].

$\mu^+ \to e^+\gamma$. Using drift chambers (e^+ detection) and a liquid Xenon calorimeter (photon detection), the positron momentum, the photon energy and both the angle and time of the decay products were detected. An upper limit of $BR < 5.7 \cdot 10^{-13}$ at 90% CL was set [13].

Chapter 3

The Mu3e Experiment

The Mu3e experiment is set out to search for the lepton flavour violating muon decay $\mu^+ \to e^+e^-e^+$ with a sensitivity of one in 10^{16} decays. The discovery of a lepton flavour violating decay would directly challenge the SM. Both phases of the experiment will be located at the Paul Scherrer Institute in Switzerland (PSI). During the first phase of the experiment the sensitivity goal is $2 \cdot 10^{-15}$ for a stopped muon rate of 1×10^8 Hz [14]. For the final phase the muon rate will be upgraded to 2 GHz. In order to achieve such ambitious sensitivity goals, good momentum, time and vertex resolution is needed to suppress background. This is especially important as combinatorical background and internal conversion processes ($\mu \to eee\nu\nu$) cannot be avoided.

The whole setup will be surrounded by a superconducting magnet so he decay products are forced on a curved path for momentum measurement. To reduce scattering, the amount of material in the active part of the detector is minimised. The final setup will be triggerless, incorporating a push-architecture. To provide good time resolution and operate fast digital electronics, the pixel sensors, scintillating fibres, tiles and the readout system need to be supplied with a clean clock signal via optical links. Here a jitter of <10 ps is envisioned. In this chapter the detector together with the main components of the experimental setup will be discussed. As this thesis focusses on the clock distribution, the readout system clock will be discussed in detail in chapter 4.

3.1 Background Suppression

The vast majority of the muons undergo normal Michel decay. The data acquisition needs to remove these uncorrelated events. Since the Mu3e experiment will be triggerless, this will be done through constraints given mainly by vertex and momentum resolution. The incoming muon will be stopped by a double cone shaped Mylar target. So, decaying at rest, the total energy and momentum available for any decay will be as given in eqn. 3.1.

$$E_{tot} = \sum_{i=e^+,e^+,e^-} \sqrt{m_i^2 c^4 + \vec{p_i}^2 c^2} = m_\mu \cdot c^2 = 105.7 \frac{MeV}{c^2} \quad and \quad \vec{p}_{tot} = 0 \frac{MeV}{c}, \tag{3.1}$$

where m indicates rest mass, c is the speed of light and $\vec{p}$ denotes a momentum vector.

One of the main contributors to background will be the internal conversion decay $\mu^+ \to e^+e^-e^+\bar{\nu}_\mu\nu_e$. Here, however, a fraction of the muon rest energy is carried away by the generated neutrinos. Therefore, these decays can be separated from the data given a good enough energy resolution.

For a given rest mass available for the decay, the branching ratio of the searched for decays can be plotted against the neutrino energy as in fig. 3.1. In order to achieve the suppression of background noise below $1 \cdot 10^{16}$ decays at 2σ set for Mu3e, the needed energy resolution to distinguish the lepton flavour violating decay from other decays is given by $0.5\,\mathrm{MeV/c^2}$ [14].

A source of accidental background is mainly consisting of Michel decays of the form $\mu^+ \to e^+\bar{\nu}_\mu\nu_e$. The positron emerging from Michel decays together with electrons generated during Bhabha scattering with material inside the detector can have the same signature as the searched for decay. Such difficult cases can only resolved with good vertex reconstruction and timing, as for $\mu^+ \to e^+e^-e^+$ all decay products emerge from a single vertex in space and time.

The momentum resolution will be deteriorated by multiple Coulomb scattering in the detector material. The RMS Coulomb scattering angle θ_{rms} [16] can be calculated as in:

$$\theta_{rms} \propto \frac{\sqrt{\frac{x}{x_0}}}{p} \quad , \tag{3.2}$$

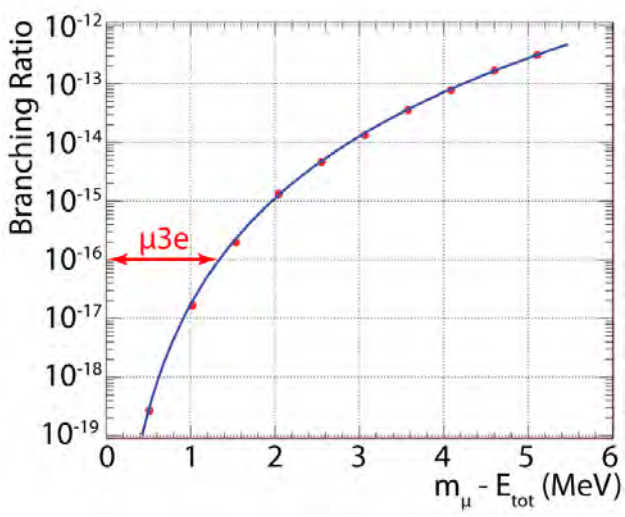


Figure 3.1: Branching ratio of the radiative decays with internal conversion as a function of the energy carried away by the neutrino. The energy resolution at the sensitivity goal of Mu3e is indicated in red. Aadapted from [15].

where x denotes the distance travelled by the particle in the given material, x_0 is the radiation length in the material and p is the absolute value of the momentum of the incoming particle.

The goal here is to make θ_{rms} as small as possible. This is necessary to retain the curvature of the decay products produced by the magnetic field to determine their momentum. At least three points are needed to determine their velocity and radius and thus their momentum. Few points are gathered by the decay products interacting with the three layers of pixel sensors in the central setup, where the material in the active part of the detector is minimised through minimising the effective radiation length $\frac{x}{x_0}$.

3.2 The Detector Setup

While the pixel sensors provide good position resolution, scintillating tiles and fibres improve the time resolution. Charged decay products are forced onto curved paths through a 1 T magnetic field, which is generated by a

superconducting magnet that surrounds the pixels, tiles and fibres. With the obtained curvature the particle momentum and charge can be determined. As shown in fig. 3.2, the target is surrounded by a cylinder consisting of two inner pixel layers, a layer of scintillating fibres and two outer pixel layers. All layers are mounted on Kapton structures and connected with aluminum interconnects on Kapton flex prints. Kapton cylinders containing more pixel sensors to detect recurled tracks along with scintillating tiles are added on both sides of the main cylinder. By using very thin components like high density interconnects and pixel sensors the effective radiation length per layer was reduced to $\frac{x}{x_0} = 0.1\%$ [17].

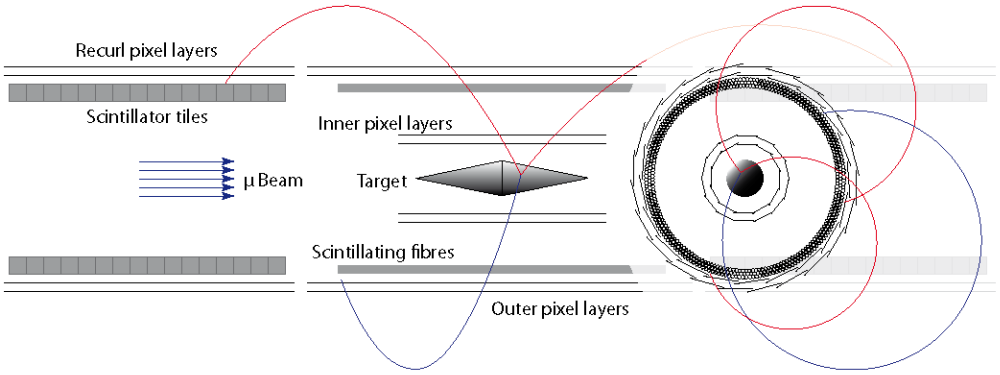


Figure 3.2: The detector setup shown from the side and in a cross-section.

3.3 MuPiX

Incorporated in the pixel tracking sensors is the high voltage-monolithic active pixel-sensor (HV-MAPS) technology. Here, a reverse bias high voltage is applied to a diode, thereby increasing the size and electric field strength of it's depletion zone. Shown in fig. 3.3 is the basic principle of the sensor utilising HV-MAPS. N-doped semiconductor sections are embedded in p-doped substrate, between which an electric field is generated through the application of a voltage. Incident charged particles of at least 3.7 eV can

generate electron-hole pairs which then get charge separated through the depletion zone. The sensor is manufactured in the complementary metal-oxide-semiconductor CMOS technology [18]. In the current iteration, MuPix8 chips can achieve a time resolution of 15 ns and a spacial resolution of 23.1 μm at an efficiency of 99.8%. Through the application of a HV of 85 V the depletion zone was increased to 30 μm for a substrate resistivity of 80 Ω cm [19]. Other benefits arise from the HV-MAPS technology. Since the sensor can be thinned to 50 μm and all electrical components needed for the readout can be incorporated on the chip, the effective radiation length was reduced to $\frac{x}{x_0} = 0.054$ % [20]. In the final design the complete chip will be $20 \cdot 23$ mm in size, while the active detector part will have a size of $20 \cdot 20$ mm yielding $250 \cdot 250$ pixels. A serial interface will transfer the taken data at a rate of 1.25 Gbit/s.

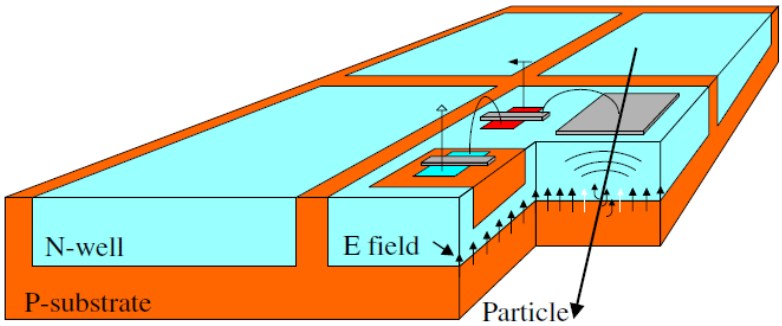


Figure 3.3: Schematic drawing showing the design of the HV-MAPS pixel design.

The signal of each pixel is processed as shown in fig. 3.4. Individual pn-transitions can be described as diodes. Here, a charge sensitive amplifier (CSA) amplifies the integrated pulse. After a source follower and another amplifier the pulse is digitised with a comparator. There, also a timestamp for each rising edge is generated using a 125 MHz clock. This clock is generated using a voltage controlled oscillator (VCO) which in turn is synchronised to a 125 MHz reference signal using a phase locked loop (PLL). This reference is generated centrally for the experiment and supplied to all parts of the readout chain.

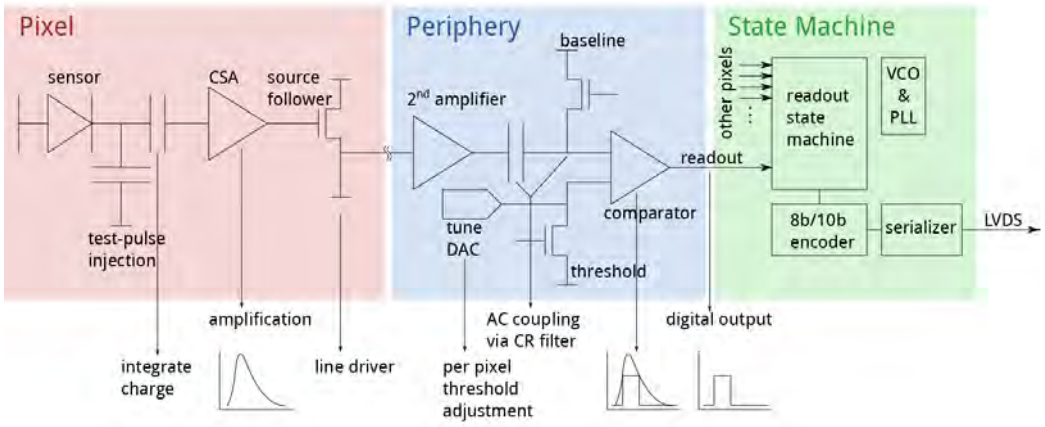


Figure 3.4: Schematic of electronic readout components on the MuPiX chip.

3.4 Timing Detector

In order to achieve sufficient time resolution, scintillating detectors are used additionally to the MuPiX chips. While the scintillating tiles possess a time resolution of 70 ps, the scintillating fibres achieve a resolution of 0.5 ns. As the material volume of the fibres is lower than that of the tiles, fibres are used in the central detector cylinder where scattering has to be minimised and tiles are applied in the recurl station cylinders adjacent to the central detector. All scintillators are connected to silicon photo multipliers (SiPM). These are not affected by the magnetic field in the detector volume and detect photons with an efficiency of 45 % [17]. For the time detection readout an application-specific-integrated-circuit named MuTRIG was developed. In essence, here the signal is analysed and the energy and the time of the detection are converted into a digital format using a time-to-digital converter (TDC) operated with a reference frequency of 625 MHz. This digital signal is equipped with a timestamp generated in synchronisation to the externally generated reference clock of 125 MHz using a PLL and a VCO. Together, scintillators and pixel detectors can achieve the momentum, vertex and time resolution needed for the Mu3e experiment.

3.5 Data Acquisition

Mu3e searches mainly for the $\mu^+ \to e^+e^-e^+$ decay. Therefore, potentially all tracks measured at one point in time can be correlated coming from a single vertex in space and time. The detector is triggerless and taken data is streamed continuously at a rate of up to 80 Gbit/s in Phase I and up to 1 Tbit/s in Phase II [17]. Specifically, data is sent from the detector elements, namely the pixels, tiles and fibres through Kapton flex prints to the Front-End FPGAs (field programmable gate array). All components of the Front-End system are inside the experiment solenoidal magnet as can be seen in fig. 3.5. 6 Gbit/s optical links connect the Front-End FPGAs to the switching boards and from there to the filter farm GPU (graphical processing unit) PCs. A fast track reconstruction is done online and the relevant vertices are stored and analysed offline.

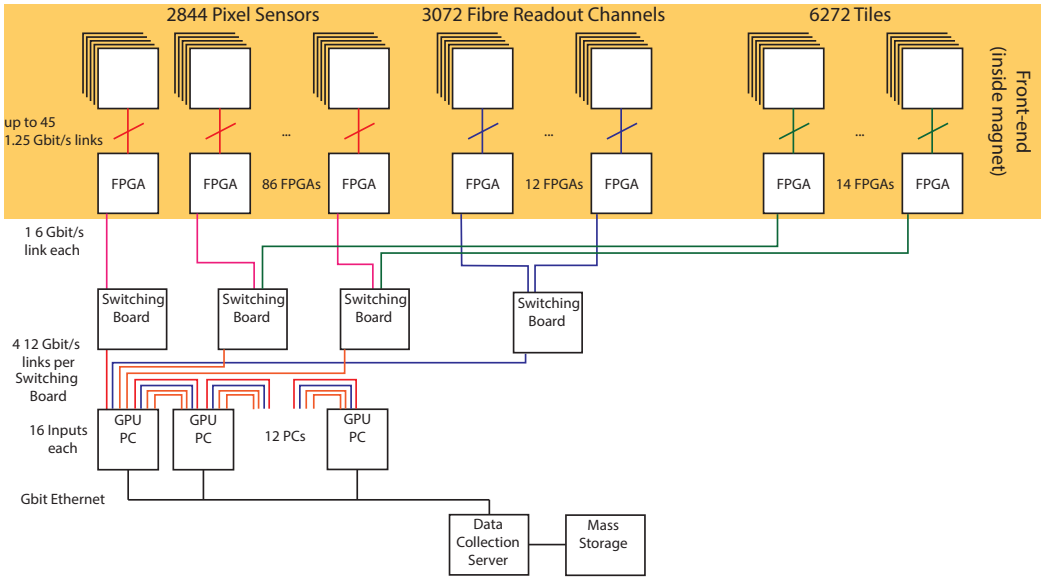


Figure 3.5: Schematic of the readout system.

- Front-End FPGA Pixel sensors provide zero suppressed hit information to the Front-End FPGA via 3 LVDS (low voltage differential signal) links each for the inner layers (1 connection for the outer layers). The pixels not only provide measured hit data but are also in continuous contact with the Front-End board to control the pixels status.

Each FPGA collects data from 15 pixel sensors for the inner layers and 36 pixel sensors for the outer layers [17]. Similarly, MuTRIG ASICs are connected to the Front-End board. Finally, the FPGA buffers the data after ordering it by time stamps and sends it via optical links to the switching FPGA. For the optical links three different kinds of optical transceivers are used. On the front-end board FireFly transceivers capable of a data rate of up to 15 Gbps connected to OM3-multimode-fibres [21] are implemented. For the switching boards MiniPod transceivers [22] capable of up to 12 Gbps fo each of twelve available channels connected to 850 nm multimode fibres are used. And for the filter farm QSFP transceivers [23] are used which comply withe the quad-small-formfactor-pluggable norm. The transciever uses a 850 nm emitter diode to drive 50/125 nm multimode optical fibres at 5 to 12 Gbit/s.

- Switching Boards The switching board FPGAs primarily serve as data collectors and routers. All tracks need to be reconstructed and checked for correlation, which is why all data from both recurl stations and the central detector is combined and routed as reconstruction timeframes to the filter farm via the switching boards.

- Filter Farm In the filter farm 12 FPGA and GPU equipped PCs process the data arriving via the optical links. First, a coordinate transformation from the sensor to the global laboratory system is done. Then, track reconstruction and subsequent track selection is done online. Tracks corresponding to the given requirements for the $\mu^+ \to e^+e^-e^+$ decay are stored and further processed offline.

Chapter 4

Clock Distribution

The main motivation for the construction of a low jitter clock distribution network for the triggerless Mu3e DAQ are the timing detectors which possess a timing resolution of $\ll$100 ps. More precisely the clock must not contribute more than 10 ps jitter RMS to the timing signal. Furthermore, a globally synchronised reset signal is provided. The reset signal is transferred in a 1.25 Gbit/s link and synchronised to the right 125 MHz clock cycle corresponding to a 8 ns period. The clock signal has a frequency of 125 MHz with a desired jitter of <10 ps [17]. First, the clock signal is generated by the clock generation board, a Xilinx Kintex-7 Field Programmable Gate Array (FPGA) development board Genesys 2 by Digilent.

There, a Si5345 low jitter, any output, any frequency, jitter cleaner together with a voltage controlled oscillator (VCO) with jitter <90 fs [17] is used to generate the clock signal and synchronise the reset signal to, as illustrated in fig. 4.1. In order to synchronise the reset signal, two clock outputs of the Si5345 are connected to the FPGA, while the remaining eight are routed towards Firefly transceivers. Similarly eight reset signal lines are linked to one Firefly. The clock generation board is controlled via I^2C on a FPGA Mezzanine Connector (FMC) board. The I^2C interface is used for communication between the FMC board and the FPGA and also to collect data from the Firefly transceivers like temperature and power monitoring. Also, the reset signal command is provided externally via ethernet and the reset signal is generated by the FPGA.

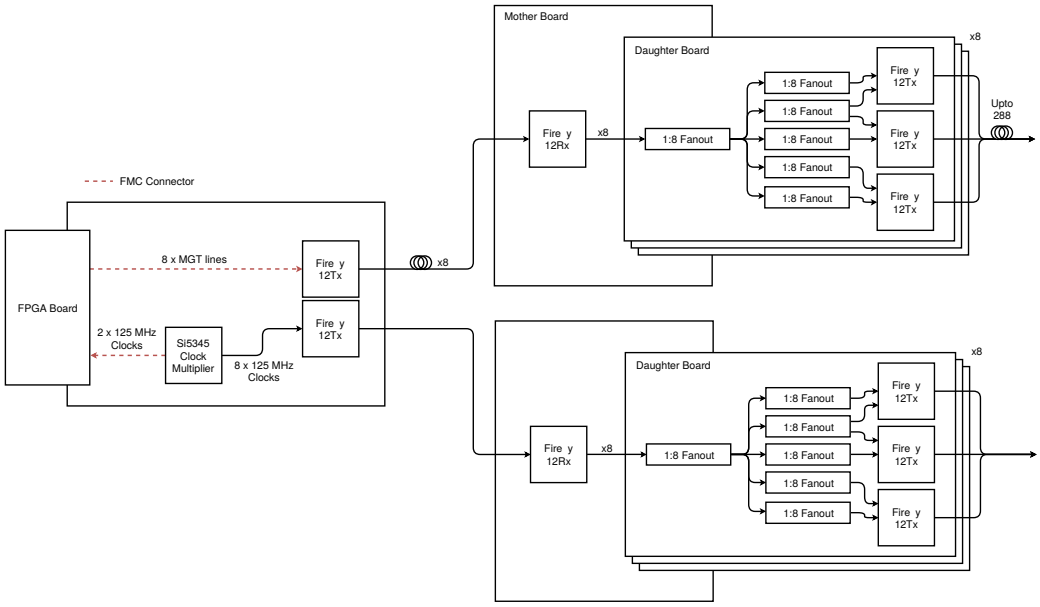


Figure 4.1: Schematic illustrating the clock generation setup. Here, a FPGA is connected to the FMC board creating eight copies of the clock and reset signal each. From there, multiple mother and daughter boards are connected for further splitting the signals [17].

I^2C is a master-slave data bus protocol. It consists of a two-wire bidirectional serial interface. Hence, two power links, a data (serial data SDA) and a timing (clock select SCL) link are necessary. Up to 118 integrated circuits (IC) can be connected serially and are contacted via a 10 bit address. Additionally, for each data set of 8 bits sent, a start, a read or write (RW), a acknowledgement (ACK) and a stop bit are sent. Most notably, I^2C differs from other data busses concerning timing. While the master provides an upper bound on the data link clock, the slave can answer using a slower clock providing that intermittent bits are kept low [24].

Next the clock signals are fed through optical links to Firefly connectors on so called mother boards. Per mother board up to eight daughter boards can be connected by a mezzanine connector. A rendering is shown in fig. 4.2. In total 288 copies of the original clock signal are made [17] through multiple splitters. Used on the daughter boards is an On-Semi NB7L1008M fanout chip providing a $1:8$ 6.5 Gbit/s differential splitter with a clock jitter of less than 0.5 ps. Of the generated 40 clock copies only 36 can be used, as the

number of inputs on the Firefly transceivers is limited.

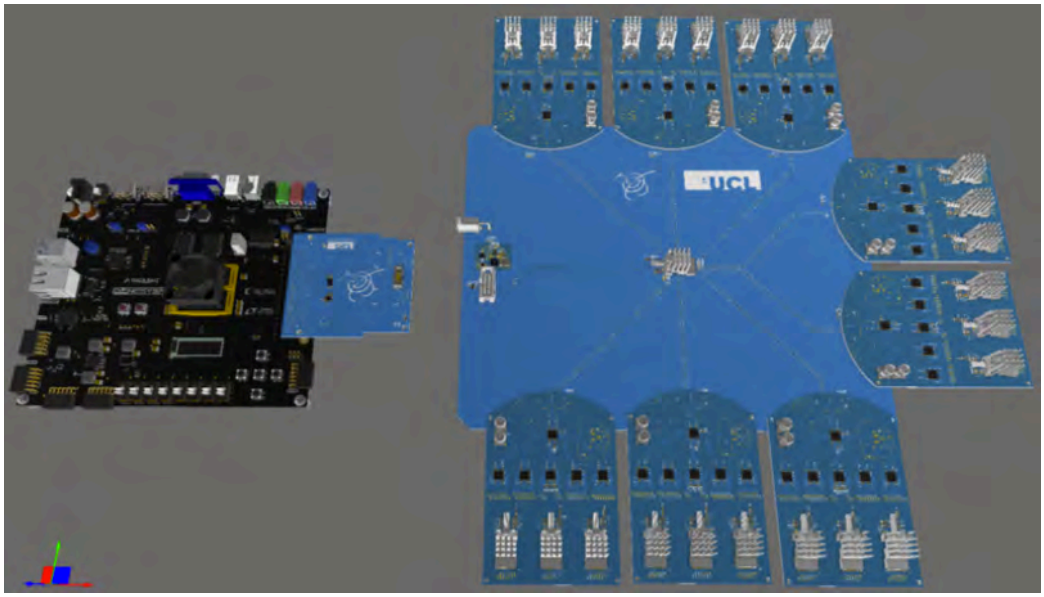


Figure 4.2: CAD drawing showing the clock generation setup. In black, the Genesys 2 board is connected to a FMC board via a Mezzanine connector. On the Genesys 2 board the Xilinx Kintex-7 FPGA is visible underneath the cooling fan. The signals are transmitted through an optical fibre from the Firefly transceiver of the FMC board to the motherboard. On the right hand side the motherboard with a Firefly optical transceiver at it's center is shown, connected to eight daughter boards, each of them creating 36 signal copies. These copies are then distributed via three Firefly transceivers per daughter board [17].

Henceforth, individual optical links for the clock and reset signal are routed toward the frond-end boards inside the detector magnet's bore, the switching boards and the farm PCs as shown in fig. 4.3. The front-end board receives the clock and reset input via a Firefly transceiver. The signal jitter is attenuated before being distributed individually to the timing boards and their detector elements, specifically being the MuPiX pixel detector chip and the MuTRIG timing detector ASIC. On the front-end board the signal is being sent as a Low Voltage Differential Signal (LVDS). Each switching board has a dedicated jitter cleaner.

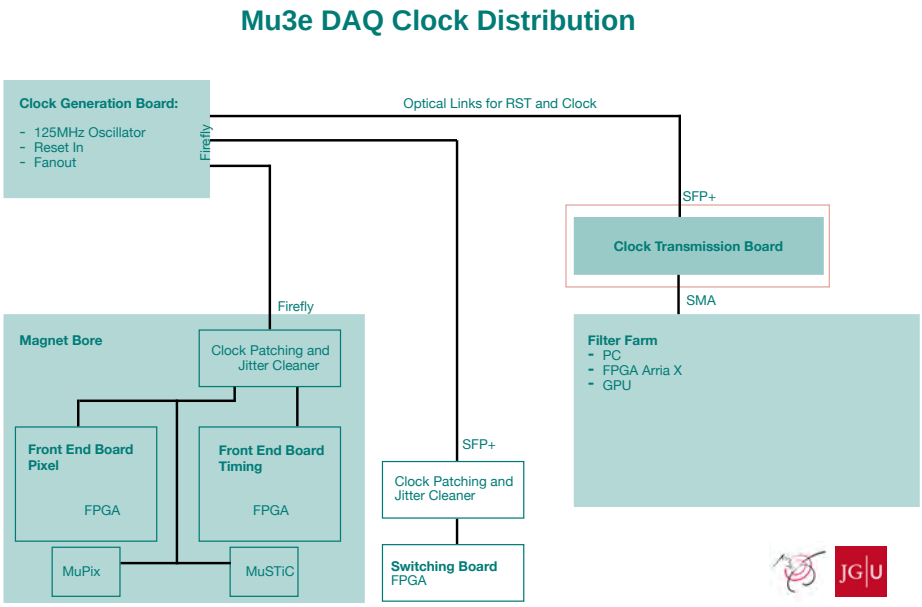


Figure 4.3: Schematic of the Mu3e clock distribution setup. The clock is generated on the upper left clock generation board and then optically transmitted to the front-end board, the switching boards and the filter farm PCs. In this thesis, the Clock Transmission Board needed to receive the clock signal for the filter farm PC was developed.

The project behind this thesis is to develop and characterise the Clock Transmission Board (CTB) framed in red in fig. 4.3. Clock and reset signals arrive via optical fibres from the clock generation setup. The optical fibre connector corresponds to the Small Formfactor Pluggable (SFP+) norm. Consequently, a SFP+ transceiver is implemented on the CTB. As the CTB is still a prototype, more inputs for testing of different scenarios are included. As such the CTB possesses three more electrical SubMiniature version A (SMA) inputs. Furthermore, the signal is cleaned and manipulated by a Si5344 any-frequency, any-output, jitter-attenuating clock multiplier. From there, the signal is routed to the filter farm PC's FPGA via a differential or single ended SMA connector. The CTB is designed to carry four outputs.

Chapter 5

Signal Theory

As humanity becomes more and more dependent on high speed data interconnects, faster signal transmission links have to be constructed. For the Mu3e experiment as well as for mobile communication networks the transmission of fast electrical and optical clock signals is essential. Hence, signal theory stands at the center of enabling fast data transmission.

A signal is the time-dependent variation of the value of a physical observable. Important for this thesis is the transmission of a voltage amplitude, in which case the signal is given by the variation of a voltage with time. Furthermore, signals can be continuous (analog) or discrete (digital). Digital signals ideally are given by square waveforms. Due to interference with external factors, this exact square waveform is never reached in reality but rather distorted such that the edges of the waveform are not vertical but tilted. Through the analysis of how the actual signal deviates from it's ideal form, the signal quality can be quantified. This is especially important for digital signals, as the exact amplitude value at one point in time decides over the state of the signal. Factors contributing to this distortion and quantities characterising the signal quality will be discussed in this chapter.

5.1 Voltage Signals

A voltage signal is transmitted as a time-dependent voltage-level over an electrical conductor. For this the respective resistance, capacitance and inductance of the transmitting and receiving end of the connection and the

connection itsself have to be taken into account. Commonly two methods of electrical signal transmission are used: Single ended signal transmission and differential signal transmission.

5.1.1 Single Ended Signal

For a single ended transmission link two electrical conductors are used. As one is held at a common ground level between the transmitter and the receiver, the other one carries the signal amplitude as a voltage level. While this method is cost-effective because multiple connections can share the same ground connection and n links correspond to $n+1$ connections, single ended transmission links are prone to noise coupling from ground differences between circuits and electromagnetic interference. The most commonly used single ended transmission standard is the low voltage complementary metal oxide semiconductor (LVCMOS) standard [25].

5.1.2 Differential Signal

Differential signal transmission uses two complementary conductors. At each point in time, the voltage amplitude being sent through the conductors is equal with different sign around an offset. Consequently, the actual signal is given by the difference between the voltage levels on both conductors. Since the two conductors have to possess exactly the same transmission time, the same length in most cases, for the differential signals to arrive at the same time, for every link two connections are needed. This leads to increased cost compared to single ended connections. However, differential signal links have considerable advantages over other forms of signal transmission. As both complementary parts of the electrical signal are affected equally by noise coupling and electromagnetic interference, the signal difference and as such the received signal stays the same. Hence, differential signals are well suited to fast low voltage signal transmission. Commonly used standards include the low voltage differential signal (LVDS) standard [26] and the low voltage positive-emitter coupled logic (LVPECL) standard [27]. Used for Mu3e is the LVDS standard. Here the driver supplies a maximum current of 3.5 mA and due to the 100 Ω termination on the receiver side a voltage difference of 350 mV is applied on each link, respectively. Hence, the current flow direction determines whether the receiver sees negative of positive current, interpreting it as a logic 0 or 1.

5.2 Optical Signal

The need for faster transmission of signals with less power loss than that associated with electrically conducted signals led to the development of optical links. Further advantages beside very fast transmission times and near loss-free transmission include a small form factor and immunity to electromagnetic interference. The transmitter side is represented by a light emitting diode (LASER diode by todays standards) and the receiver side by a diode light sensor. In most applications optical links are bidirectional, thus transmitter and receiver are combined. The actual transmission of the signal is conducted discretely (digitally) through optical fibres. Used for the Mu3e experiment is the small form factor pluggable (SFP+) standard for transceivers [28] together with OM3 multimode optical fibre cables.

5.3 Signal Characteristics

5.3.1 Jitter

Timing jitter is defined as the time deviation of a PLL[1]-generated controlled edge from its nominal position [29] as indicated in fig. 5.1. If the timing jitter of a signal is referenced to a clock signal it is also called jitter. As such, jitter can be measured as the standard deviation of the period length of a periodic signal. The period jitter quantifies the deviation in cycle length of a signal with respect to the theoretical period as [29]:

$$t_{jit}(period) = t_{cyclen} - \frac{1}{f_0} \quad , \tag{5.1}$$

where f_0 is the nominal signal frequency and t_{cyclen} is the period time of the n^{th} measured cycle of the signal.

Cycle-to-cycle jitter then adds the restriction that only adjacent periods may be compared. The time interval error (TIE) is specified as the deviation of individual cycle edges from their theoretical position, as represented in fig. 5.1. When TIE > 0.5 period a bit error results [30].

In order to analyse a signal it is useful to characterise the signal jitter and interpret the distribution function to determine the cause of the jitter.

[1] Phase-locked-loop circuit, as described in sec. 5.4.2.

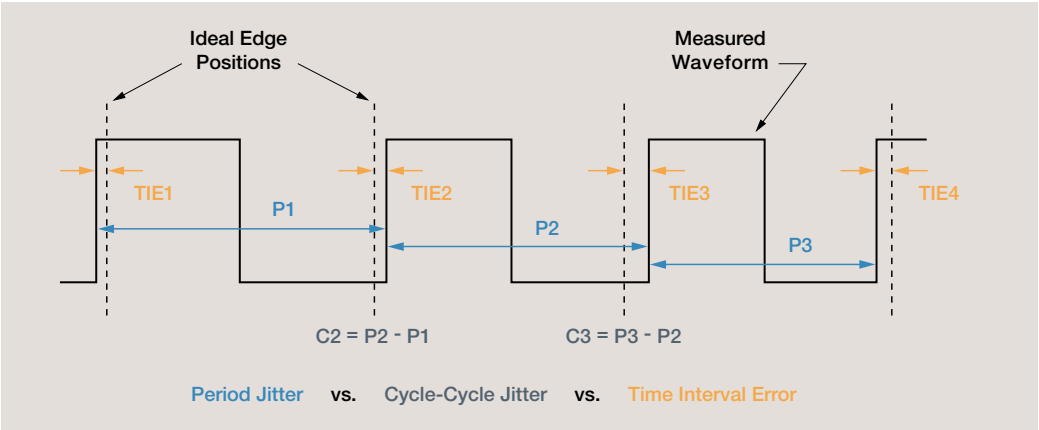


Figure 5.1: Illustration of period jitter, cycle-to-cycle jitter and time interval error of a waveform. Adapted from [30].

In the following a jitter model [30] is presented along with the different types of jitter and their pdf, respectively. A map of the jitter model is presented in fig. 5.2

- Random Jitter
  Random jitter (RJ) originates from Johnson thermal noise and as such individual contributing noise sources might not be normal distributed. However, the central limit theorem [31] states that the composite effect of uncorrelated statistical sources can be approximated as normal distributed. Hence, RJ follows an unbounded Gaussian distribution. Due to the unboundedness of RJ, special attention to the sample size of a jitter measurement has to be taken. Since this type of jitter can theoretically become infinitely large, the probability to measure a jitter value larger than the current bound increases with increasing sample size.

- Deterministic Jitter
  In contrast to RJ, deterministic jitter (DJ) is reproducible and non-normal distributed. As individual contributing sources for DJ are bounded, deterministic jitter is bounded as well. Continuing, DJ can be further specified.

  - Periodic Jitter
    If DJ appears in cyclic fashion and uncorrelated with repeating

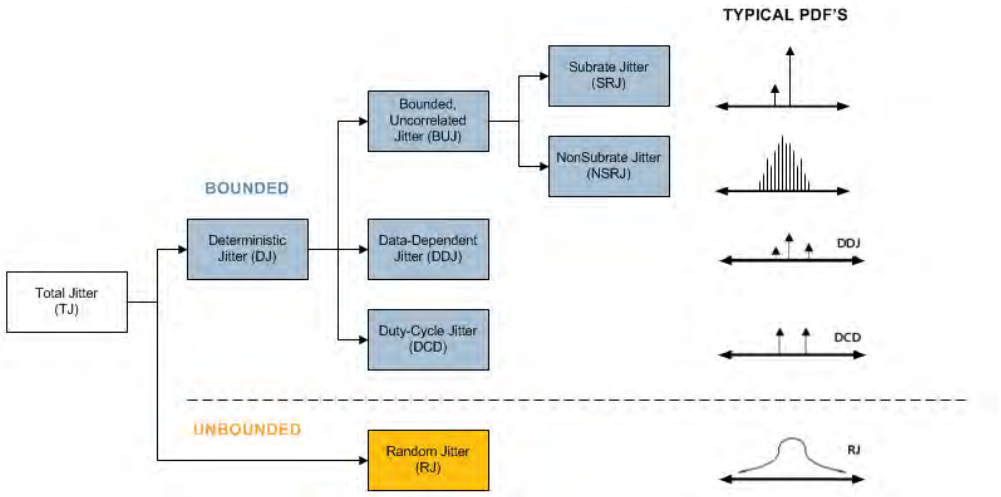


Figure 5.2: Jitter map illustrating the relation between different types of jitter and their probability distributions. Adapted from [30].

data streams it can be identified as periodic jitter (PJ) [30]. Possible causes include electromagnetic interference and power supply noise.

- Duty-Cycle Dependent Jitter
  Duty-cycle dependent jitter (DCD) can have two main causes. Either the slew rate of the rising edges of a digital signal differs from that of the falling edges or the decision threshold for a certain signal is misplaced [30].
- Data Dependent Jitter
  If the jitter intensity is time dependent and correlated to data streams being processed, it is likely that certain voltage levels or frequencies cause resonances coupling into the system. Such jitter is called data dependent jitter (DDJ).
- Bounded Uncorrelated Jitter
  Bounded and uncorrelated PJ (BUJ) is induced through crosstalk between electrical conductors [30]. Any non-harmonic BUJ (SRJ[2]) induced is likely generated by signal processing in logic devices, which is why some chip developers recommend shielding. This

[2]Substrate Jitter, as shown in fig. 5.2.

cause of jitter is however not only limited to on-substrate logics. If BUJ is larger than SRJ it is likely non-substrate jitter (NSRJ) originating from logic devices on other nearby substrates.

- Total Jitter
  The results of a jitter measurement may be a convolution of any of the above types of jitter as many contributing factors play a role. The effect of multiple jitter types influencing a measured signal is illustrated in fig. 5.3. Due to factors described above and also observable in fig. 5.3 the actual measurement might produce significantly non Gaussian results. Hence, a peak-to-peak measurement might be evaluated. The total jitter can be approximated as in eqn. 5.2.

$$T = D_{Pk-Pk} + 2nR_{rms} \quad , \tag{5.2}$$

  where T denotes the total jitter, D_{Pk-Pk} the peak-to-peak value of the DJ, R_{rms} the root mean square value of the random jitter and n is a coefficient based on the bit error rate (BER) of the associated clock. Typical values range around $n = 10^{-12}$ [32].

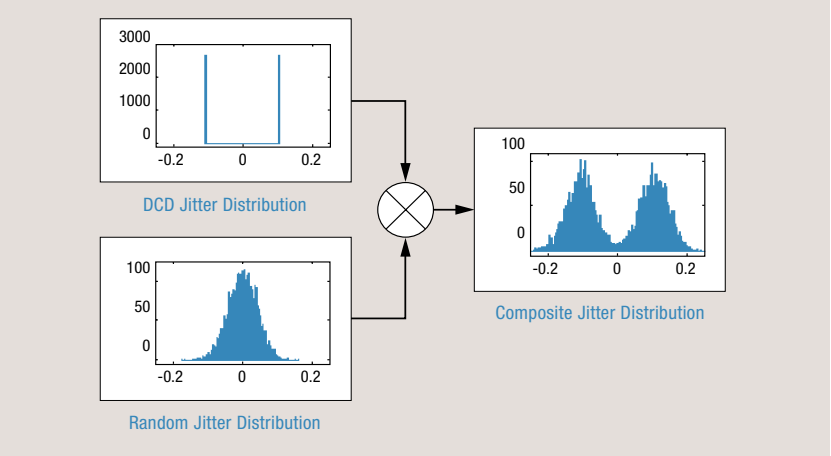


Figure 5.3: Illustration of the composite effect of different types of jitter. Adapted from [30].

- Sampling Jitter
  When converting a signal using an analog-to-digital converter (ADC)

the sampling is typically assumed to be periodic with a constant period length. However, for varying period length due to signal jitter, the sampling process might produce invalid bins and thus the conversion a distorted signal. This signal error is proportional to the slew rate and the amplitude of the input signal. Furthermore, the effect of different types of jitter on the sampling process can be differentiated. While random jitter introduces broadband noise, deterministic jitter adds spectral components to the sampling input signal [30]. Effects of sampling jitter can be significant for high frequency signals such as the clock signal in the Mu3e DAQ.

To approximate the influence of actual measurement tool, in most cases an oscilloscope, on the measurement, eqn. 5.3 is used [32].

$$Jitter\ Floor = \sqrt{\left(\frac{Oscilloscope\ Noise}{Slew\ Rate}\right)^2 + \left(Sample\ Clock\ Jitter\right)^2}\ , \tag{5.3}$$

where the oscilloscope noise mainly affects the vertical signal axis and the sample clock jitter is the intrinsic jitter of the measured object influencing the horizontal signal axis distortion.

5.3.2 Rise Time

Digital signals are ideally approximated by step functions. In reality, however, due to finite capacitances and inductances, the edges are tilted from their nominal vertical position. This results in a non-zero rise time. According to the United States Federal Standard 1037C [33], rise time is defined as the time a step function takes to change from a specified low value to a specified high value. Generally, the low value is set as 10% and the high value as 90% of a specified step height.

5.3.3 Phase

In this thesis the phase difference between two signals is of interest. Imagining a periodic waveform each repeating value of the waveform occurs at a certain point in time repeatedly. Also, a waveform can be imagined as a pointer chart

in the complex plane. Now, an angle between two points circumnavigating the circle in the complex plane can be defined as the phase. This relative displacement between two specified points on both waveforms referenced to the same time is the differential phase between two signals.

5.4 Tools

5.4.1 Eye Diagram

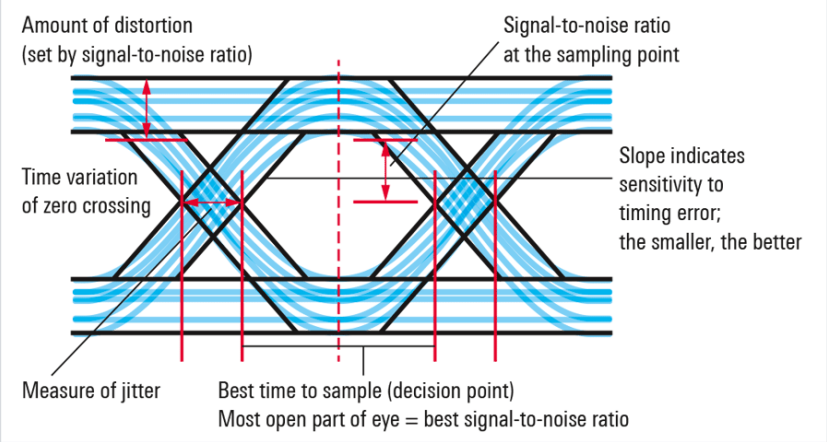


Figure 5.4: An eye diagram of a signal distorted by signal impurities. Also shown are the factors distorting the signal and how they can be interpreted from the eye diagram. Adapted from [34].

By overlaying all possible bit sequences of a digital signal on an oscilloscope with high persistency, an eye diagram is generated. In this thesis, only the clock signal which only consists of periodic changes from the low to the high and to the low state again, is of importance. Such a diagram can be used to analyse the quality of a transmitted digital signal. On the x-axis the time and on the y-axis the voltage level of the signal is shown. As the ideal digital signal is a perfect rectangular pulse, for the eye diagram in the ideal case the convolution of all possible bit sequences, i.e. all possible sequences of rectangular pulses, is expected. Due to signal impurities the eye diagram opening and the slope of the rising and falling edges are decreased as shown in fig. 5.4. Most importantly the eye height indicated the quality of the dig-

ital signal with the ideal case being that the low level is below the digital low level decision threshold and the high level above the digital high level decision threshold. In this case the amplitude of the signal is equal to the eye height. Secondly, the eye width can be used to determine the maximum data rate of the signal. The time duration between two eye crossings is called the bit period which is the inverse of the bit rate for the transmitted signal.

5.4.2 Phase Locked Loop

A phase locked loop (PLL) circuit is used to determine the phase difference between a given reference signal and a signal generated by a voltage controlled oscillator (VCO) included in the PLL. The goal is to produce an output signal, which possesses the a rational multiple of the reference signal frequency with equal phase to the input. This is done by comparing the phases of both signals. A constant phase between both signal yields equal frequencies of the signals. Central to any PLL are the phase detector (PD) and the VCO.

- Phase Detector

  Shown in fig. 5.5 is the schematic of one of the most basic PD's. More complicated, but also more exact solutions provide not only sensitivity for phase but also frequency.

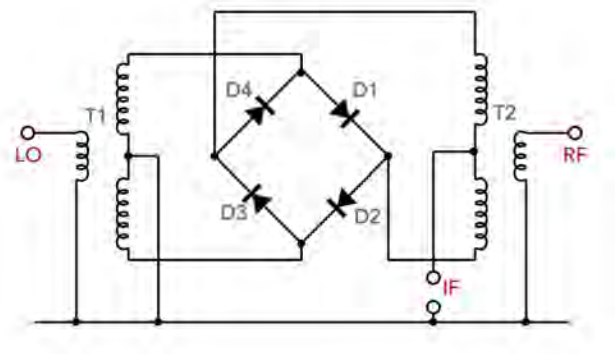


Figure 5.5: Schematic of a simple phase-only sensitive phase detector. Adapted from [35].

As observable in fig. 5.5 the frequency of the oscillations of the reference signal (RF) and the VCO signal (LO) are captured through the inductive current of a coil. Then, in a diode ring the signals are correlated. The output of programmable amplitude and signal type then has a frequency equal to the value of the frequency difference and is produced at IF. The output signal is largely influenced by the coils used in this setup as there the phase detection resolution is set.
The PD produces a constant voltage, if the phase difference between the two given signals is constant. For signals of different frequencies, hence non-static phase difference, the PD produces an output voltage that is oscillating at the frequency equal to the value of the frequency difference of the two given signals.

- Voltage Controlled Oscillator

  A VCO possesses the characteristic that it's output frequency is monotonously related to the input voltage. As the PLL error voltage (PD output voltage) increases the VCO frequency increases as well. For the case of a locked loop the error voltage stays at a constant level such that the VCO frequency stays constant as well; the VCO frequency is the same as that of the PLL reference.

Finally, the quality of the PLL output signal largely depends on the VCO since for a locked loop, the VCO ideally produces an output signal of desired type and a frequency equal to the reference frequency. The VCO's jitter and rise time are also the signal characteristics of the PLL output. Through the VCO the output signal type (differential or single ended) and amplitude are set.

It is important to tune the frequency range of the VCO to the frequency acceptance range of the loop filter of the PLL. A loop filter resembles a network of capacitors, inductances and resistors which work together to produce a band pass filter. This can easily be visualised using the transmission function for a bandpass filter in Laplace space:

$$G(s) = \frac{2ds\omega_0}{s^2 + 2ds\omega_0 + \omega_0^2} \quad with \quad \omega_0 = \sqrt{\frac{1}{LC}} \quad and \quad d = \frac{R}{2\omega_0 L} \quad , \qquad (5.4)$$

where R denotes the resitsance, L the inductance, C the capacitance, ω_0 the resonance frequency, s the frequency, and d the band width.

By plotting eqn. 5.4 as a Bode diagram one can easily see the suppression of frequency components above and below the band pass. For PLLs it is important to match the bandwith of the loop filter to the frequency range of the VCO. If this is not the case, the VCO might lock onto a frequency component not present in the reference signal but induced by the PD thus producing an unwanted output. Furthermore, the loop filter influences the output signal quality through shaping the phase noise, governing the frequency agility of the PLL and determining the loop stability [35].

A block diagram of the main components of a PLL is shown in fig. 5.6 and the process of a PLL locking onto a reference signal described below.

1. The PD takes inputs from the reference and the VCO and determines the phase difference. Then, the PD produces an error voltage oscillating with a frequency equal to the determined frequency difference.
2. This error voltage then passes through the loop filter which acts as a band pass filter, removing all frequency components outside of the VCO tuning range, hence the PLL capture range.
3. The filtered error voltage is then supplied to the VCO.
4. The VCO frequency changes monotonously with the error voltage, meaning that for a higher error voltage the VCO frequency rises as well. Consequently, the error voltage reduces the frequency difference between the reference and the VCO. This cycle ends with the error voltage reaching a constant level, meaning a constant phase difference between the reference and the VCO. The reference and the VCO now oscillate at the same frequency. As the PD reduces the input amplitude itsself and thus induces a frequency response, the frequency difference will only be minimised, but never completely eliminated.
5. In the case of a steady state phase offset the loop is locked onto the reference and the output frequency is equal to the input frequency.

PLLs can be used in a wide variety of applications and can be found in nearly all communications electronics. Possible applications include frequency synthesis, signal modulation and demodulation and clock recovery.

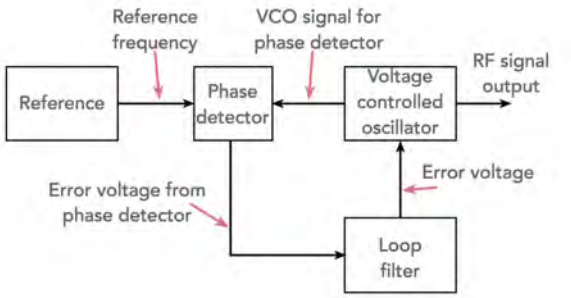


Figure 5.6: Block diagram of a phase locked loop. Adapted from [35].

5.4.3 DSPLL

Implemented in the Si5344 is a dual stage cascaded phase locked loop (DSPLL). Here, the first loop resembles a conventional narrow-band PLL with very low phase noise. Since for the inner loop only a narrow frequency band has to be captured, a very low jitter and phase noise 15 GHz LC-oscillator is used. The LC-oscillator is digitally controlled by a frac-N divider. Here, the frac-N divider divides the VCO output signal by integer division to match its frequency to the one of the PLL input signal such that the phases can be detected by the PD. The second outer loop, as shown in fig. 5.7, implements an analog wide band PLL. Herein, the outer loop performs the synchronisation of the inner loop output to the external reference, further jitter attenuation and clock multiplication to the desired frequency [36].

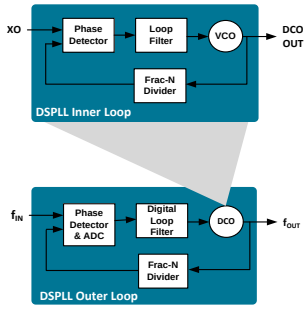


Figure 5.7: Block diagram of a dual stage phase locked loop. Adapted from [36].

As the DSPLL is implemented digitally using analog-to-digital convert-

ers and digital-signal processing, it has a programmable bandwidth and frequency range with a timing resolution of one part-per-trillion. Consequently, due to the on-chip realisation, no component changes for different output configurations are necessary.

5.5 Termination

For electrical circuits and connections it is important to match the impedance of all electrical conductors of a system. Generally the conductor impedance if given by $50\,\Omega$. Mismatched lines can lead to hazardous effects like signal reflection, power loss and even short cuts. In digital signals such effects result in status misinterpretation and in analog systems in noise interference. To avoid such effects, termination circuits consisting of RC-networks are used to match the impedance of individual links. For the termination it is important to know the signal type which will be carried by the link as different signalling standards require different impedances, capacitances and voltage levels [37]. Ordinarily, the termination circuit is implemented on the receiver side.

5.6 Coupling

Electrical connections can either be DC- or AC-coupled. When AC-coupling an electrical connection a capacitor is added in series. This capacitor filters out the DC-component, the constant voltage level offset of an electrical signal. Thus, the removal of a voltage offset improves the resolution of signal measurements [38]. Depending on the signal frequency, the capacitor size has to be adapted. For faster frequency components it is useful to use smaller capacitances as the associated charge times are smaller. Hence, capacitors can be combined in parallel to filter out different frequency components. Furthermore, different signal standards use different common mode-voltage levels. Hence, different coupling capacitances are used for different signal standards. For DC-coupling no additional capacitor is needed, as both the AC-component (voltage amplitude) and DC-component (common mode voltage) are passed through.

Chapter 6

Clock Transmission Board Design

The main goal of this thesis is the design of the Clock Transmission Board (CTB). Therefore, the required functionality described in section 4 was analysed. Corresponding to these requirements electrical components were chosen and the schematic along with the printed circuit board (PCB) layout were designed. For the PCB design Autodesk Eagle Version 9.1.0 (education) [39] was chosen.

6.1 Requirements and Characteristics

The CTB will receive the 125 MHz clock signal via an optical link as in fig. 4.3. Then, the signal will be jitter attenuated and manipulated before being sent via an electrical link to the FPGA of a filter farm PC. As the overall goal is to supply the filter farm FPGA with a synchronised clock signal of less than 10 ps jitter rms, the Si5344 any output, any frequency, jitter attenuator (section 6.2.1) was chosen as the central IC on the PCB. Furthermore, the reference clock signal for the Si5344 will be provided by a VCO. For testing purposes two single ended and one differential electrical connectors additionally to the optical connector on the input side and two differential and two single ended electrical connectors on the output side were included. Both the optical transceiver and the Si5344 are controlled via an SPI interface through a ten pin header. As the interface voltage level of the optical transceiver differs from the communication voltage level of the Si5344 voltage level converters are applied. Also the reset signal for the Si5344 will be provided through the ten pin header. In a design similar to the Si5344

Evaluation Board [40] the chip is provided with three core voltages and two output voltages. Each of the voltage levels is converted using linear voltage regulators and for each pair of outputs as well as two of the core voltages the voltage level can be chosen as 1.8 V, 2.5 V or 3.3 V. The whole board is powered with a 5 V power source which can be connected either through a SMA connector, a Phoenix terminal block or a USB 3.0 type B connector. Finally, the form factor of the CTB was determined corresponding to the final application inside a filter farm PC case. Consequently, the CTB has the outer dimensions of a PCIe short card and can be mounted to a PCIe slot such that the input connectors can be connected from the outside of the filter farm PC case.
The use of galvanic decouplers was evaluated in order to avoid ground loops between the CTB and the filter farm PC it is deployed in. As of today, the fastest galvanic decoupler is the capacitive decoupler. Still, the maximum signal rate allowed by capacity decouplers is 150 Mbaud. Thus, new constraints on the applicability of the CTB would arise. However, the added complexity of supplying an external voltage, the question of whether in it's final application a galvanically decoupled external voltage source is providable and the frequency constraints introduced by a galvanically decoupling device led to the decision of not including galvanic decouplers into the current CTB design.

6.2 Electrical Components

In the following section the main electrical components of the CTB will be presented.

6.2.1 Silicon Laboratories Si5344

Central for the CTB is the Si5344 10 channel, any frequency, any output, jitter attenuator and clock multiplier. This chip was chosen based on its jitter characteristics and in- and output channels. Incorporating technologies like DSPLL™ and MultiSynth™ as described in section 5.4.3, it is capable of producing output jitter of less than 90 fs rms for any combination of in- and output amplitude, signal type and frequency [41]. Specifically, MultiSynth™ is a low jitter (1 ps jitter rms) fractional divider combined with phase error correction [42] and is used to produce multiple unrelated

outputs using a single chip, hereby reducing PCB development complexity. An external crystal is required. The Si5344 supports an input frequency range of 8 kHz − 750 MHz for differential signals and 8 kHz − 250 MHz for single ended signals. Similarly the output range is given by 1008 Hz − 1028 MHz for differential signals and 8 kHz − 250 MHz for single ended signals. Common output amplitude voltages for LVDS, LVPECL, LVCMOS, CML and HCSL signals and terminations as well as AC and DC in- and output coupling are supported. The Si5344 possesses an in-circuit programmable non-volatile memory in order to ensure a controlled and known state during power up. Programming is done via a serial interface.

A block diagram of the Si5344 is shown in fig. 6.1. The chip has four in- and outputs and an optional feedback loop. Integer dividers are used on all channels. An external crystal provides the reference signal and an DSPLL™ is used for jitter attenuation and clock multiplication. MultiSynth™ enables the use of multiple unrelated in- and output signals over a single DSPLL. The chip itsself is powered by two supply voltages VDDA and VDD with a total power consumption of 730 mW, and status monitors as well as a SPI and I^2C interface are supported.

6.2.2 Silicon Laboratories Si5344 Evaluation Board

In order to set a benchmark for the performance of the CTB, measurements of the rise time, frequency stability, phase stability and jitter were conducted on the Si5344 Evaluation Board. The evaluation board provides an excellent base for evaluating the real life performance of the Si5344. Hereby, the evaluation board supports LVDS, LVPECL and LVCMOS in- and outputs in its standard configuration. These signal types will be used in the Mu3e DAQ and thus the measurement procedure is efficient. While the CTB possesses additional functionality by implementing an optical transceiver and being optimised to fit the requirements for the application in the Mu3e DAQ system, the evaluation board is programmable not only via a serial interface, but also via the ClockBuilder Pro™software over USB. On the evaluation board, a micro processor, as visible in fig. 6.2, is used to translate the USB protocol into an I^2C interface protocol and also to read various power consumption and temperature values. Furthermore, the evaluation board is powered via the same USB port that is used for programming.

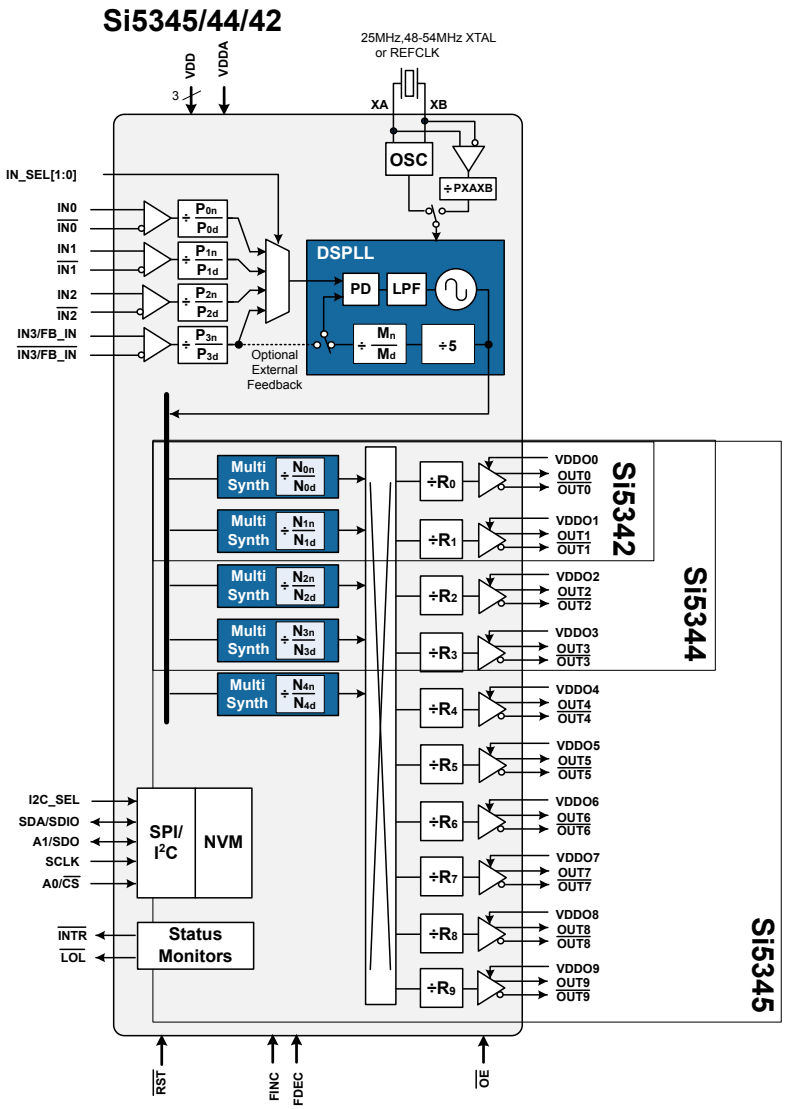


Figure 2.1. Block Diagram Si5345/44/42

Figure 6.1: Block diagram of the Si534x family. On the CTB the Si5344 with four in- and outputs is used. Adapted from [43].

Figure 6.2: The Si5344 Evaluation Board. Central on the PCB the Si5344 is visible as well as the control MCU on the lower right side. Also, four in- and outputs as well as an external reference signal input XA/XB and a ten pin header for serial interface programming are visible. Adapted from [40].

6.2.3 Kyocera CX3225SB

In order to produce a low jitter reference clock for the DSPLL of the Si5344 a combination of an internal and an external oscillator as indicated in fig. 6.3 is used. This clock is needed for freerun and holdover modes [41]. Furthermore, a recommended PCB layout can be found in [43]. The Kyocera CX3225SB48000D0FJCI 48 kHz oscillator was chosen in agreement with [44] and possesses a load capacity of 8 pF and a total power dissipation of 200 µW [45].

6.2.4 Finisar FTLF8528P3BxV

A bidirectional Finisar FTLF8528P3BxV 8.5 Gb/s Short-Wavelength SFP+ Transceiver equipped with a 850 nm laser diode is used on the CTB. The transceiver uses less than 500 mW and can be controlled via a two-wire serial interface. Total jitter induced by the transceiver at a data rate of 8.5 Gbit/s is 83.5 ps [46]. Furthermore, the transceiver assembly connects to a TE Connectivity surface mount PCB connector and is held by a Finisar V23838-S5-NI cage [47].

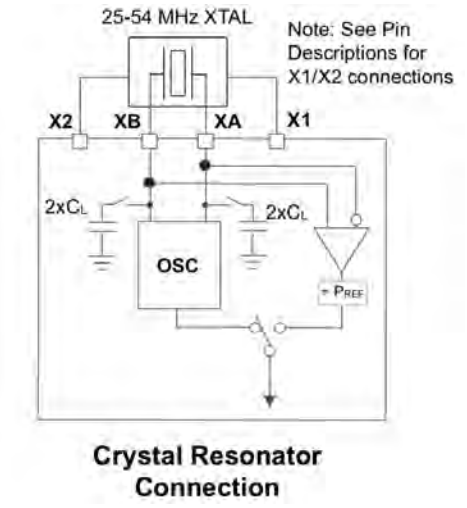


Figure 6.3: A combination of external crystal and internal oscillator generate the reference clock for the Si5344 DSPLL in freerun and holdover mode. Adapted from [41].

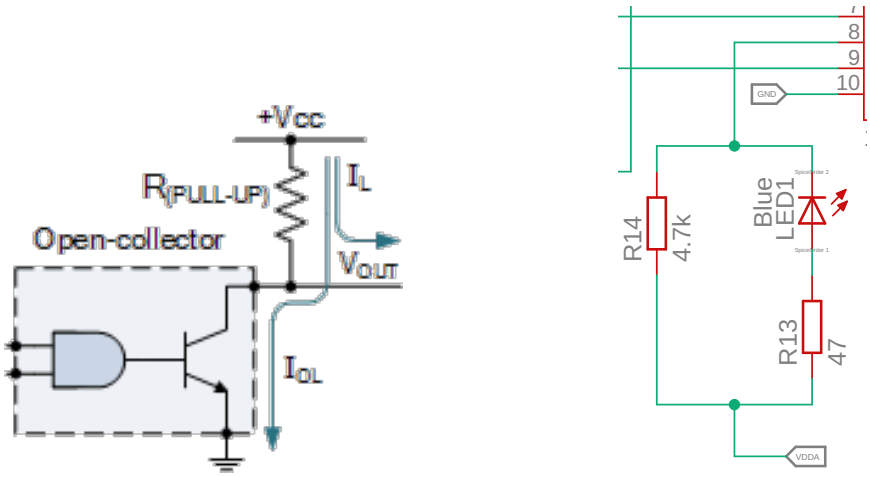
Since the two-wire serial interface uses a different voltage level than normally used for SPI protocols and on the CTB both the Si5344 and the transceiver are controlled via the same connection a Texas Instruments TXB0101 1-bit bidirectional level-shifting and voltage translator with auto direction-sensing is used.

6.2.5 SMA Connectors

For both electrical signal in- and outputs and power supply, SubMiniature version A (SMA) connectors are used.

6.2.6 Voltage Conversion

While the CTB is powered by a 5 V voltage source which can be connected through a USB connector, a SMA connector or a wire port, throughout the CTB three voltage levels of 1.8 V, 2.5 V and 3.3 V are used as core and output voltages. Consequently, linear power converters are used. Adapted from the Si5344EVB the linear power converters Maxim Integrated MAX8869, Texas Instruments TPS795 and Texas Instruments TPS76201 are used.



(a) The open-collector output of a transistor logic connected to a pull-up circuit. Adapted from [49].

(b) Pull-up circuit used on the TFAULT pin of the optical transceiver on the CTB.

Figure 6.4: Comparison of theoretical pull-up circuit schematic and implementation in the CTB schematic.

6.2.7 USB Connector

The main power supply of the CTB in its final form and also implemented on the is a universal serial bus (USB) 3.0 type B connector, enabling a supply voltage of 5 V and a maximal current of 900 mA [48].

6.2.8 Pull-Up Circuits

Floating is a terminology used in electronics for the undetermined state of an open pin as the voltage actually applied to the pin in the open state is not defined. To avoid such behaviour, pull-up resistors are used to ensure a high state for the open pin and the low state when the pin is grounded. Here, high corresponds to a logic 1, high voltage level and low to a logic 0, low voltage level.

In order to explain the pull-up circuit, the open collector output is approximated as a switch. For the switch open state the output is effectively connected to the Vcc power supply via the pull up resistor. Consequently, the current flowing into the transistor logic input is minimised. High ohmic values ensure no voltage drop over the pull-up resistor as current-flow is min-

imised in the high state. Thus, nearly the complete voltage value of Vcc is applied to the input creating a high, logic 1 state [49]. To the contrary case when the switch is closed, the transistor logic output is grounded, thus producing a logic 0 low voltage state. Because the pull-up resistors high ohmic value, Vcc is not grounded as not much current flows through the resistor. To determine the minimum resistor value needed for the application eqn. 6.1 is used.

$$R_{pull-up,min} = \frac{V_{cc} - V_{OL}(max)}{I_{OL}(max)} \qquad and \qquad I_R = \frac{V_{cc}}{R_{pull-up}} \quad , \tag{6.1}$$

where $R_{pull-up}$ denotes the pull-up resistor value, V_{cc} is the power supply voltage rail, $V_{OL}(max)$ is the maximum transistor logic input voltage for the low state and I_{OL} is the maximum transistor logic input current for the low state. Furthermore, the current going through the pull-up resistor can be determined using Ohm's law, where I_R is the resistor current. This is useful, if a diode is implemented in the pull-up circuit. Equivalently, the maximum resistor value can be determined using the minimum voltage and current values for the high state.

The process described above is visualised in fig. 6.4a, where $V_{out} = V_{cc} - V_{OL}$, I_L is the current for the open switch state and I_{OL} is the current for the closed switch state.

One example where such a circuit is used on the CTB is pin 8 of the optical transceiver to PCB connector as shown in fig. 6.4b. Here, an open-collector output is pulled up with a pull-up resistor and the status is indicated using a LED. A logic 0 indicated normal operation (LED off) whereas logic 1 indicated the loss of the signal. Further implementations include the output enable pins on all linear voltage converters.

6.2.9 Voltage Divider

Two impedances in series can be used to generate a circuit which produces an output voltage which is a fraction of its input voltage, as shown in fig. 6.5a. Here, the input voltage V_{in} is distributed over $Z_1 + Z_2$ over ground, while V_{out} is connected through Z_2 to ground. Thus, eqn. 6.2 gives the voltage relation.

$$V_{out} = \frac{Z_2}{Z_1 + Z_2} \cdot V_{in} \quad , \tag{6.2}$$

where V_{out} denotes the output voltage, V_{in} the input voltage and Z_x the impedance, respectively.

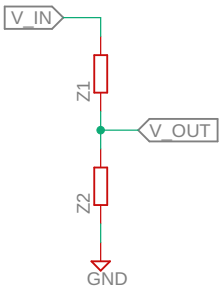
Most prominently on the CTB, voltage divider circuits are implemented to enable supply voltage conversion. Shown in fig. 6.5b is the voltage divider circuit used to set the output voltage for the channels 0 and 2 on the CTB. On this voltage netclass (all circuits corresponding to a certain signal class where certain parameters like PCB trace width and PCB clearance are set accordingly to the signal characteristic), a Texas Instruments TPS76201DBVR linear voltage divider is used. Furthermore, a voltage divider circuit is used to vary the feedback (FB) voltage which drives the voltage converter output voltage internally. Typical circuit designs are given by [50] and thus the output current driven by the feedback loop can be calculated by eqn. 6.3. Hence, Z_1 in eqn. 6.2 is always given by R104, while Z_2, depending on the jumper JP16 position is either given by R111, R111 + R110 or R111 + R109. Consequently the feedback voltage is set such that the output voltage at VDDO0 is, in the same order as for Z_2, 1.8 V, 2.5 V and 3.3 V. Additionally, R100 is installed to limit the output current. Further filtering is done by the implementation of a RC-network consisting of C64, C65 and R106 and to improve transient response and noise rejection, the output is coupled to ground via the polarised bypass capacitance C66 [50].

$$V_{out} = V_{ref} \cdot \left(1 + \frac{Z_1}{Z_2}\right) \quad , \tag{6.3}$$

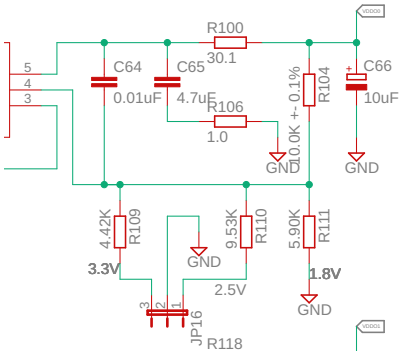
where V_{out} is the output voltage as in fig. 6.5a and fig. 6.5b, $V_{ref} = 0.6663\,\mathrm{V}$ is an internal reference voltage and Z_x with $x = 1, 2$ are the respective voltage divider impedances.

6.3 CTB Schematic

Development of the CTB started after research with the conception of the schematic, which can be found in Appendix A: CTB Schematic. This was done with Autodesks Eagle Software. As many of the required parts for the



(a) Theoretical basic voltage divider circuit, where the voltage V_{in} is transformed to the value of V_{out} using a series of two impedances Z_1 and Z_2.



(b) A voltage divider circuit as implemented in the channel 0 and 2 output voltage supply circuit on the CTB.

Figure 6.5: Comparison of theoretical voltage divider circuit schematic and implementation in the CTB schematic.

CTB were not available in the Eagle parts library, their schematic symbols and layout packages were either downloaded from the Ultralibrarian [51], SnapEDA [52] and Silicon Laboratories websites or designed by the author. In the following section the CTB schematic will be explained in detail by page.

6.3.1 Si5344 and SPI Interface

Since the Si5344EVB already possessed much of the functionality needed for the CTB, the schematic of the CTB was adapted from the Si5344EVB. Consequently, the Si5344 was placed at the heart of the CTB. As a PLL reference, the Kyocera CX3225SB VCO was used. Noticeably, the VCO ground differs from the general CTB ground which has to be kept in mind during the design of the CTB PCB layout. Moving on, the Si5344 is controlled via a four-wire SPI interface which can be connected to an external drive through a ten pin header. Additionally, the global reset signal line, external 1.8 V and 3.3 V power supplies and ground, and a two-wire serial interface for the optical transceiver are implemented in the ten pin header. Voltage supplies and external ground can be connected the local CTB power supplies and ground through the use of jumpers. Both the inverted output-enable pin ($\overline{OE}$) and I^2C-select pin (I2C_SEL) were connected to ground in order to enable the

ouput mode of the Si5344 and choose SPI as the implemented serial interface, All voltage supply net classes, which can be found in in tab: 6.1, are supplied to the Si5344 in parallel to a 1.0 µF capacitance connected to ground, respectively. Hence, unwanted supply noise which can result in additional jitter is minimised. Furthermore, 0 Ω resistors are implemented to enable the installation of further filtering elements during testing. Finally, the status registers for inverted data interrupt ($\overline{INTR}$, indicating a change of state in either of the out-of-frequency and loss of input signal), inverted loss of the oscillator reference clock ($\overline{LOS\_XAXB}$) and inverted loss of lock of the DSPLL on the input signal ($\overline{LOL}$) are indicated through a LED connected via a pull-up resistor to VDD_MCU.

6.3.2 I/O 0 and 1

While both inputs and outputs 0 and 1 are differential, input and output 0 connect to the optical transceiver and input and output 1 connect to electrical SMA connectors. The optical transceiver is implemented as advised in [46]. Both status indicators transmitter fault and loss of signal indication are a open collector/drain output connected to a pull-up circuit. Continuing, the rate selection (4.25 Gbit/s or 8.5 Gbit/s each) for receiver and transmitter, respectively, can be done by setting the pin open or high with the use of jumpers. A two wire serial interface with a data and a clock line is voltage transformed from 3.3 V to 1.8 V using the TXB0101DRLT voltage level shifter for each line, respectively. To improve jitter performance, the power supply pins for the voltage level shifter are capacitively coupled to ground. The individual power supply nets for the receiver and transmitter will be discussed in section 6.3.4. Finally, the input nets are done equally for both channels 0 and 1.
First, the signal is AC-coupled using a 10 nF capacitance to filter high frequency and a 0.1 µF capacitance for lower frequency components. Then both lines are differentially terminated [37] and further capacitively filtered. Shown in fig. 6.6 is the complete termination and coupling circuit for input channel 0. On the output side, jitter attenuation is implemented with a 1.0 µF capacitance placed directly at each Si5344 output pin. For the electrical output 1 another RC-network is implemented for noise reduction and reflection prevention. Empty lots for different terminations and couplings were included for output 1.

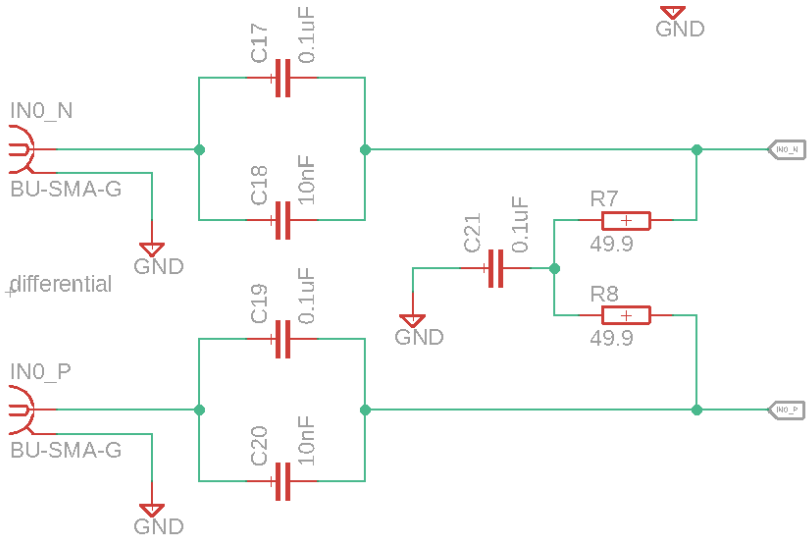


Figure 6.6: Termination and coupling circuit used on the input channel 0 of the CTB.

6.3.3 I/O 2 and 3

Inputs and outputs 2 and 3 can be configured as differential or single ended individually. All inputs are LVCMOS parallel terminated using a 100 Ω pull-down resistor to ground and a 100 Ω pull-up resistor to VDDOx (x indicating the channel, respectively) [53]. All outputs are noise attenuated using a RC-network.

6.3.4 Voltage Regulators

A 5 V supply voltage is connected to the CTB through either a SMA connector, two wire ports or a USB 3.0 type B connector. To overcome possible power negotiation issues the USB data pins were shorted using a 200 Ω resistor while otherwise only the 5 V and ground pins of the USB connector are connected. Different voltage supply netclasses for the CTB are generated from the global 5 V netclass using linear power regulators and voltage dividers as shown in tab. 6.1.

Before each voltage regulator the 5 V supply voltage is capacitively coupled to ground for jitter attenuation. Every voltage regulator can be switched on and off individually using a jumper in a pull up circuit. Normal opera-

Supply Netclass	Voltage [V]	Voltage Converter	
VDD	1.8	MI MAX8869	Core Digital Supply
VDDA	3.3	TI TPS795	Analog Supply
VDD_MCU	3.3	TI TPS76201	Digital I/O Supply
VDDO0	1.8/2.5/3.3	TI TPS76201	Clock Output Supply
VDDO1	1.8/2.5/3.3	TI TPS76201	Clock Output Supply

Table 6.1: CTB supply voltage netclasses, the corresponding voltage values and the linear voltage regulator used, respectively.

tion happens in the connected state. Furthermore, jumpers can be used to choose between 1.8 V, 2.5 V and 3.3 V output voltages for the VDD, VDDO0 and VDDO1 netclasses. On the output side a RC-network is used for noise attenuation and reflection prevention. To avoid back-currents from ground level a polarised capacitance is used.

An individual noise attenuation circuit is applied between VDDA and the optical transceiver receiver (VCCR) and transmitter (VCCT) power supply as recommended in [46].

The Peripheral Serial Interface express (PCIe) connector is used purely for stable installation of the CTB inside a filter farm PC and is thus not connected.

6.4 CTB PCB Layout Design

After the design of the schematic the next step in the CTB development was the design of the printed circuit board (PCB) layout. This was done with Autodesks Eagle Software [39]. First, the general form factor was determined corresponding to the PCIe short graphics card form factor [54] [55]. The outer dimensions of the CTB are given by 175.26 mm · 106.68 mm. Furthermore, the layer setup was determined based on the required trace impedances and recommendations [43], [56], [57], [58].

Layer Requirements

- For the transmission of differential signals impedance controlled traces

are necessary. Hence, a layer with 100 Ω impedance is needed.

- For the transmission of single ended signals impedance controlled traces with 50 Ω are needed.
- A solid copper ground layer is needed for good shielding.
- A power supply layer is needed for the distribution of the different power supply netclasses.
- Slow CMOS control signals can be routed on outer layers.

Layer Recommendations

- Clock output layers should always be internal layers with ground reference planes directly above or below to improve shielding, avoid crosstalk during transit, provide better impedance control and provide a low-impedance path for the return current flow. However, vias must be used for transit and thus inductances are induced.
- Ground flooding near traces whenever possible improves shielding.
- A solid ground plane improves noise attenuation and heat distribution. Vias should be added to avoid the ground plane acting as an antenna for electromagnetic signals generated by high-speed signals.
- Plugged vias should be used underneath high-power devices to improve heat dissipation.
- A crystal shield should be applied on the device layer directly underneath the oscillator. On all layers no traces or flooded planes should be underneath the crystal.
- Especially for power distribution planes and traces enough area should be provided to carry a sufficiently current to avoid voltage drop and provide good heat dissipation. This has to be kept in mind when placing vias as too close placement can induce significant voltage drops.

The layer design was also influenced by the netclasses needed for the CTB. A netclass combines all circuits which are used for similar purposes. For instance, a power netclass will need larger PCB trace width and clearances

to accommodate higher currents and heat dissipation than signal netclasses. Separate netclasses for power, ground, differential, single ended and slow standard signals were used. After the layers requirements and recommendations were discussed, the layer setup shown in fig. 6.7 was designed:

1. Layer: device layer, with low speed CMOS control/status signals, ground flooded
2. Layer: crystal shield, ground plane
3. Layer: differential clocks, ground flooded (100 Ohm)
   Between layer 3 and 4 a core of 600 µm was applied to provide shielding.
4. Layer: single ended clocks, ground flooded (50 Ohm)
5. Layer: power distribution, ground flooded
6. Layer: low-speed CMOS control/status signals, ground flooded

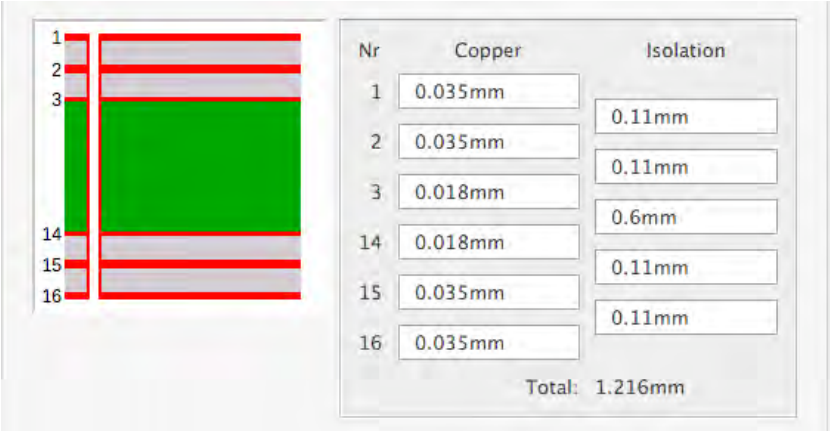


Figure 6.7: CTB PCB layer construction. Six layers with the outer two connected by prepreg material, respectively and a large core at its centre are connected by vias.

With this setup, multiple advantages were combined. While low speed CMOS signals are routed on the outer layers, the impedance controlled fast-signal layers are shielded on both sides from solid copper layers and a large core. Impedance calculations were provided by Contag [59], checked with the

Saturn PCB software and are shown in fig. 6 and fig. 7 in the Appendix Part B: CTB Layers. Contag was chosen for the manufacturing of the CTB.
After the general parameters for the CTB were set, design rules were determined. These were on one side affected by the impedance requirements for fast-signal lines and current requirements for power lines and also by the technical limitations given by Contag.

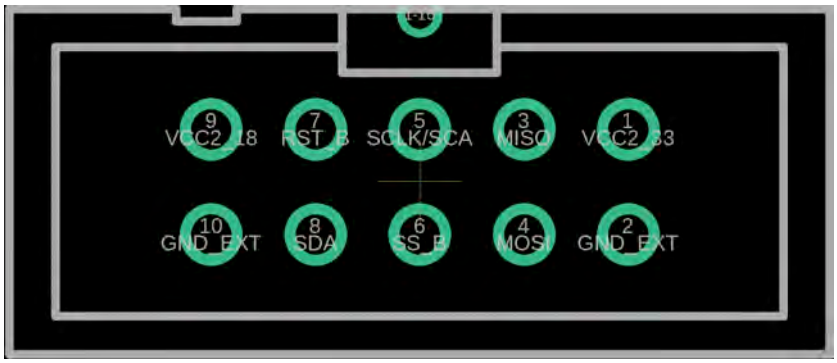


Figure 6.8: CTB ten pin header pinout for serial interface communication.

Next, all necessary connectors were placed. Hereby, the individual position of a connector was determined corresponding to its use. In its final deployment, the CTB will be installed inside a filter farm PC housing. Correspondingly, the USB power supply connector, the optical transceiver socket, two single ended and a pair of differential SMA input connectors were placed facing the rear of the CTB so that they can be accessed from the outside of the filter farm PC housing. Also, holes were included to allow the installation of a PCIe faceplate with screws and stands. All electrical clock outputs were placed at the front of the CTB so that they can be connected on the inside of the filter farm PC. While the remaining single ended channel 3 input connectors, the SMA power connector and the ten pin header were placed at the side of the CTB PCB facing aways from the filter farm PC motherboard to be accessible from the side, the power supply wire ports were installed at the side of the PCB facing towards the filter farm PC motherboard as access is only needed during testing. The ten pin header pinout is shown in fig. 6.8 and serial interface pin relations are explained in tab. 6.2. To connect external ground (pin 10 and 2) to the CTB PCB ground, short JP4. Since both the SPI interface of the Si5344 and the two-wire interface of the optical transceiver use the same clock, the position of JP6 determines which

interface is connected to the clock provided by an external host.

Continuing, the voltage supply conversion circuits were placed closest to the USB power connector. Hence, minimal distance lies between the 5 V power supply and the linear voltage converters and voltage drop is minimised. A solid copper plane with intermittent vias supplies 5 V to each voltage converter. Planes going along the short axis of the CTB PCB then supply the converted voltages to the consumers. Through the use of jumpers, VDDA (JP23), VDD (JP19), VDDO1 (JP18) and VDDO0 (JP14) can be enabled. While VDD and VDDA are enabled when leaving their respective jumpers open, VDDO1 and VDDO0 are enabled through shorting their respective jumpers. VDD, VDDO0 and VDDO1 supply 1.8 V per default. However, the output voltage can be changed to 2.5 V or 3.3 V through setting the jumpers JP21 (VDD), JP20 (VDD1) and JP16 (VDDO0) accordingly. While the Si5344 was placed centrally on the board to equalise trace lengths between in- and outputs and their corresponding influences on jitter, all remaining parts were placed in a matter to minimise trace length. Bypass capacitors were applied on all in- and outputs of the Si5344 and placed as near as possible to the pins, respectively.
The next step was to connect all elements with traces and solid copper planes and fill the remaining spaces with ground fill. On the internal layers, the high-speed signal traces were routed corresponding to the impedance requirements calculated by Contag. The corresponding trace parameters for differential signals are shown in fig. 6 and fig. 7 in the Appendix Part B: CTB Layers. Length compensation for the individual signal lines of differential signals were included and only larger than right angles were used on fast-signal lines to avoid signal phase error and reflection. Layer 3 containing all differential signal traces is shown in fig. 10 and layer 4 containing all single ended signals in fig. 11 in the Appendix Part C: CTB Layout.

Layer 2 is a solid ground copper layer as shown in fig. 9 and layer 5 was used for the power distribution planes as in fig. 12. Here, trace width was maximised to fill all the space available to minimise voltage drop. All remaining low-speed CMOS control and status signals were routed on the outer layers which are shown in fig. 8 and fig. 13. Several options are available for controlling the Finisar transceiver as indicated in [46]. Thus, the transmitter can be enabled by shorting JP1 and the receiver and transmitter rates can be set to either 2.125 Gbit/s or 4.25 Gbit/s per fibre channel by leaving JP2 (receiver rate select) and JP3 (transmitter rate select) open or to 8.5 Gbit/s per fibre channel by shorting them, respectively. LEDs indicating transmit-

Figure 6.9: Three CTB prototypes. On the lower side of the picture the optical transceiver can be seen; the output side of the board can be observed at the top of the image.

ter fault and loss of signal were also included through open-collector circuits. A low output on these LEDs indicates normal operation. Status LEDs indicating loss of lock (LOL_B), loss of oscillator reference (LOSXAXB_B) and either input signal loss or loss of lock on the input signal (INTR_B) for the Si5344 were installed. Here, also a low output indicates normal operation. Furthermore, the outer layers were ground filled to equalise the weight distribution of the PCB and prevent bending under mechanical stress. These ground fill planes were removed in the vicinity of the signal in- and outputs to keep the controlled impedances. Vias were added where applicable to avoid ground planes picking up electromagnetic noise from fast in- or output signals. Finally, all parts were labeled with their name and value, respectively. Also pin descriptions and a logo were added.

CTB Pinout	Si5344 Pinout	Finisar Optical Transceiver Pinout
3 MISO	15 A1/SDO	–
4 MOSI	13 SDA/SDIO	–
5 SCLK/SCA	14 SCLK	5 SCA
6 SS_B	16 A0/CSb	–
7 RST_B	17 RSTb	–
8 SDA	–	4 SDA

Table 6.2: CTB ten pin header pinout and the pin descriptions of the connected Si5344 and Finisar optical transceiver pins, respectively. The connections to the optical transceiver are voltage transformed from 3.3 V coming from the transceiver to 1.8 V on the ten pin header. External ground and CTB PCB internal ground can be connected by shorting JP4.

A picture of the three CTB prototypes is shown in fig. 6.9.

Chapter 7

Clock Transmission Board Programming

The Si5344 on the CTB cannot only be used as a jitter attenuator but also as a clock generator in freerun mode. Apart from these basic operating modes, other features of the chip can be configured by setting register values. This is done by creating a register map with Silicon Laboratories Clock Builder Pro software. To communicate this register map to the Si5344, a serial peripheral interface was chosen for the CTB.

7.1 Serial Peripheral Interface

Serial peripheral interface (SPI) is a de-facto standard, allowing individual interpretation of a common idea. A master-slave architecture, where the slave is synchronised to a clock generated by the master is used. While only one master can be implemented with SPI, multiple slave devices are possible. Generally, four links make up one SPI connection:

- SCLK: A clock signal generated by the master to synchronise the communication between all slaves and the common master. Alternative nomenclature includes CLK.
- CS: Every slave is given an individual chip select (CS) link which indicates data flow. Normally, this signal is inverted, meaning a active low. The master toggles the low state with a falling edge of the chip select link activating the slave and then transmits or receives data. Since

sometimes pull up power of the slave is not sufficient, a pull up resistor on this link is recommended to prevent false-assertion of the communication status. Alternative nomenclature includes CS_B, SS, NSS and SS_B (B or an overline indicating an inverted state).

- MOSI: The master-in-slave-out (MOSI) link is used to transmit data from the master to the slave. Alternative nomenclature includes slave-data-in (SDI).
- MISO: Data sent as a response from the slave is transmitted via the master-in-slave-out (MISO) link. When unused, the MISO link should be pulled high by the slave to allow communication from the other slaves. If the driving power of the slave is not sufficient, a pull-up resistor is recommended. Alternative nomenclature includes slave-data-out (SDO).

SPI allows high transfer speeds as high amounts of data can be transferred without address and command bits. The speed of the link is only limited by the parasitic capacitance of the SCLK link which at increasing clock speeds overcomes the signal. Otherwise, communication frequencies can be chosen freely as integer divisions of a maximum frequency which is set by most devices as 16 MHz[60]. As such, normal SPI frequencies are between a few kHz and a few MHz. For SPI, however there is no boundary to slower speeds. Furthermore, SPI communication is in full duplex mode, meaning that all links are unidirectional and the MISO, MOSI links are separate[1].

SPI communication works like a shift register. The signal transmitted through MOSI gets returned by the MISO link. The exchange of data thereby can me conducted as shown in fig. 7.1. The master asserts a low state on the CS_B of the respective slave. This enables the slaves communication circuit. After a delay of a few clock cycles the master transmits a command followed by data. Every bit is synchronised to a clock cycle edge of the clock signal which is toggled for each transaction. Depending on the data transmitted through MOSI the slave then responds by sending data through MISO. Communication is terminated by the master pulling CS_B high.

Special attention has to be taken when selecting the polarity and phase of a SPI connection. Additionally to the chip select link either being an

[1]This is the case for four-wire SPI. Alternative approaches combine the MISO and MOSI link.

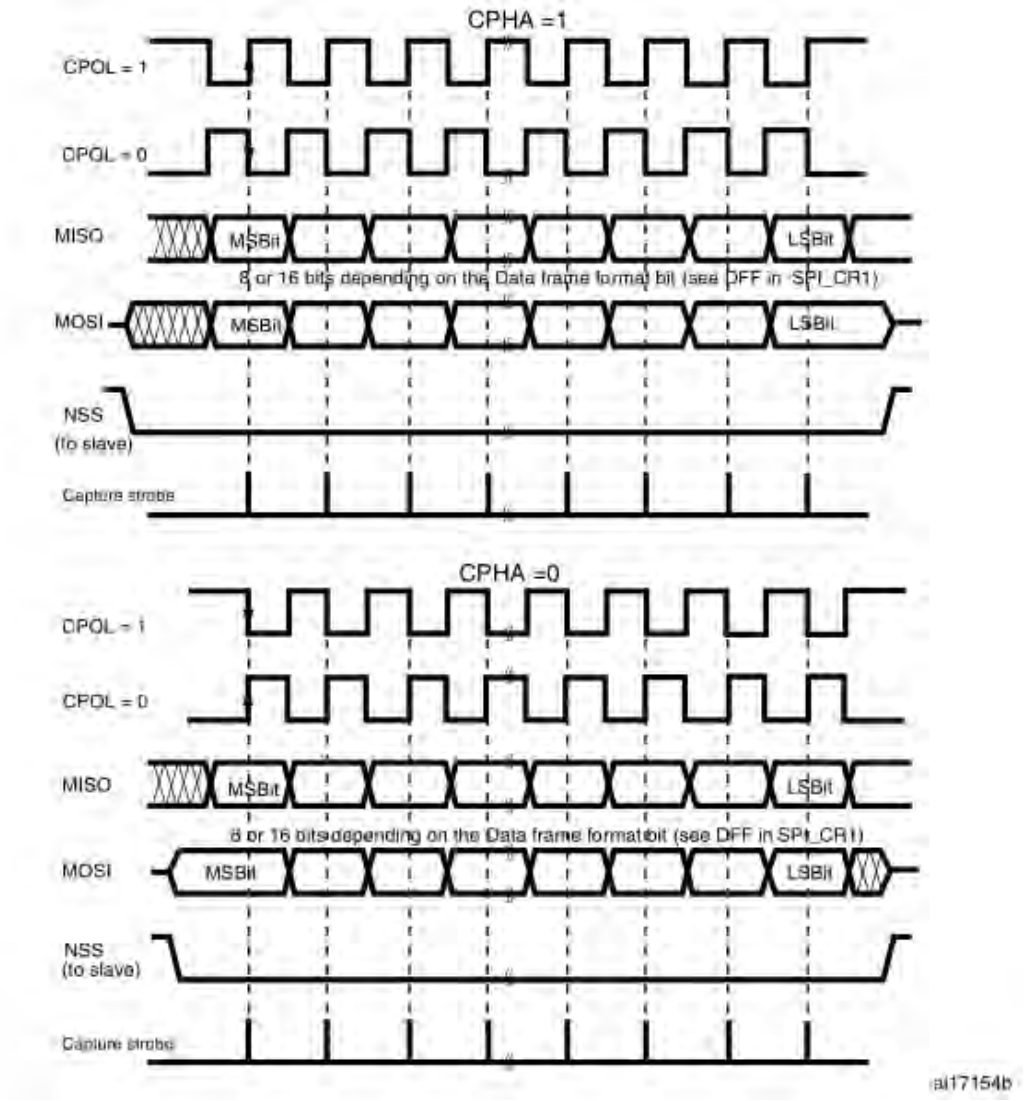


Figure 7.1: Diagram indicating four different combinations of phase and polarity options for four-wire SPI connections. The capture strobe indicates the data sampling point. Adapted from [61].

active-low (CS_B) or active-high (CS) signal, the clock signal can either idle in the low or the high position. Here, the former describes a clock polarity of CPOL= 0 and the latter of CPOL= 1. Both possibilities are shown in fig. 7.1. Furthermore, the signal phase CPHA determines whether the received data on both the master and the slave side is sampled at the leading or trailing edge of the clock signal. As shown in fig. 7.1, for a signal sampled at the rising clock edge phase and polarity are equal. For the contrary case, phase and polarity are not the same. This leads to four different versions of this kind of SPI, as shown in tab. 7.1.

	Sampling on Rising Edge	Sampling on Falling Edge
Clock Idles High	CPHA = 0 & CPOL = 0	CPHA = 1 & CPOL = 0
Clock Idles Low	CPHA = 0 & CPOL = 1	CPHA = 1 & CPOL = 1

Table 7.1: Different phase and polarity combinations for four-wire SPI. Adapted from [61].

As such, SPI offers many advantages over other serial interfaces: high transmit frequencies allow high data rates and both hard and software implementations are simple. However, due to the high speeds of the signals distances between master and slave should be kept short. Furthermore, SPI needs more wires as other serial interfaces as for N slaves $N + 3$ links are needed.

7.2 SPI on the CTB

7.2.1 SPI host: FPGA

After failed attempts with both a Raspberry Pi and the Si5344 EVB, an Arria 10 DE5a-Net FPGA development board [62] as shown in fig. 7.2 was used as the SPI master for the CTB as the slave. As sources of error for the other devices master communication speed, the correct CS_B signal and the correct common-mode voltage were diagnosed. The SPI links were connected to the CTB via the RS422 expansion header on the FPGA board, on which the pin layout of the ten pin header of the CTB was based. Here, the pin RS422_DIN was connected to MISO, RS422_DOUT was connected

to MOSI, RS422_DE_n to CS_B and RJ45_LED_R to SCLK. The implementation of the SPI protocol was done by Dr. Alexandr Kozlinskiy and Marius Köppel in the C programming language compiled by Quartus [63] for the Nios II microprocessor [64] implemented on the FPGA.

Figure 7.2: Arria 10 FPGA used as the SPI host for the CTB.

7.2.2 SPI Slave: Si5344 on the CTB

Communication with the Si5344 is possible via the I^2C protocol or SPI. For the application on the Si5344 SPI was chosen. Hence, the I2C_SEL pin was grounded, selecting SPI as the mode of communication. Furthermore, in its standard configuration the Si5344 is set to four-wire SPI as shown in fig. 7.3. Although, three-wire operation can be selected by changing the SPI_3WIRE register bit. The common-mode voltage used for communication can be set in the IO_VDD_SEL register bit (for Si5344 registers, see [43]). Voltages can be chosen between VDDA (3.3 V) and VDD (1.8 V) and are set to 1.8 V as standard [41]. These configurations were also used for the CTB. Commu-

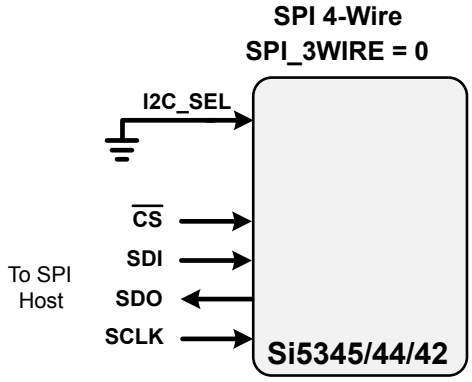


Figure 7.3: Connection diagram for the Si5344 in 4-wire SPI mode. Adapted from [43].

nication speed was set to 122 kHz.

All registers of the Si5344 are 8-bit addressable, while the register pages are 16-bit addressable with the first 8 bits being the page [65]. Continuing, reading or writing data always begins with the set address command followed by the read and write instruction. All possible commands can be found in [65]. As such, the command to read the value of register $52A$ is shown in eqn. 7.1. First the set address command is asserted after which the page register is set to page 5. Then, the next command is started by a set address command after which the value of register $2A$ on page 5 is read. It is important not to forget dummy bits $0xFF$ to keep CS_B low and SCLK enabled during the slave's response.

$$\begin{aligned} &\overbrace{0x00}^{SetAdress} \;/\; \underbrace{0x01}_{PageRegister} \;/\; \overbrace{0x40}^{Write} \;/\; \underbrace{0x05}_{Page5} \;/ \\ &\overbrace{0x00}^{SetAddress} \;/\; \underbrace{0x2A}_{RegisterPage} \;/\; \overbrace{0x80}^{Read} \;/\; \underbrace{0xFF}_{Return} \;, \end{aligned} \tag{7.1}$$

Another particularity of the communication with the Si5344 is shown in fig. 7.4. Again, the 16 bit register page command structure with 8 bit addresses is observable. Furthermore, a command is always sent before transmitting or receiving data. Finally, a delay longer than two clock periods is used between commands to prevent buffer overflow.

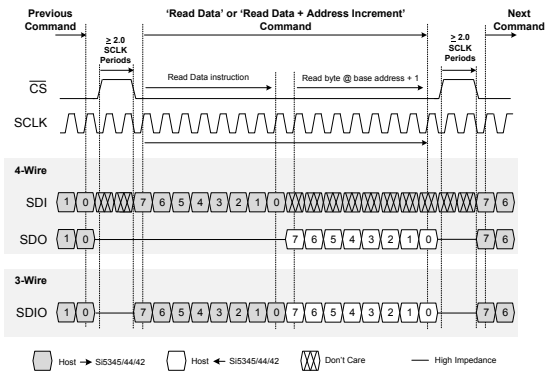


Figure 7.4: Timing instruction for the read and set address and read data command. Adapted from [43].

Chapter 8

Measurements

In order to characterise the impact of the CTB, measurements of the output signal jitter, rise time and phase stability were conducted. These quantities were chosen as they are responsible for possible bit errors produced by the filter farm FPGA in the case of a contaminated clock signal. Furthermore, signal types also present in the Mu3e setup were used. Consequently, frequencies of 625 MHz and 125 MHz with both single ended and differential termination and voltage levels of 2.5 V and 1.8 V were tested. While in the final setup the clock will be generated by the Mu3e clock generation board and then transmitted by the CTB to a filter farm FPGA as described in chapter 4, the test setup involved various stages. First, the signal characteristics of the clock generated by the Si5338 clock generator development kit were determined. Then, to set a benchmark for the CTB performance the Si5344 evaluation board's impact on the generated clock were determined. In the final test measurement setup for this thesis, a clock generated by the Si5338 was measured at the output of the CTB.

8.1 Measurement Instruments and Devices

8.1.1 Tektronix MSO 70404C Mixed Signal Oscilloscope

The signal characteristics were analysed with the Tektronix MSO 70404C Mixed Signal Oscilloscope. When working with oscilloscopes certain considerations regarding resolution have to be taken. The most important equations to keep in mind are given by [30], [66]:

$$\begin{aligned} \beta = \frac{\sigma}{\tau_{signal}}, \quad \sigma \in [0.35, 0.45] \quad , \\ \tau_{scope} \leq \tau_{signal} \quad , \\ \eta \quad = \quad \frac{1}{\lambda} \quad , \end{aligned} \tag{8.1}$$

where β is the oscilloscope bandwidth, τ_{signal} is the signal rise time, τ_{scope} is the oscilloscope rise time, η is the oscilloscope time resolution and λ is the oscilloscope sampling rate.

Furthermore, one has to keep in mind to divide the sampling rate λ by $\sqrt{12}$ due to the binning of the data. The Tektronix MSO 70404C possesses a bandwidth of 4 GHz and a sampling rate of 25 Gsamples/s. Consequently, the minimum rise time correctly measurable with this oscilloscope is 87.5 ps and the time resolution is given by 138.6 fs [67]. These values are the systematical errors of all measurements involving time measurement in this thesis. Used for frequency spectrum analysis and eye diagrams was the DPOJET feature of the oscilloscope. Also, the digital signal analyser included with this oscilloscope proved useful for the debugging of the SPI interface of the CTB.

8.1.2 Silicon Laboratories Si5338 Clock Development Kit

Used for the clock generation was the Si5338 clock development kit [68] as shown in fig. 8.1. The Si5338 can produce four any-frequency, any-output clocks. All common clock formats and voltages are supported at a very low jitter and very high frequency and phase stability. Programming of the board is done via the graphical user interface of the ClockBuilder software.

8.1.3 Clock Builder and Clock Builder Pro Software

Silicon Laboratories Clock Builder (CB, used for the Si5338) and Clock Builder Pro (CBP, used for the Si5344) softwares are used for the configuration of the Si5338 and Si5344 boards. A graphical user interface can be used to change operating modes of the chips, reference clock types, input and output characteristics such as frequency, phase, voltage, termination

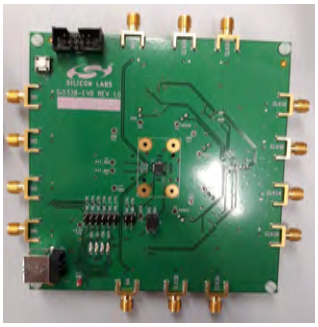


Figure 8.1: The Si5338 clock development kit board. While the board possesses four inputs for the generated clock signals to lock onto, for this thesis only the four output clocks were used. The output termination had to be soldered correspondingly to the signal standard that was used, respectively.

and coupling, and register settings. Register files created with CBP can be exported to external Si5344 chips. CBP communicates directly with a micro controller on the evaluation board via a USB link. Continuing, the micro controller translates the header file generated and sent by CBP into register settings for the DUT and transfers them via SPI to the DUT [69]. External I^2C hosts for the DUT can be installed via a ten pin header.

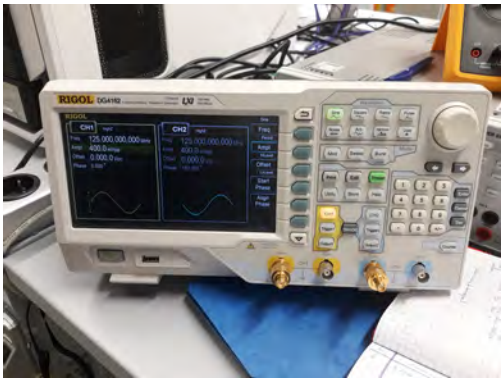
8.1.4 Hameg HMP4040

During the testing phase the CTB's power is supplied by the Hameg HMP4040 via a SMA link. This programmable power supply offers up to 384 W on four channels and is shown in fig. 8.2a. Per channel a maximum voltage of 32 V at a accuracy of $\leq 0.05\% \pm 5\,\mathrm{V}$ can be generated [70]. A feature which was used extensively was the current limiter on a set voltage level to prevent hazardous effects of high currents during electrical testing.

8.1.5 Rigol DG4162

The Rigol DG4162 two channel function/arbitrary waveform generator was used to verify measurement results and is shown in fig. 8.2b. However, at a frequency of 125 MHz only sinusodial waveforms can be generated instead of rectangular waveforms which would have represented better comparability to the actual clock signal [71]. A frequency of 625 MHz cannot be generated

(a) The Rhode-Schwarz Hameg HMP4040 programmable power supply used for testing of the CTB.



(b) The Rigol DG4162 was used to provide verification of measurement results.

Figure 8.2: Further components of the measurement setup.

with this device.

8.1.6 Measurement Standard

For all measurements the JEDEC standard JESD65B was chosen. JEDEC Solid State Technology Association is an organisation providing open standards and publications for the microelectronics industry. More than 300 companies subscribed to the standards set by JEDEC.

The standard important for this thesis is JESD65B: Definition of Skew Specifications for Standard Logic Devices from September 2003. Here, jitter is defined as "the time deviation of a PLL-generated controlled edge from its nominal position". For the measurement of jitter the measurement of more than 2000 clock cycles are recommended to achieve a sufficiently large sample size [29]. Also, for this thesis the total period jitter was measured as discussed on chapter 5. For the rise time and phase measurements undertaken for this thesis the same measurement standards were used.

8.2 Measurement Setup

In the following section the measurement setup for each device under test (DUT) will be explained.

8.2.1 DUT: Si5344 EVB

After the jitter, rise time and phase stability of the clock signal generated by the Si5338 were determined, a Si5344 evaluation board was used to provide a benchmark on jitter attenuation and signal cleaning for the CTB. Both the Si5344 evaluation board (EVB) and the Si5338 development board (DB) were connected to a PC with the Clock Builder and Clock Builder Pro software via USB, respectively. While the Si5338 was used for clock generation, the Si5344 performed jitter attenuation and signal manipulation. Finally, the signals were analysed using a Tektronix oscilloscope. The setup is shown in fig. 8.3.

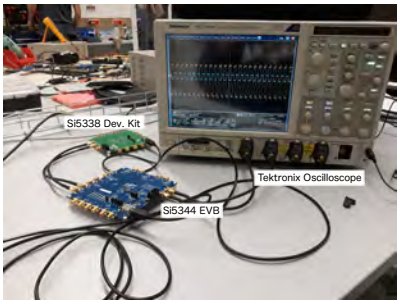
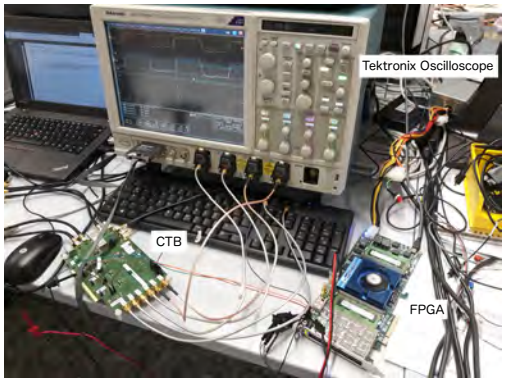


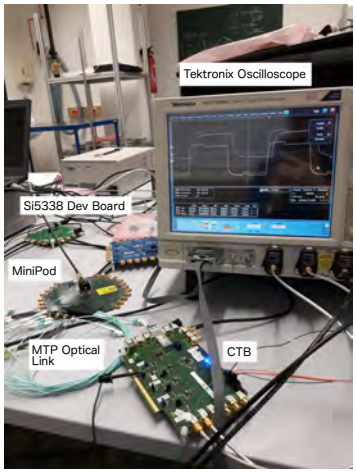
Figure 8.3: The measurement setup used for the determination of the Si5344 EVB signal characteristics.

8.2.2 DUT: CTB

Evaluating the CTB performance, the clock was generated with the Si5338 DB and then supplied to the CTB shown on the lower left side of fig. 8.4a via a SMA link. Furthermore, the CTB was programmed using the FPGA shown on the lower right side of fig. 8.4a. The signals were analysed using a Tektronix oscilloscope. To evaluate the optical characteristics of the CTB, a clock signal generated by the Si5338 DB and transmitted optically through a MiniPod transceiver was sent through a MTP optical link to the CTB as shown in fig. 8.4b. Then, the original signal coming from the Si5338 DB shown in violet on the oscilloscope's screen was compared to the signal coming from the CTB (orange) in fig. 8.4b.



(a) electrical signals.



(b) optical and electrical signals.

Figure 8.4: CTB measurement setups for the evaluation of:

8.3 Data Analysis

For the Mu3e experiment a jitter, rise time and phase stability of less than 100 ps were envisioned. In the following the measurement data taken for this thesis is analysed. Furthermore, it is evaluated whether the CTB can meet the signal quality goals set for the DAQ of Mu3e as discussed in chapter 4.

Tables 3 and 4 show the measurements made for this thesis ordered by the measurement number (no.), the device under test (DUT), the input and output signal types and frequencies.

While histograms for jitter, rise time and phase stability were done for all measurements and measurement channels, respectively, only one explanatory case is shown in Appendix part F in this thesis to illustrate the following procedure. All signals used conform to the LVDS standard [26] and are adjusted to 625 MHz[1]. Hence, for the Si5338 DB as device under test (DUT) an output signal of such characteristics was measured[2]. Continuing, for the Si5344

[1]For higher frequencies, generally, the effects of signal disturbances are more observable than for lower frequencies.

[2]For measurement 43 shown in Appendix part E the Si5338 generated two identical output clocks. One was used to generate an optical signal which was then processed by

EVB as DUT both input and output signals were chosen at 625 MHz LVDS (measurement 15). Finally, measurement 43 is shown for the CTB as DUT, where a 625 MHz optical clock generated by a MiniPod [22] which in turn is driven by a Si5338 is converted to a 625 MHz LVDS output clock by the CTB.

Figure 8.5: Complete waveform of measurement 44 (oscilloscope screenshot).

Typical waveforms that were used for measurements of jitter, rise time and phase stability had an appearance similar to the one of measurement 44 shown in fig. 8.5. Here, a 2.5 V LVDS differential signal of 125 MHz was generated by the CTB locked onto an optical input signal. The two differential links are shown in yellow and turquoise, their difference in orange and a reference signal generated by a Si5338 in green and pink. Below the waveforms in fig. 8.5 the rise time, jitter (standard deviation of the period) and phase performances of the signals can be observed. Also, the effects of pre-emphasis by the Si5344 are clearly visible. To improve the steepness of the rising edge the driver of the Si5344 increases the signal frequency at the beginning of every half period. Similarly, the signal frequency is decreased at the end of every half-period. Consequently, rising and falling edges are

the CTB and another was taken as a reference. This reference signal is used here.

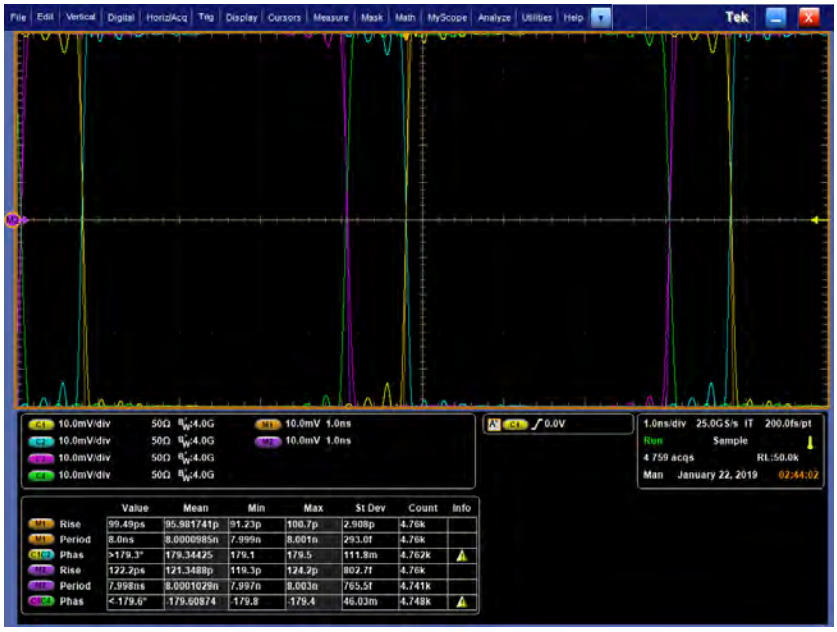


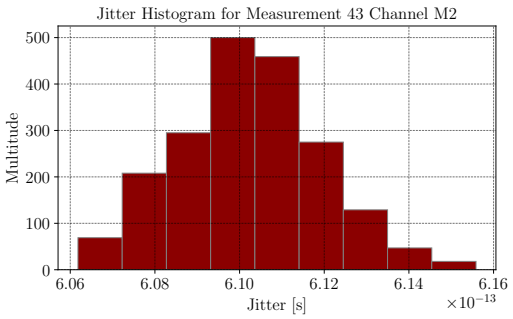
Figure 8.6: Optimised waveform of measurement 44 (oscilloscope screenshot).

steeper. As an artefact a step in the high and low voltage levels of the signal appears. For a clock signal the signal quality of the rising and falling edges is most important, while the exact form of the high and low states are irrelevant as long as the threshold for each state is met, respectively. In order to maximise the resolution of the rising and falling edges of the signal and thus create more exact measurements, the oscilloscope settings were adjusted to focus on these parts of the signal as shown in fig. 8.6.

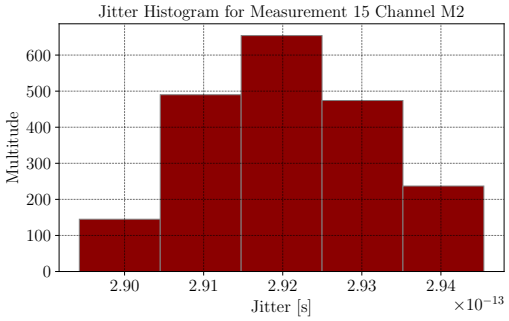
8.3.1 Jitter

While the DPOJET feature of the Tektronix MSO70404C provides detailed jitter analysis it was not used for this purpose during this thesis. Due to the minimum timing resolution of $\mathcal{O}(100\,\mathrm{fs})$ as calculated in sec. 8.1.1 and an expected jitter of the same order, DPOJET was not reliably able to trigger on jitter events. Thus, the standard deviation of the clock period was taken as a measure for the total jitter of the signal, as shown in fig. 5.1 in sec. 5.3.1. For each measurement 2000 samples of jitter events were taken, accordingly to

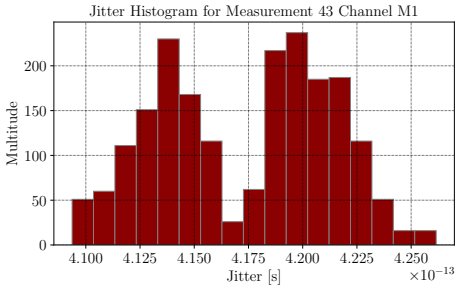
[29]. These were plotted in a histogram. For each histogram the binsize was chosen to be 1 fs to stay reasonably near the oscilloscope's timing resolution. The resulting histogram for the Si5338 DB is shown in fig. 8.7a, for the Si5344 EVB in fig. 8.7b and for the CTB in fig. 8.7c. Especially in the case of fig. 8.7c, the influences of a convolution of random and deterministic jitter as described in sec. 5.3.1 are observable in a double Gaussian distribution.



(a) Si5338.



(b) Si5344.



(c) CTB.

Figure 8.7: Jitter histogram for for each DUT, respectively.

To account for all measured values equally, the root mean square and the standard deviation as shown in eqn. 8.2 were taken of the data distribution of each histogram, respectively.

$$\overline{x} = \sqrt{\frac{1}{N}\sum_{i=1}^{N} x_i^2} \quad ,$$
$$\Delta x = \sqrt{\frac{1}{N}\sum_{i=1}^{N} (x_i - \overline{x})^2} \quad , \tag{8.2}$$

where $\overline{x}$ is the mean value, N is the number of samples, x_i are values in the distribution, Δx is the standard deviation for the mean value. For these formulas the samples are assumed to be uncorrelated.

By applying this method to all measurements the jitter performance of the DUT under different configurations was determined. Furthermore, the jitter values determined are shown in fig. 8.8 in the case of the Si5338 DB as DUT, in fig. 8.9 for the Si5344 EVB as DUT and in fig. 8.10 for the CTB as DUT. Also shown in these figures is the weighted mean of each distribution which was calculated with eqn. 8.3.

$$\overline{x} = \frac{\sum_{i=1}^{N}(x_i \cdot \omega_i)}{\sum_{i=1}^{N} \omega_i} \quad with \quad \omega_i = \frac{1}{\sigma_i^2} \quad ,$$
$$\sigma = \frac{1}{\sum_{i=1}^{N} \omega_i} \quad , \tag{8.3}$$

where $\overline{x}$ is the weighted mean, N is the sample size, x_i are the values of the distribution, ω_i are the weights for each value, σ_i is the variance of each x_i and σ is the total variance for the weighted mean. The weights were chosen as the reciprocal of the squared variance as each data point can potentially be part of an individual and uncorrelated probability distribution. Since different forms of jitter can have different probability distributions that convolute to a total spread such a case is present for the measurements made for this thesis.

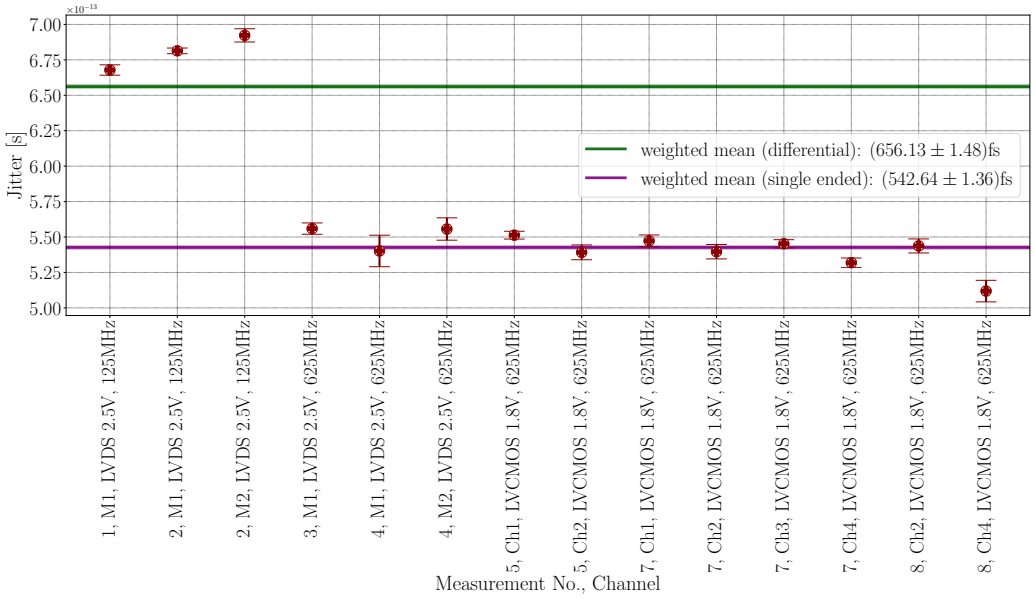


Figure 8.8: Si5338 DB jitter performance.

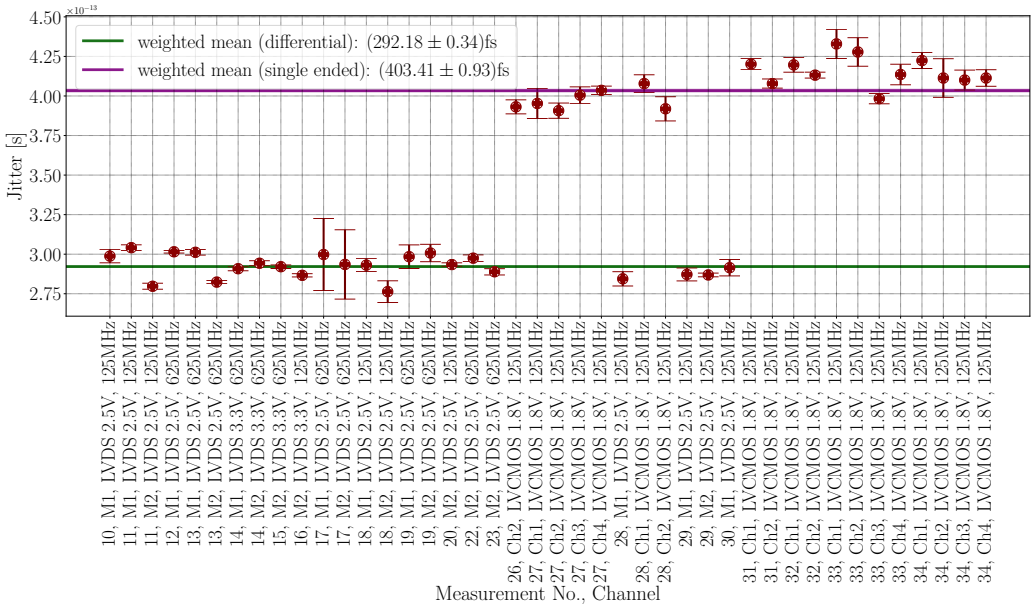


Figure 8.9: Si5344 EVB jitter performance.

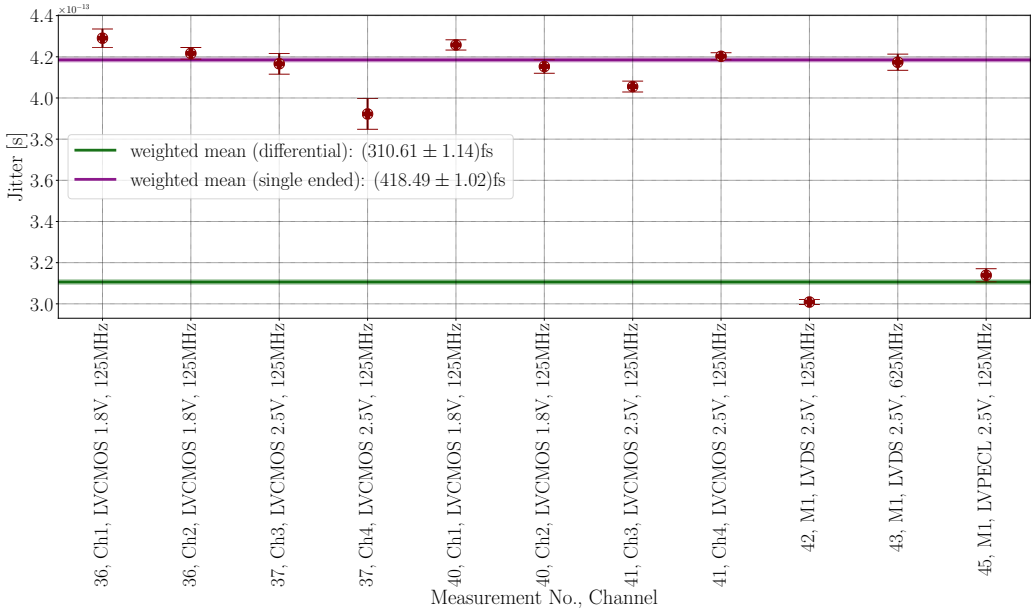


Figure 8.10: CTB jitter performance.

For the CTB and the Si5344 EVB a significant increase of jitter for single ended output formats compared to differential output signals is noticeable. Furthermore, the absolute value of the jitter decreases with increasing signal frequency while the relative jitter increases. Such effects are however anticipated as the Si5344 jitter performance for differential signals is significantly better than for single ended signals and jitter decreases for higher frequencies as described in [56]. According to [56] the Si5344 produces a signal jitter rms of 102 fs for a differential output signal of 625 MHz[3]. Consequently, the jitter values determined are in agreement with the manufacturer's specifications. The jitter measurement results are shown tab. 8.1. Here, an advantage of both the CTB and the Si5344 EVB over the Si5338 development board can be seen, justifying their roles as jitter attenuators. The CTB's jitter is comparable to the values achieved by the Si5344 EVB.

[3]This value, however, concerns the jitter directly at the chip output. Thus, jitter induced by the PCB, connectors and measuring equipment is not included.

DUT	Jitter differential [fs]	Jitter single ended [fs]
Si5338 DB	656.13 ± 1.48	542.64 ± 1.36
Si5344 EVB	292.18 ± 0.34	403.41 ± 0.93
CTB	310.61 ± 1.14	418.49 ± 1.02

Table 8.1: The weighted mean jitter and error of jitter for each DUT for single ended and differential signals.

8.3.2 Rise Time

The same procedure as explained in sec. 8.3.1 was used to determine the rise time of individual signals generated by each DUT for different configurations. Results for the Si5338 DB as DUT are shown in fig. 8.11, for the Si5344 EVB as DUT in fig. 8.12 and for the CTB as DUT in fig. 8.13. Exemplary rise time measurement histograms are shown in Appendix Part F. Again, the CTB achieves similar results as the Si5344 EVB.

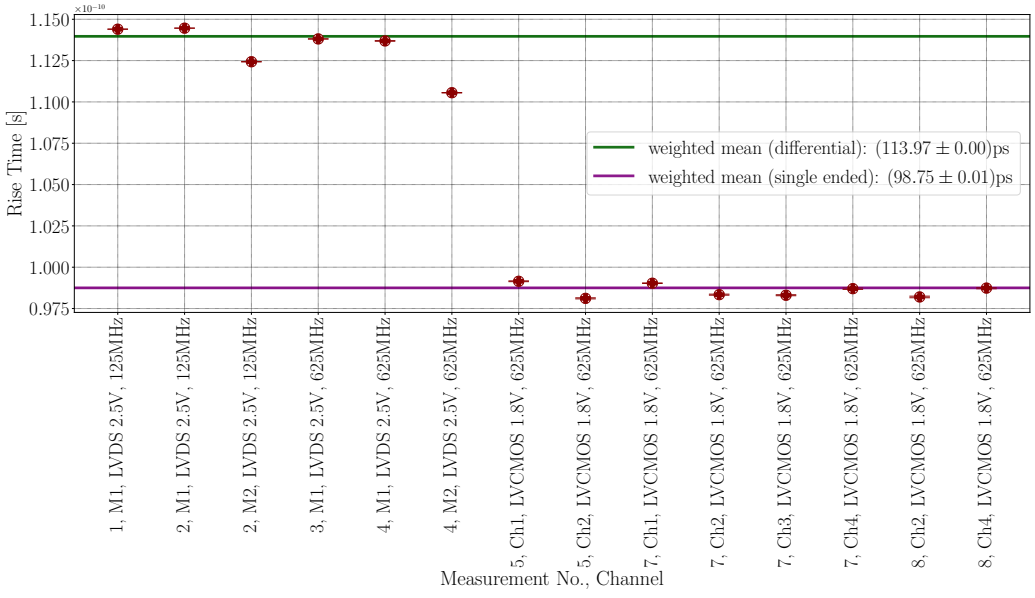


Figure 8.11: Si5338 DB rise time performance.

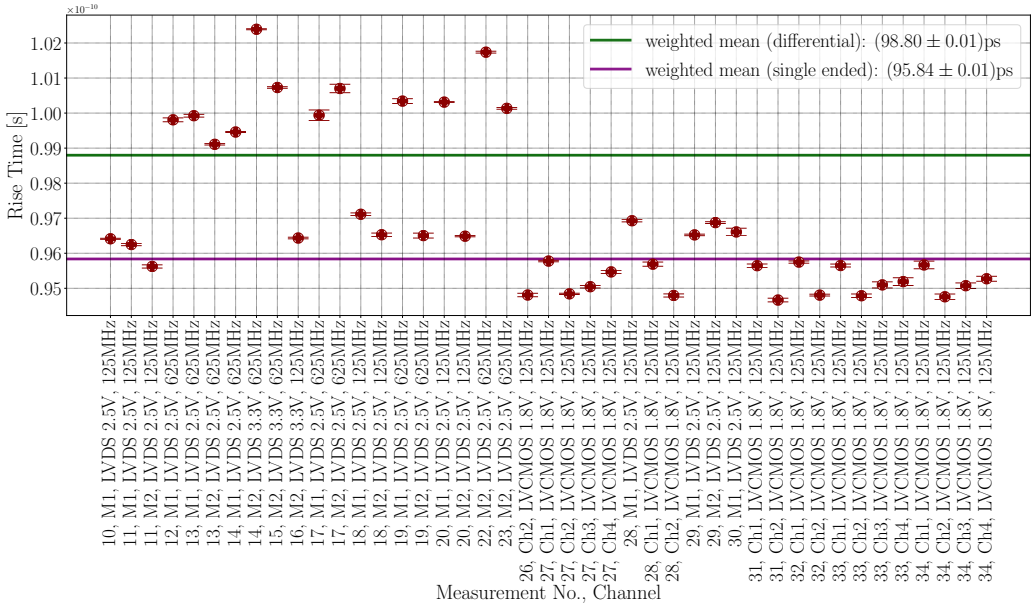


Figure 8.12: Si5344 EVB rise time performance.

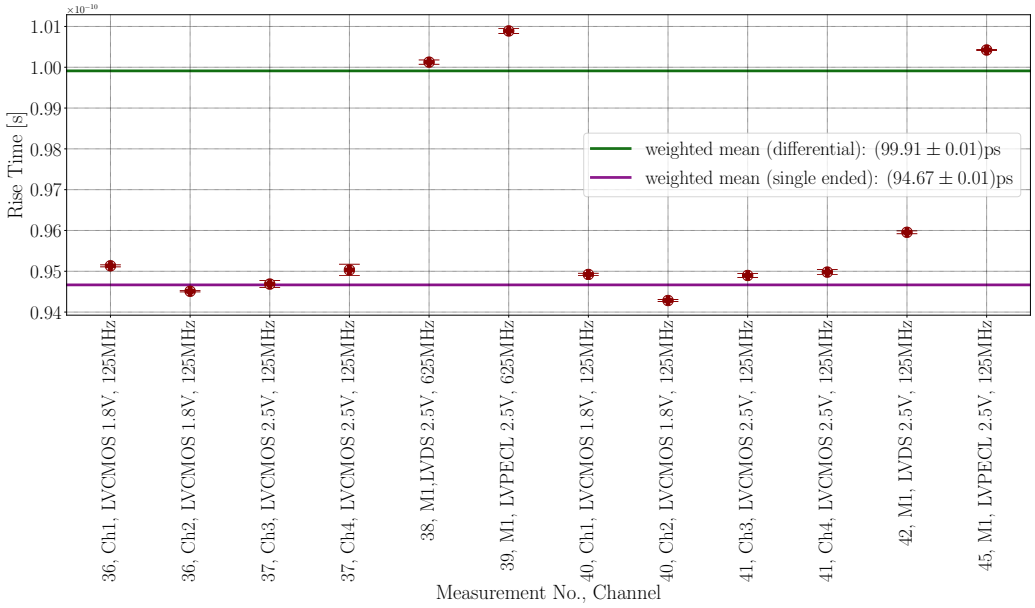


Figure 8.13: CTB rise time performance.

In tab. 8.2 the weighted mean rise time measurement results for the three DUTs are shown. While the Si5338 DB does not meet the 100 ps rise time goal set for Mu3e, both the Si5344 EVB and the CTB achieve lower rise time values with CTB beating the Si5344 EVB.

DUT	Rise Time differential [ps]	Rise Time single ended [ps]
Si5338 DB	113.97 ± 0.00	98.75 ± 0.01
Si5344 EVB	98.80 ± 0.05	95.84 ± 0.01
CTB	99.91 ± 0.01	94.67 ± 0.01

Table 8.2: The weighted mean rise time and error of rise time for each DUT for single ended and differential signals.

8.3.3 Phase Stability

Finally, the phase stability of the output signals was measured. Therefore, the relative phase of two identical single ended output signals coming from the same DUT or the two links of a differential signal were compared. Consequently, the relative phase of two single ended signals is close to zero, while the relative phase of two links of a differential signal are shifted by π. To determine the phase stability of the signal over a certain time, 2000 samples were taken for each measurement and eqn. 8.2 was applied as in sec. 8.3.1. Exemplary phase histograms are shown in Appendix Part F. The results are shown in fig. 8.14 in case of the Si5338 DB as DUT, in fig. 8.15 in case of the Si5344 EVB as DUT and in fig. 8.16 in case of the CTB as DUT. In the case of the CTB, the phase was proven to be stable with the relative phase never deviating more than 10% from it's ideal value over 2000 samples.

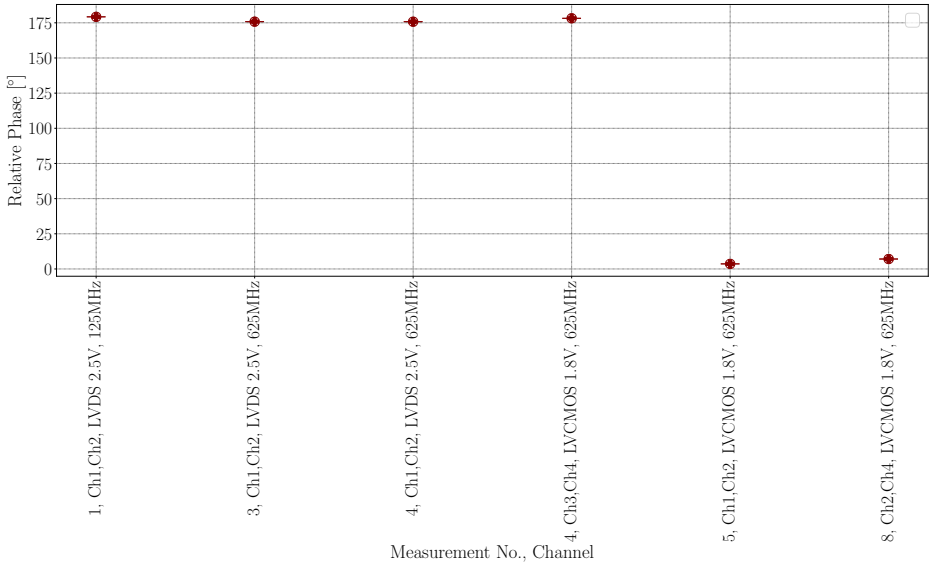


Figure 8.14: Si5338 DB phase performance.

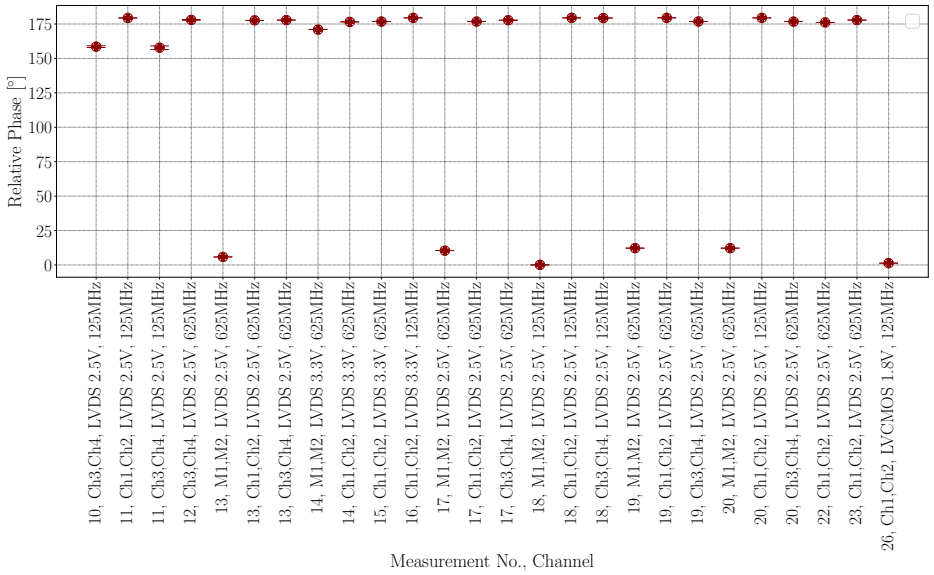


Figure 8.15: Si5344 EVB phase performance.

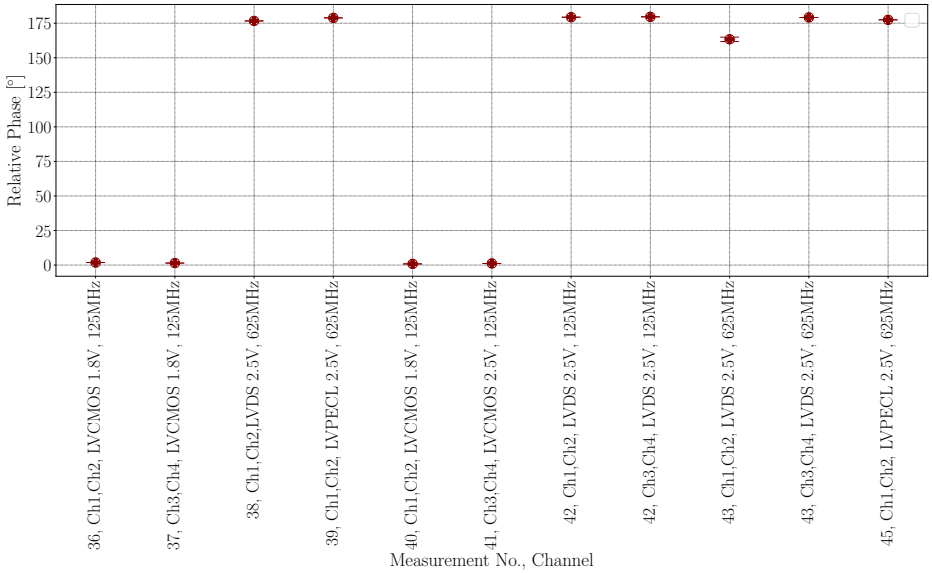


Figure 8.16: CTB phase performance.

8.4 Further Analysis of the CTB Signal Transmission Quality

To further characterise the CTB's performance for transmitting signals, an eye diagram was generated shown in fig. 8.17. On the x-axis the time and on the y-axis the signal voltage level are shown. Very steep rising and falling edges indicate a bit period of 4 ns for nearly every voltage of the signal, corresponding to the signal frequency of 125 MHz. Very low jitter and short rise time are observable. Also the eye height is in agreement with industry standards [26], never dipping below a 400 mV amplitude. Furthermore, the influence of pre-emphasis done by the Si5344 on the CTB are visible, indicated by the step in the high and low levels of the signal.

Also, a frequency spectrum for the CTB output signal was conducted shown in fig. 8.18. On the x-axis the frequency is shown, in units of 312.5 MHz. On the y-axis the signal intensity is shown, in units of 20 dB. Accordingly, the strongest and leftmost peak represents the signal frequency of 125 MHz. Then, the harmonics can be seen. Their intensity decreases with rising frequency. Signal noise however never reaches a level of more than 10% to the absolute signal intensity.

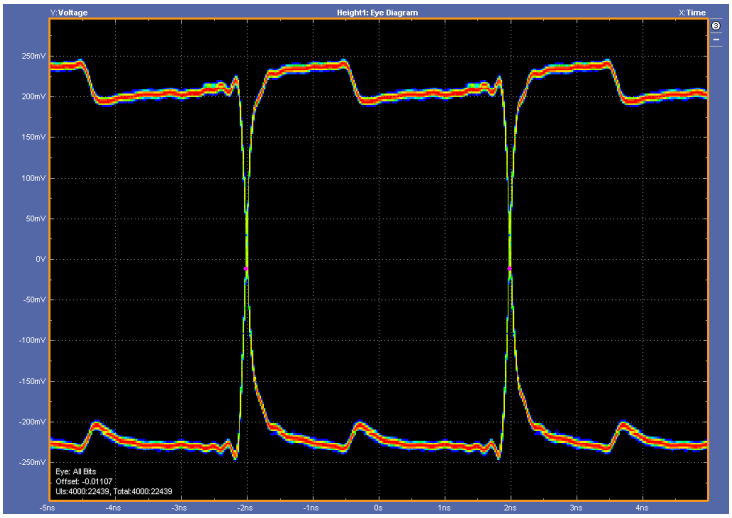


Figure 8.17: Eye diagram for measurement 44. Here, a 125 MHz optical input signal was locked onto an LVDS 2.5 V output signal by the CTB with 125 MHz.

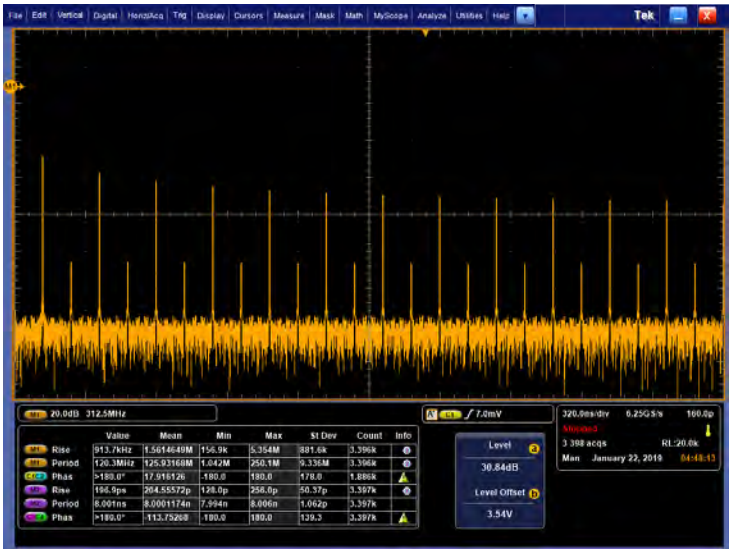


Figure 8.18: Frequency spectrum for measurement 44. Here, a 125 MHz optical input signal was locked onto an LVDS 2.5 V output signal by the CTB with 125 MHz.

Chapter 9

Outlook and Conclusion

The readout system of the Mu3e experiment need by be synchronised with a global clock signal. This signal is distributed with multimode optical fibres. To convert this optical clock signal into an electric one and to improve the signals quality for the filter farm PCs the Clock Transmission Board was designed, built and tested during this thesis.

9.1 Clock Transmission Board Design

First the schematic of the CTB was designed using the Eagle Autodesk Software. Based around the Si5344, electrical input and output channels together with termination and coupling circuits were planned, an optical transceiver integrated, power supply circuits calculated and a SPI control interface realised. Various components had to be integrated into the software's catalog. Next, the components were placed on the PCB. The placement followed to requirements set by the installation of the CTB inside a filter farm PC's case. Also, a six-layer setup for the PCB was calculated to improve fast signal characteristics. After the design phase the manufacturing process of the CTB was coordinated with Contag.

The following requirements set for the CTB by the Mu3e readout system were achieved:

- Fits into PCIe graphic card slot
- USB 3.0, wire port and SMA power supply

- Compatible with both SFP+ and SMA connectors
- Compatible with both differential and single ended signals
- Compatible with $3.3V$, $2.5V$ (Arria V) and $1.8V$ (Arria 10) signals
- Two different output voltages at the same time
- All outputs AC coupled
- Transmission of clock signals with jitter of $\mathcal{O}(100\,\mathrm{fs})$, rise time of $\mathcal{O}(100\,\mathrm{ps})$ and a high phase stability
- Internal oscillator for reference clock
- Si 5344 10 channel, any-frequency, any output, jitter attenuator, clock multiplier
- SPI programmable

9.2 Clock Transmission Board Programming

In the next step the Si5344 on the CTB was programmed. For this a SPI interface was used. As SPI master an Arria 10 FPGA development board was used.

9.3 Clock Transmission Signal Characteristics

In the final part of this thesis the signal processing performance of the CTB was determined. Therefore, various signal combinations were used. For each configuration, jitter, rise time and phase stability measurements were made. As a measurement standard the JEDEC standard JESD65B was chosen. Accordingly, for each measurement 2000 samples were taken. The data was then binned correspondingly to the oscilloscopes time resolution, histogrammed and the root mean square of the distribution determined. The resulting measurement values are shown in tab. 9.1, where also reference measurements with the SI5338 development kit board and Si5344 evaluation board were included.

DUT	Jitter differential [fs]	Jitter single ended [fs]
Si5338 DB	656.13 ± 1.48	542.64 ± 1.36
Si5344 EVB	292.18 ± 0.34	403.41 ± 0.93
CTB	310.61 ± 1.14	418.49 ± 1.02
DUT	Rise Time differential [ps]	Rise Time single ended [ps]
Si5338 DB	113.97 ± 0.00	98.75 ± 0.01
Si5344 EVB	98.80 ± 0.05	95.84 ± 0.01
CTB	99.91 ± 0.01	94.67 ± 0.01

Table 9.1: Measurement results for jitter and rise time for all DUTs and both single ended and differential signals.

It can be concluded that the CTB's signal processing performance satisfies the requirements for the Mu3e readout system.

9.4 Outlook

Beyond the scope of this thesis the following ideas are worth exploring.

- Simplifying the CTB's user experience by adding assembly print and component names and values on the CTB PCB
- Manufacturing of a PCIe slot facia plate for the CTB
- Manufacturing of a dedicated connector cable for the SPI interface between the CTB and the Arria 10 FPGA
- Testing of further signal configurations, including using the CTB as an optical clock transmitter
- Integration of the CTB into a full scale Mu3e readout system mockup with the clock signal generated by the Mu3e clock generation board and a filter farm FPGA as the clock receiver
- Improving the CTB form factor by using a more efficient PCB layout

Acknowledgements

First of all I wish to thank Prof. Dr. Niklaus Berger for supervising this thesis and giving me the opportunity to work on interesting physics together with a great group of people. Furthermore, I would like to give my sincere thanks to Prof. Dr. Kurt Aulenbacher for agreeing to be the second supervisor of this thesis.
A very warm thank you also goes to everyone part of the AG Berger, but especially to Dr. Alexandr Kozlinskiy, Dr. Frederik Wauters, Marco Zimmermann, Martin Müller and Marius Köppel answering all my questions and providing exceptional support for this thesis.
During the conception phase of the CTB the knowledge and expertise in electronics and PCB design of Dr. Andrea Brogna, Eyüp Atila Kurt (Prisma Detector Lab) and Igor Beltschikow (Institute of Nuclear Physics Electronics Lab) proved invaluable.
Finally, I would like to thank my parents and my girlfriend Anne Galda for giving me support and strength not only, but especially during the time of this thesis.

$\alpha\tau$

Declaration of Authorship

"I herewith declare that I have composed the present thesis myself and without use of any other than the cited sources and aids. Sentences or parts of sentences quoted literally are marked as such; other references with regard to the statement and scope are indicated by full details of the publications concerned. The thesis in the same or similar form has not been submitted to any examination body and has not been published. This thesis was not yet, even in part, used in another examination or as a course performance."

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Appendix

A CTB Schematic

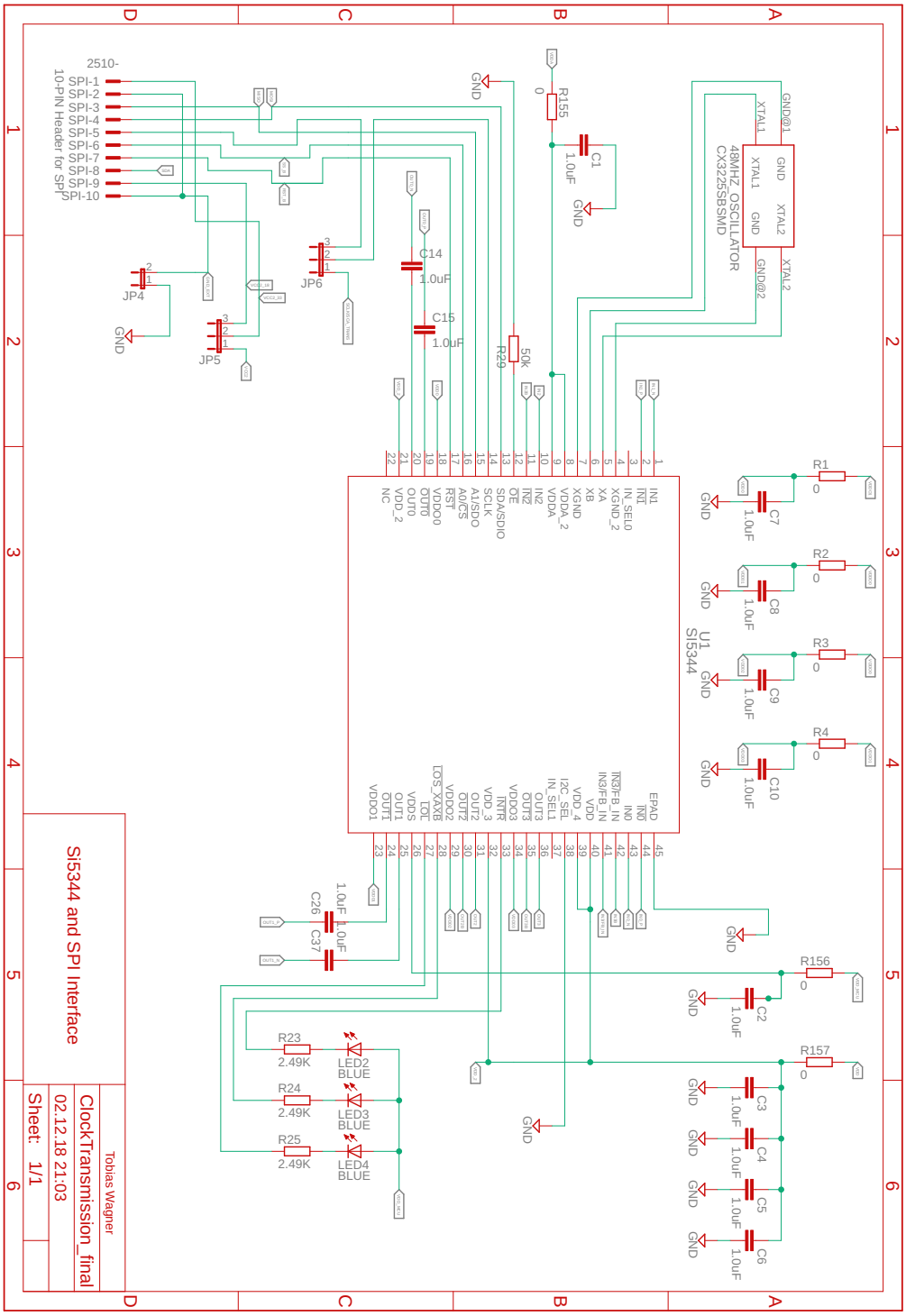

Figure 1: CTB schematic page 1.

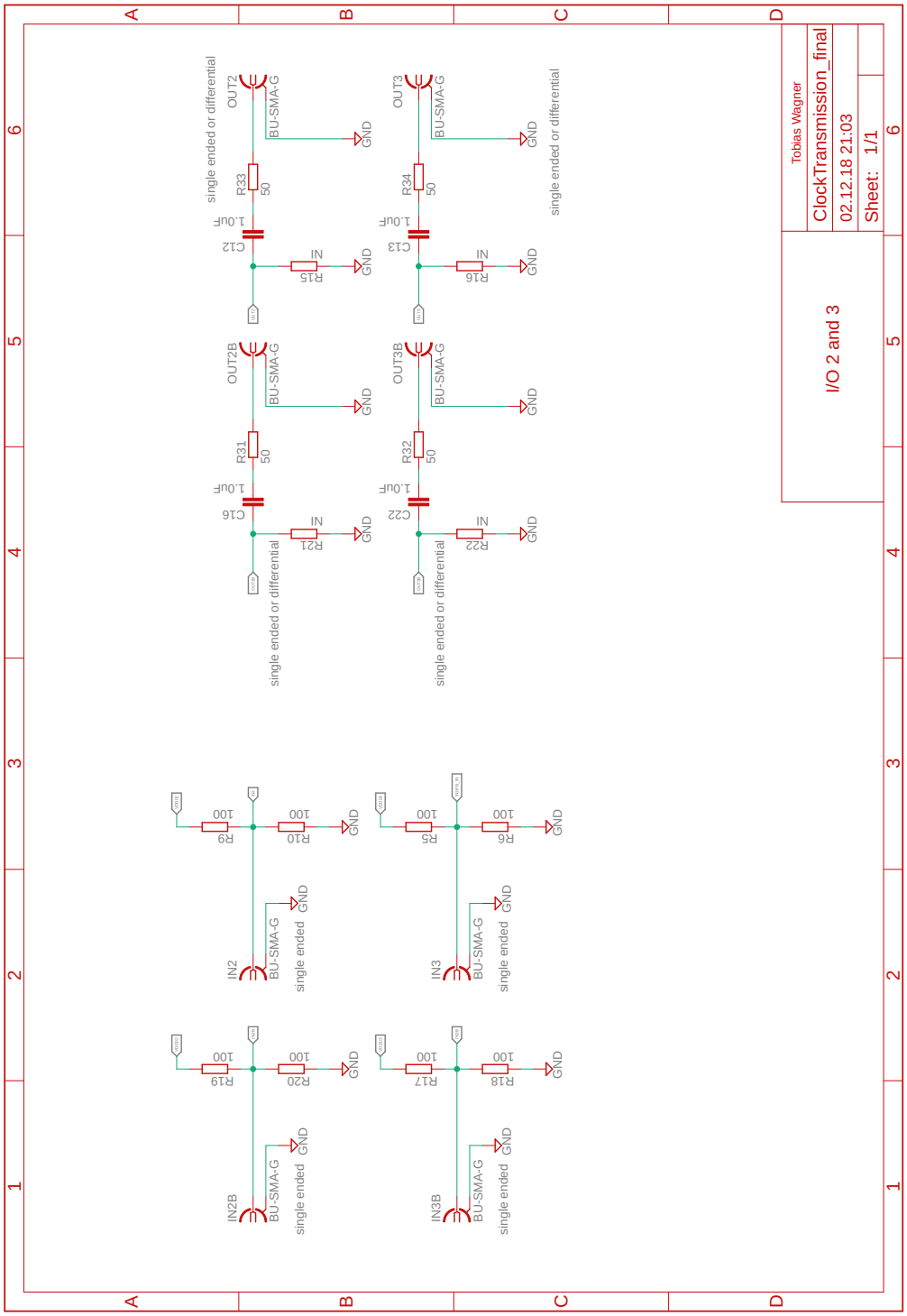

Figure 2: CTB schematic page 2.

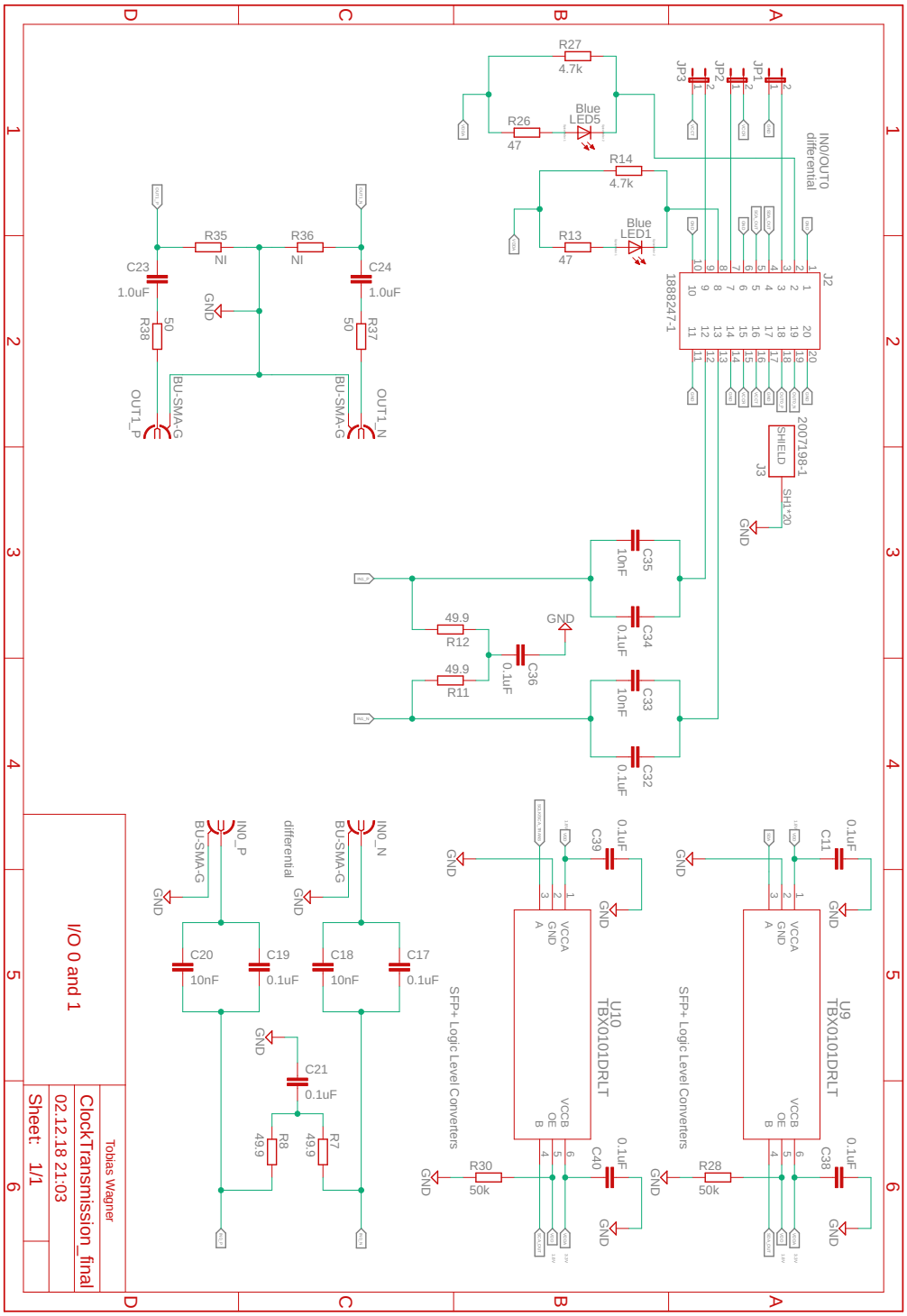

Figure 3: CTB schematic page 3.

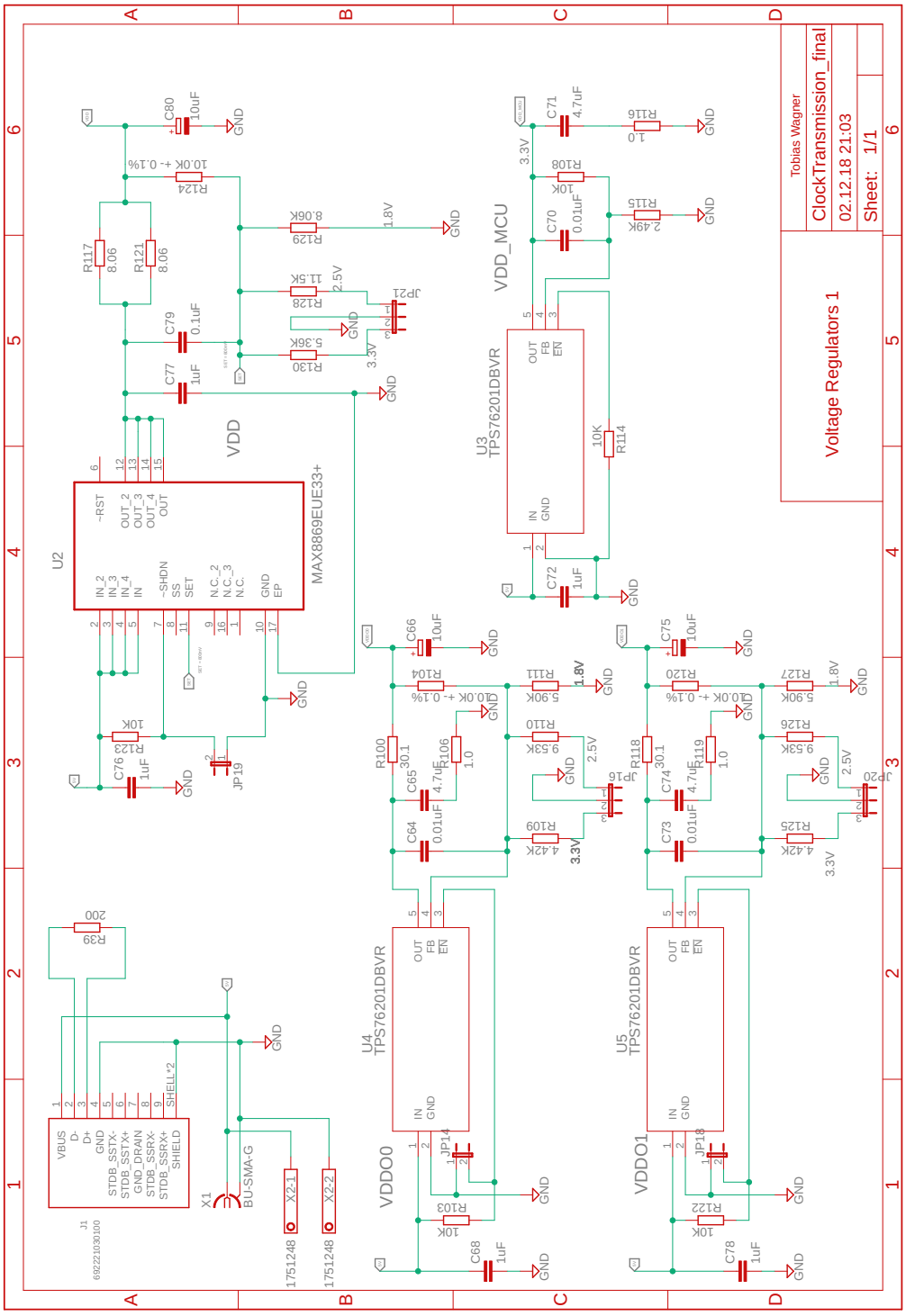

Figure 4: CTB schematic page 4.

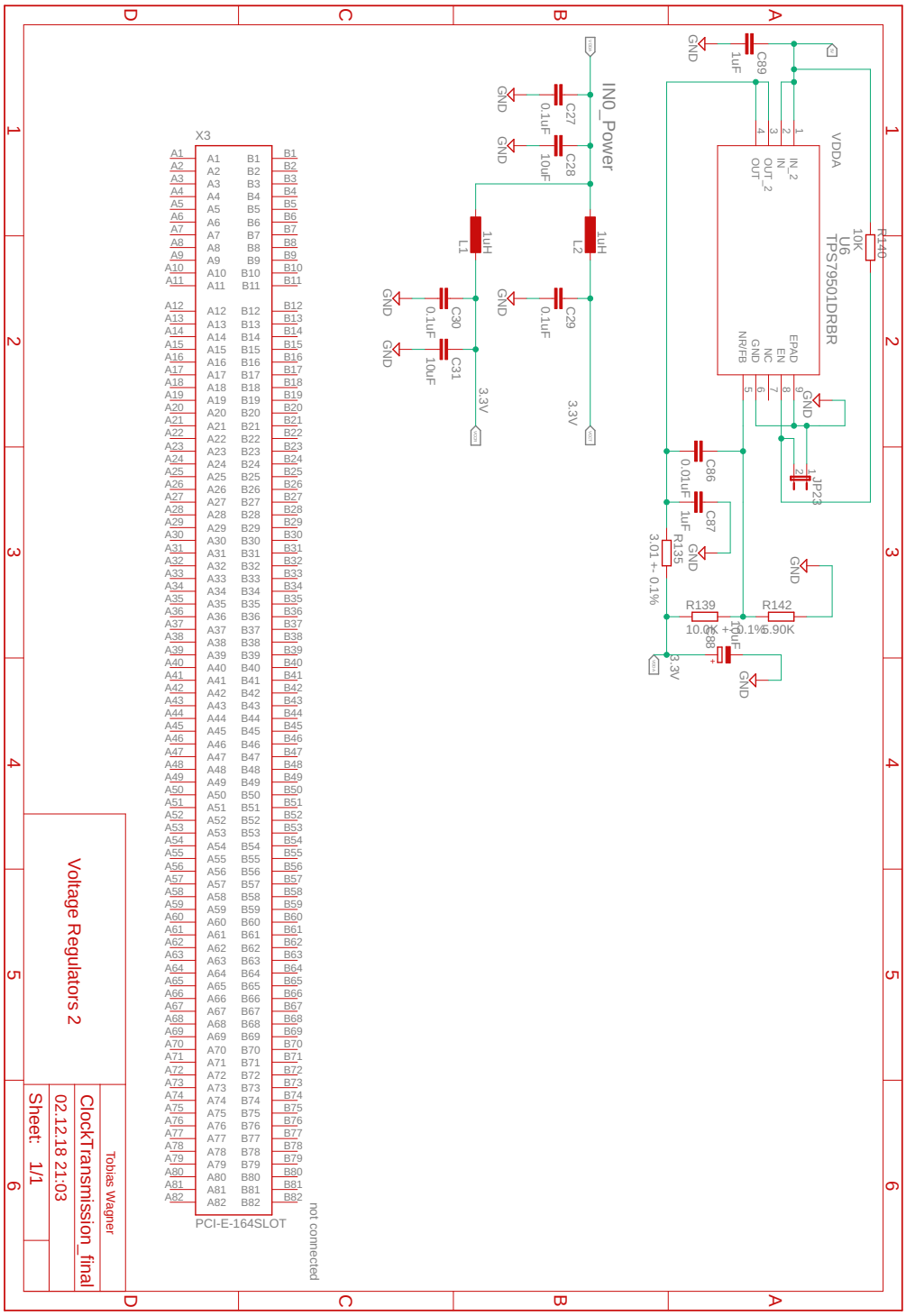

Figure 5: CTB schematic page 5.

B CTB Layers

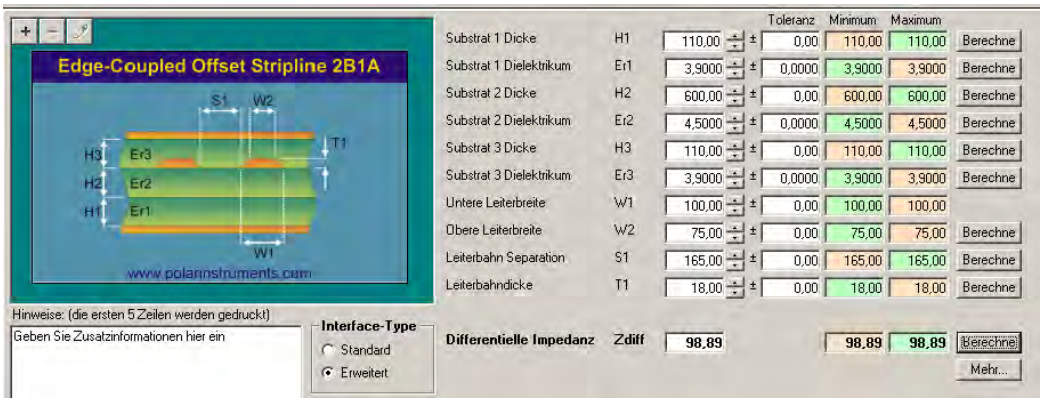

Figure 6: CTB PCB layer construction top half.

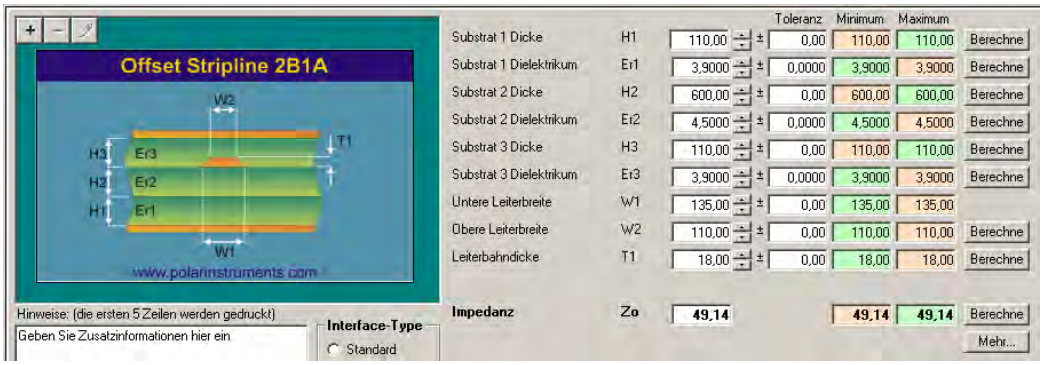

Figure 7: CTB PCB layer construction bottom half.

C CTB Layout

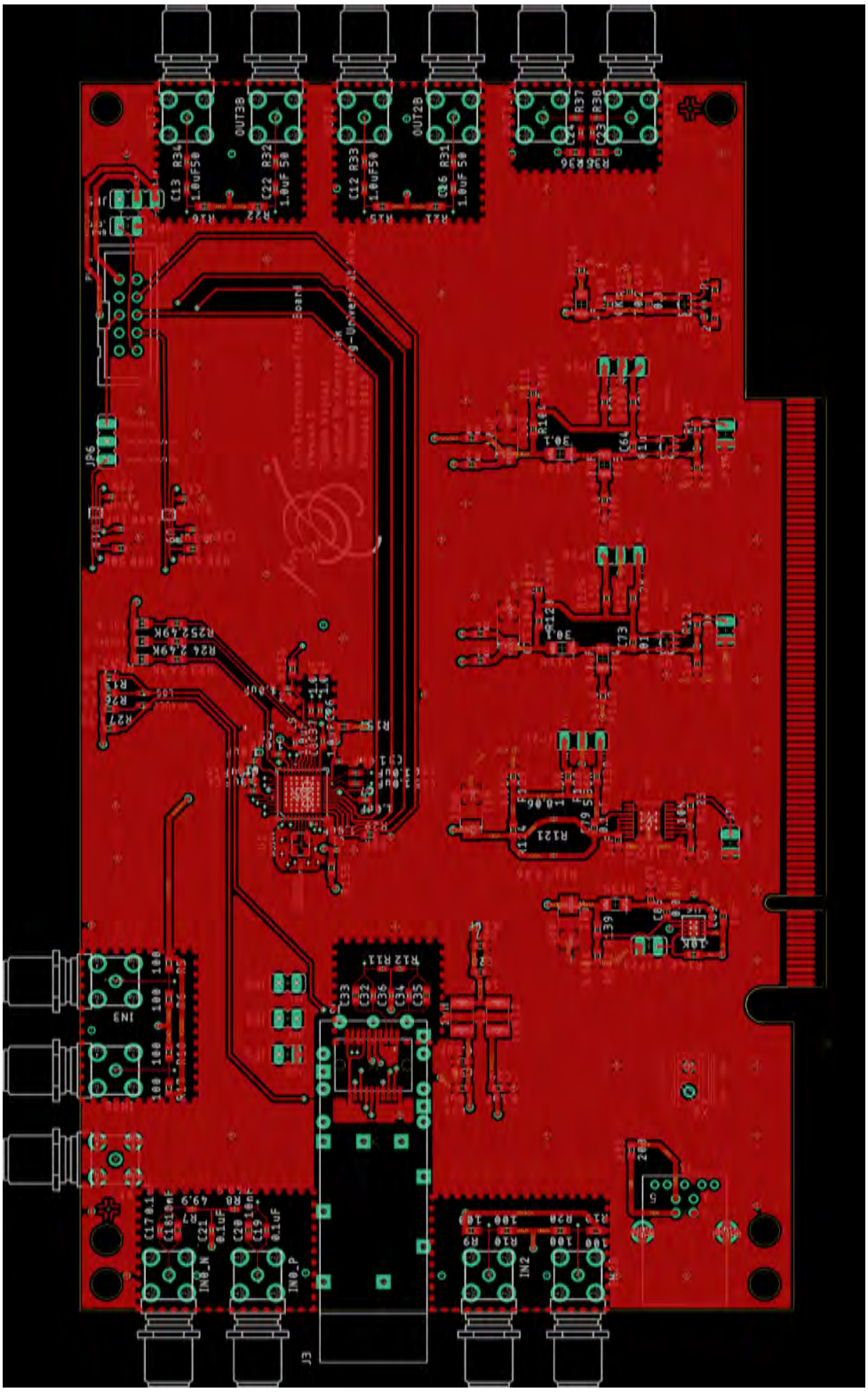

Figure 8: CTB layout layer 1.

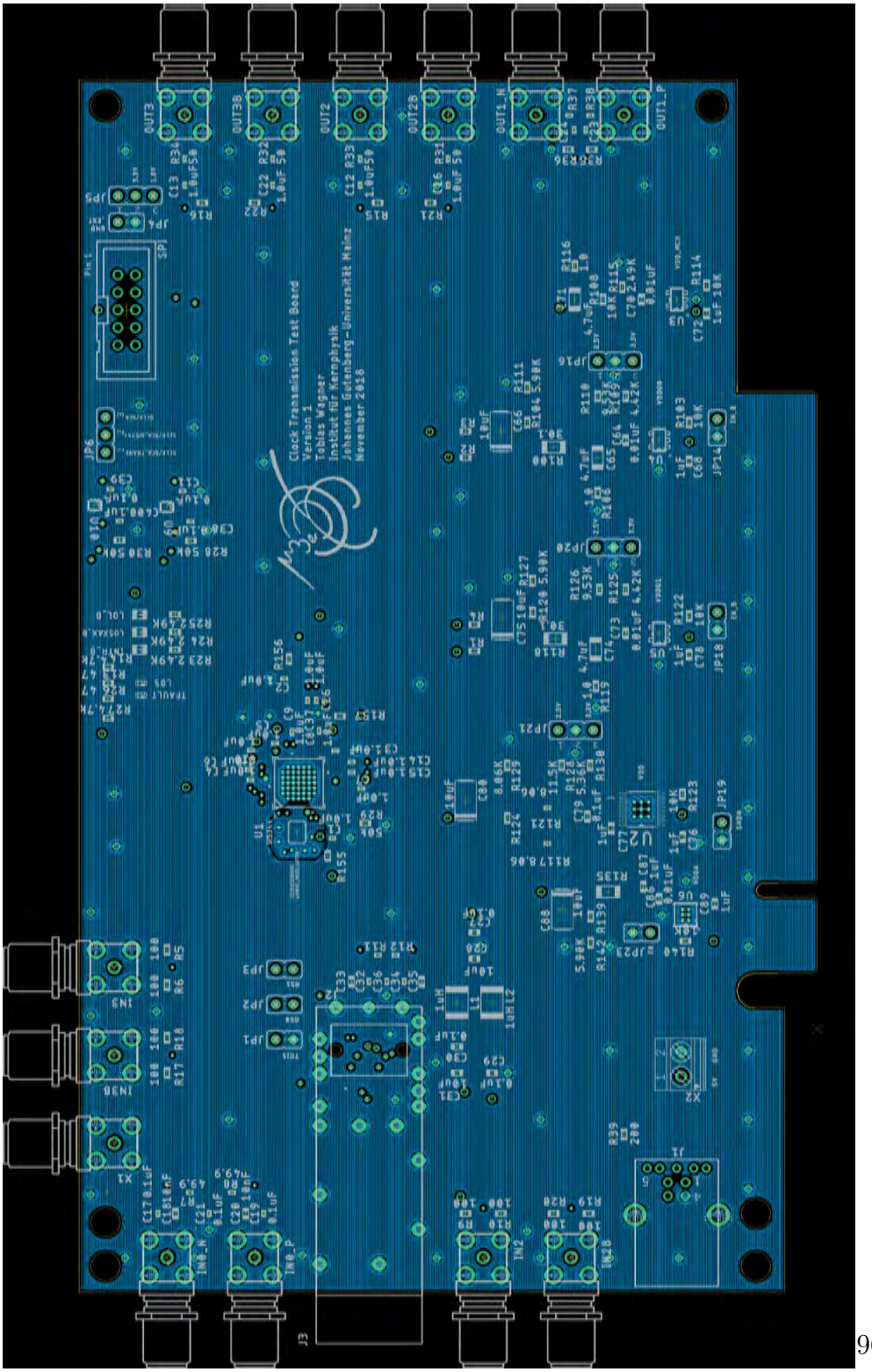

Figure 9: CTB layout layer 2.

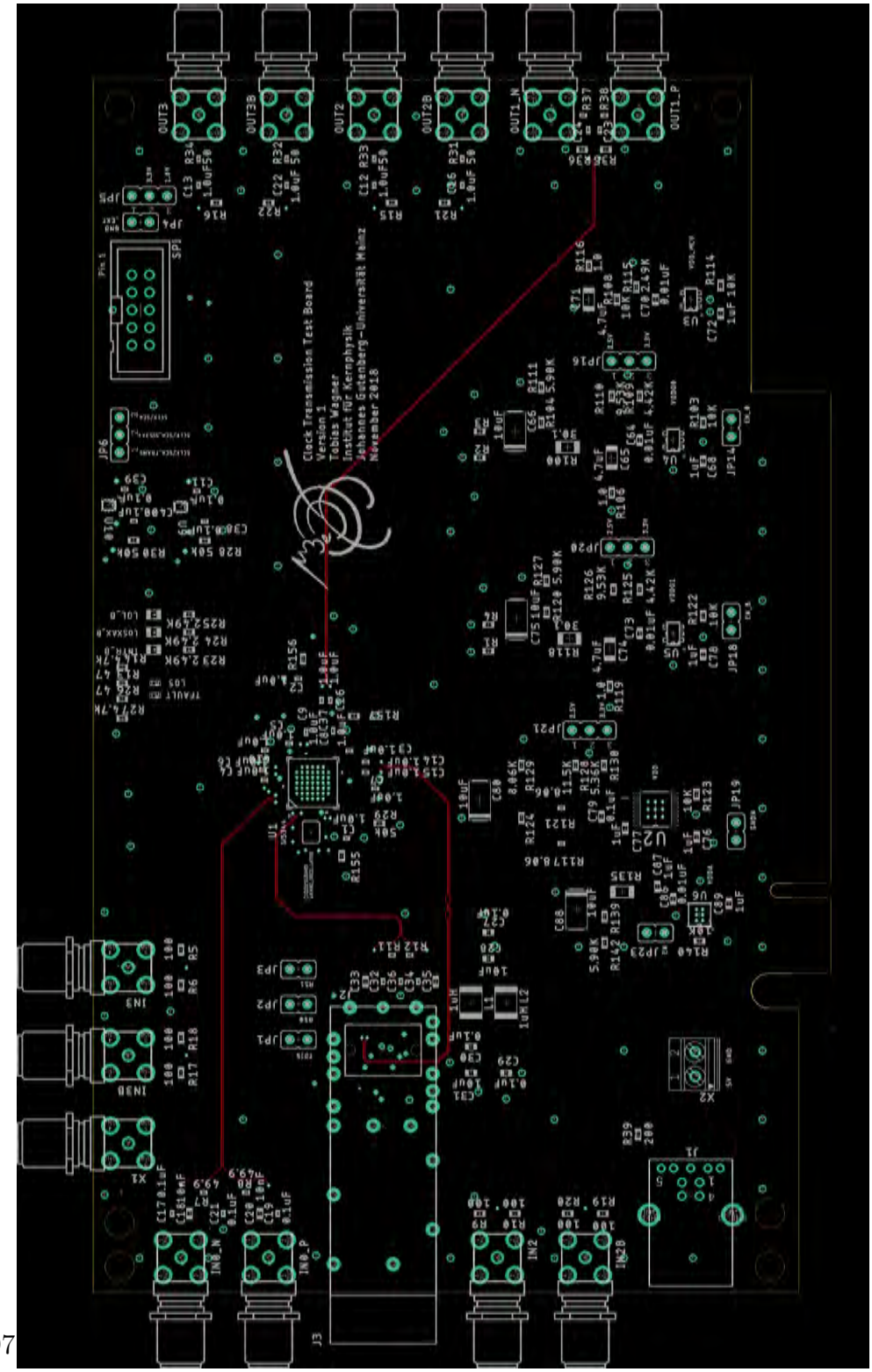

Figure 10: CTB layout layer 3.

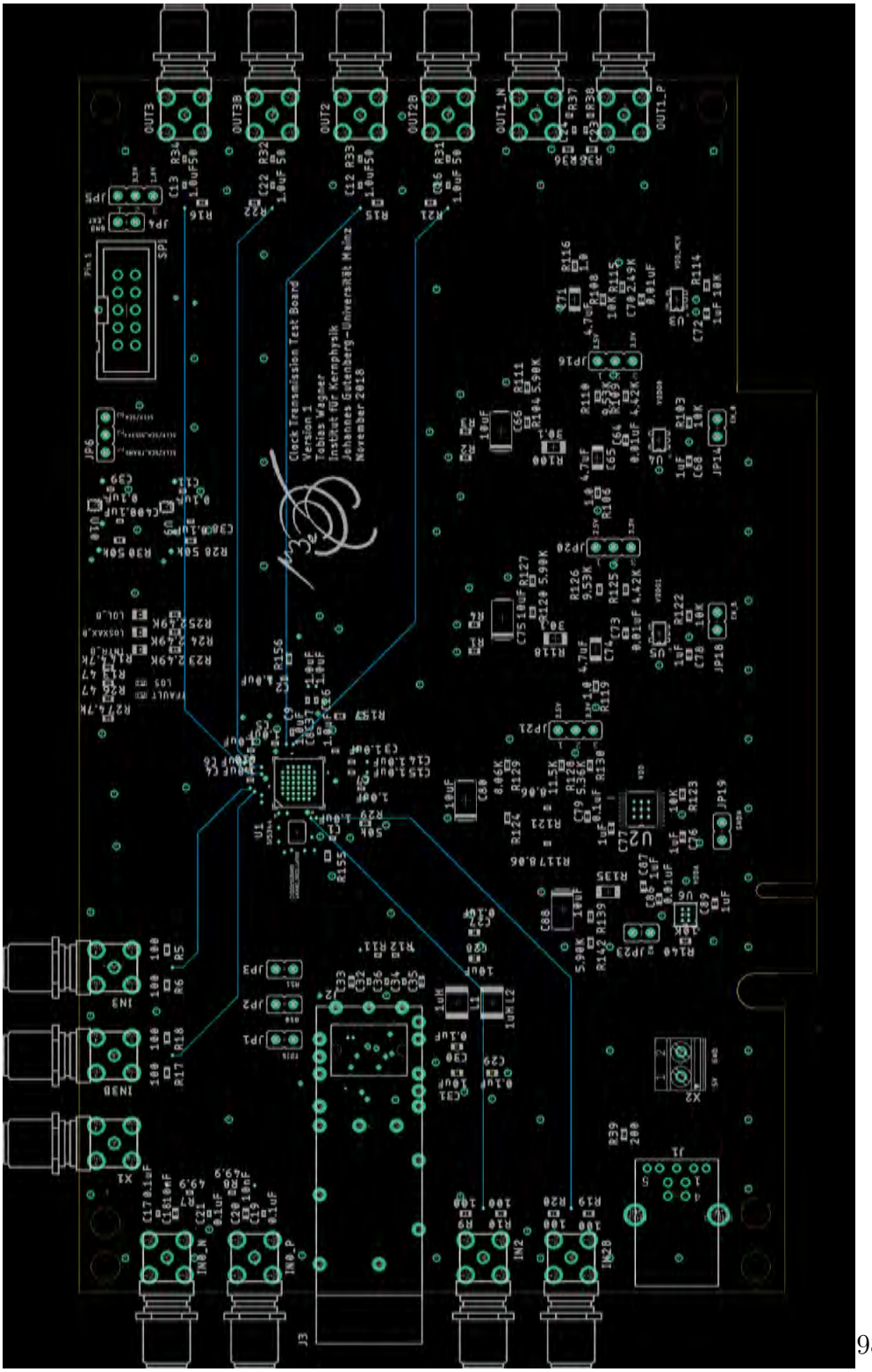

Figure 11: CTB layout layer 4.

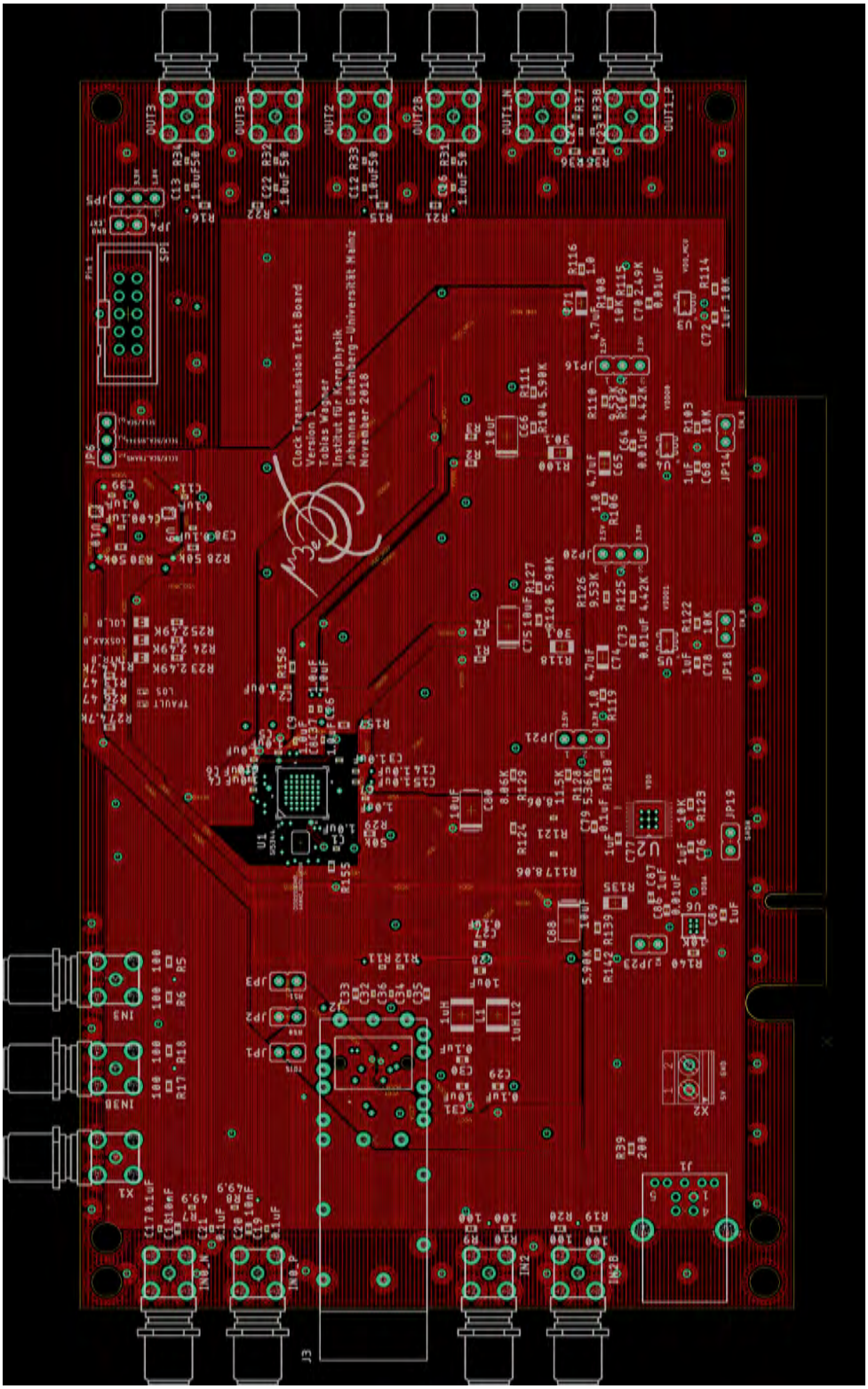

Figure 12: CTB layout layer 5.

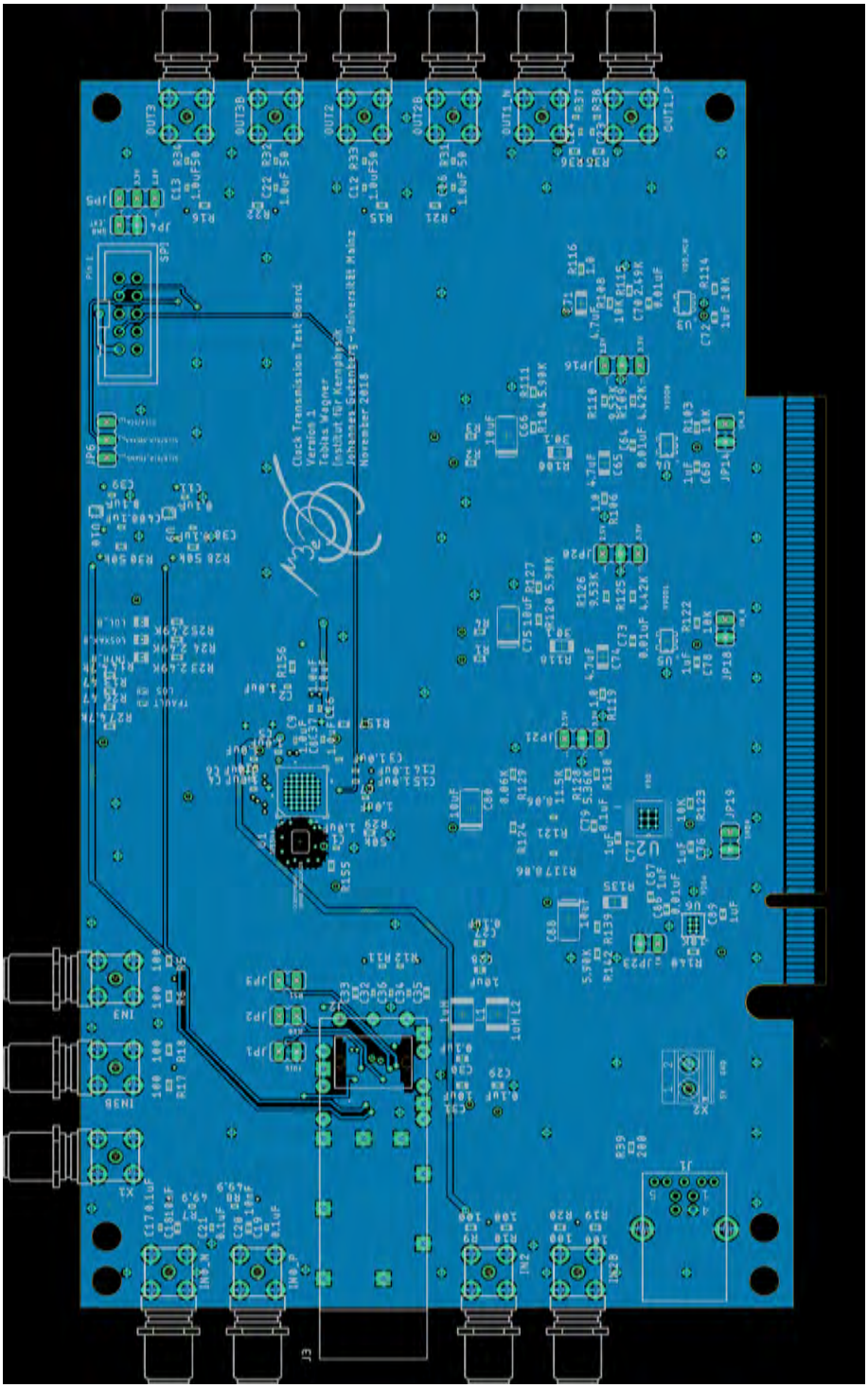

Figure 13: CTB layout layer 6.

D CTB Partslist/BOM

1	**49MHZ_OSCILLATO**	CX3225SBSMD					CX3225SBSMD	CX3225SB	Kyocera CX3225SB
2	**C1**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
3	**C2**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
4	**C3**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
5	**C4**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
6	**C5**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
7	**C6**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
8	**C7**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
9	**C8**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
10	**C9**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
11	**C10**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
12	**C11**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
13	**C12**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
14	**C13**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
15	**C14**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
16	**C15**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
17	**C16**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
18	**C17**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
19	**C18**	10nF		6.3V	+-10%	X5R	C-EUC0603	C0603	CAPACITOR, European symbol
20	**C19**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
21	**C20**	10nF		6.3V	+-10%	X5R	C-EUC0603	C0603	CAPACITOR, European symbol
22	**C21**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
23	**C22**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
24	**C23**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
25	**C24**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
26	**C26**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
27	**C27**	0.1uF		16V	+-20%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
28	**C28**	10uF		6.3V	+-20%	X5R	C-EUC0603	C0603	CAPACITOR, European symbol
29	**C29**	0.1uF		16V	+-20%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
30	**C30**	0.1uF		16V	+-20%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
31	**C31**	10uF		6.3V	+-20%	X5R	C-EUC0603	C0603	CAPACITOR, European symbol
32	**C32**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
33	**C33**	10nF		6.3V	+-10%	X5R	C-EUC0603	C0603	CAPACITOR, European symbol
34	**C34**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
35	**C35**	10nF		6.3V	+-10%	X5R	C-EUC0603	C0603	CAPACITOR, European symbol
36	**C36**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
37	**C37**	1.0uF		6.3V	+-10%	X5R	C-EUC0402	C0402	CAPACITOR, European symbol
38	**C38**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
39	**C39**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
40	**C40**	0.1uF		10V	+-10%	X7R	C-EUC0402	C0402	CAPACITOR, European symbol
41	**C64**	0.01uF		16V	+-20%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
42	**C65**	4.7uF		10V	+-20%	X7R	C-EUC1206	C1206	CAPACITOR, European symbol
43	**C66**	10uF		25V	+-20%	TANT	CPOL-EUC/6032-28	C/6032-28R	POLARIZED CAPACITOR, European symbol
44	**C68**	1uF		16V	+-10%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
45	**C70**	0.01uF		16V	+-20%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
46	**C71**	4.7uF		10V	+-10%	X7R	C-EUC1206	C1206	CAPACITOR, European symbol
47	**C72**	1uF		16V	+-10%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
48	**C73**	0.01uF		16V	+-20%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
49	**C74**	4.7uF		10V	+-20%	X7R	C-EUC1206	C1206	CAPACITOR, European symbol
50	**C75**	10uF		25V	+-20%	TANT	CPOL-EUC/6032-28	C/6032-28R	POLARIZED CAPACITOR, European symbol
51	**C76**	1uF		16V	+-10%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
52	**C77**	1uF		16V	+-10%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
53	**C78**	1uF		16V	+-10%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
54	**C79**	0.1uF		16V	+-20%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
55	**C80**	10uF		25V	+-20%	TANT	CPOL-EUC/6032-28	C/6032-28R	POLARIZED CAPACITOR, European symbol
56	**C86**	0.01uF		16V	+-20%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
57	**C87**	1uF		16V	+-10%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
58	**C88**	10uF		25V	+-20%	TANT	CPOL-EUC/6032-28	C/6032-28R	POLARIZED CAPACITOR, European symbol
59	**C89**	1uF		16V	+-10%	X7R	C-EUC0603	C0603	CAPACITOR, European symbol
60	**IN0_N**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
61	**IN0_P**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
62	**IN2**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
63	**IN2B**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
64	**IN3**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
65	**IN3B**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
66	**J1**	692221030100					692221030100	692221030100	WR-COM USB 3.0 HORIZONTAL TYPE B=>Code :Con_I-O_COM_USB-3.0_B_692221030100	
67	**J2**	1888247-1					1888247-1	TE_1888247-1	20 Position 0.8 mm Pitch Double Sided Right Angle Receptacle SFP Connector	
68	**J3**	2007198-1					2007198-1	TE_2007198-1	Connector Accessories SFP+ Cage Right Angle Silver Nickel Tray	
69	**JP1**					2 port	JP1E	JP1	JUMPER	Stiftleiste Standard
70	**JP2**					2 port	JP1E	JP1	JUMPER	Stiftleiste Standard
71	**JP3**					2 port	JP1E	JP1	JUMPER	Stiftleiste Standard
72	**JP4**					2 port	JP1E	JP1	JUMPER	Stiftleiste Standard
73	**JP5**					3 port	JP2E	JP2	JUMPER	Stiftleiste Standard
74	**JP6**					3 port	JP2E	JP2	JUMPER	Stiftleiste Standard
75	**JP14**					2 port	JP1E	JP1	JUMPER	Stiftleiste Standard
76	**JP16**					3 port	JP2E	JP2	JUMPER	Stiftleiste Standard
77	**JP18**					2 port	JP1E	JP1	JUMPER	Stiftleiste Standard
78	**JP19**					2 port	JP1E	JP1	JUMPER	Stiftleiste Standard
79	**JP20**					3 port	JP2E	JP2	JUMPER	Stiftleiste Standard
80	**JP21**					3 port	JP2E	JP2	JUMPER	Stiftleiste Standard
81	**JP23**					2 port	JP1E	JP1	JUMPER	Stiftleiste Standard
82	**L1**	1uH					L-EUL1812	L1812	INDUCTOR, European symbol	
83	**L2**	1uH					L-EUL1812	L1812	INDUCTOR, European symbol	
84	**LED1**	Blue					LED_ESML0603	LED_SML0603	IN-S63AS5B	nicht lieferbar, LED Standard, blau 0603
85	**LED2**	Blue					LEDCHIP-LED0805	CHIP-LED0805	Avago Technologies HSMR-C170	
86	**LED3**	Blue					LEDCHIP-LED0805	CHIP-LED0805	Avago Technologies HSMR-C170	
87	**LED4**	Blue					LEDCHIP-LED0805	CHIP-LED0805	Avago Technologies HSMR-C170	
88	**LED5**	Blue					LED_ESML0603	LED_SML0603	IN-S63AS5B	nicht lieferbar, LED Standard, blau 0603
89	**OUT1_N**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
90	**OUT1_P**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
91	**OUT2**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
92	**OUT2B**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
93	**OUT3**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
94	**OUT3B**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
95	**R1**	0	1A			Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	0R Standard zB RC0402FR-070RL
96	**R2**	0	1A			Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	0R Standard zB RC0402FR-070RL
97	**R3**	0	1A			Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	0R Standard zB RC0402FR-070RL
98	**R4**	0	1A			Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	0R Standard zB RC0402FR-070RL
99	**R5**	10Ω	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
100	**R6**	10Ω	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
101	**R7**	49_9	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	
102	**R8**	49_9	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	
103	**R9**	10Ω	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
104	**R10**	10Ω	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
105	**R11**	49_9	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	

Figure 14: CTB BOM page 1.

106	**R12**	49_9	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	
107	**R13**	47	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
108	**R14**	4.7k	1/5W		+-0.5%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
109	**R15**	Nil					R-EU_R0603	R0603	RESISTOR, European symbol	nicht bestückt
110	**R16**	Nil					R-EU_R0603	R0603	RESISTOR, European symbol	nicht bestückt
111	**R17**	100	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
112	**R18**	100	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
113	**R19**	100	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
114	**R20**	100	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
115	**R21**	Nil					R-EU_R0603	R0603	RESISTOR, European symbol	nicht bestückt
116	**R22**	Nil					R-EU_R0603	R0603	RESISTOR, European symbol	nicht bestückt
117	**R23**	2.49K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
118	**R24**	2.49K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
119	**R25**	2.49K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
120	**R26**	47	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
121	**R27**	4.7k	1/5W		+-0.5%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
122	**R28**	50k	150mW		+-0.1%	+-25PPM	R-EU_R0603	R0603	RESISTOR, European symbol	auch 49k9
123	**R29**	50k	150mW		+-0.1%	+-25PPM	R-EU_R0603	R0603	RESISTOR, European symbol	auch 49k9
124	**R30**	50k	150mW		+-0.1%	+-25PPM	R-EU_R0603	R0603	RESISTOR, European symbol	auch 49k9
125	**R31**	50	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	auch 49r9
126	**R32**	50	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	auch 49r9
127	**R33**	50	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	auch 49r9
128	**R34**	50	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	auch 49r9
129	**R35**	Nil					R-EU_R0603	R0603	RESISTOR, European symbol	nicht bestückt
130	**R36**	Nil					R-EU_R0603	R0603	RESISTOR, European symbol	nicht bestückt
131	**R37**	50	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	auch 49r9
132	**R38**	50	1/16W		+-1%	Thick Film	R-EU_R0402	R0402	RESISTOR, European symbol	auch 49r9
133	**R39**	200	150mW		+-0.1%	+-25PPM	R-EU_R0603	R0603	RESISTOR, European symbol	
134	**R100**	30.1	1/4W		+-0.1%	+-25PPM	R-EU_R1206	R1206	RESISTOR, European symbol	
135	**R103**	10K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
136	**R104**	10.0K +- 0.1%	1/10W		+-0.1%	+-25PPM	R-EU_R0603	R0603	RESISTOR, European symbol	
137	**R106**	1.0	1/10W		+-0.1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	0,1% nicht lieferbar, auch 1%
138	**R108**	10K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
139	**R109**	4.42K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
140	**R110**	9.53K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
141	**R111**	5.90K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
142	**R114**	10K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
143	**R115**	2.49K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
144	**R116**	1.0	1/10W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
145	**R117**	8.06	1/10W		+-1%	+-100PPM	R-EU_R0402	R0402	RESISTOR, European symbol	
146	**R118**	30.1	1/4W		+-0.1%	+-25PPM	R-EU_R1206	R1206	RESISTOR, European symbol	
147	**R119**	1.0	1/10W		+-0.1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	0,1% nicht lieferbar, auch 1%
148	**R120**	10.0K +- 0.1%	1/10W		+-0.1%	+-25PPM	R-EU_R0603	R0603	RESISTOR, European symbol	
149	**R121**	8.06	1/10W		+-1%	+-100PPM	R-EU_R0402	R0402	RESISTOR, European symbol	
150	**R122**	10K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
151	**R123**	10K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
152	**R124**	10.0K +- 0.1%	1/10W		+-0.1%	+-25PPM	R-EU_R0603	R0603	RESISTOR, European symbol	
153	**R125**	4.42K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
154	**R126**	9.53K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
155	**R127**	5.90K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
156	**R128**	11.5K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
157	**R129**	8.06K	1/2W		+-0.1%	+-50PPM	R-EU_R0603	R0603	RESISTOR, European symbol	
158	**R130**	5.36K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
159	**R135**	3.01 +- 1%	1/3W		+-1%	+-100PPM	R-EU_R1206	R1206	RESISTOR, European symbol	
160	**R139**	10.0K +- 0.1%	1/10W		+-0.1%	+-25PPM	R-EU_R0603	R0603	RESISTOR, European symbol	
161	**R140**	10K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
162	**R142**	5.90K	1/16W		+-1%	Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	
163	**R155**	0	1A			Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	0R Standard zB RC0402FR-070RL
164	**R156**	0	1A			Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	0R Standard zB RC0402FR-070RL
165	**R157**	0	1A			Thick Film	R-EU_R0603	R0603	RESISTOR, European symbol	0R Standard zB RC0402FR-070RL
166	**SPI**	2510					2510-	PAK100/2500-10		Wannenstecker Standard, Farnell 9838244
167	**U1**	SI5344					SI5344	QFN_44	3M (TM) Pak 100 4-Well Header, N2510-6002RB + Wire-To-Board Connector, 2.54 r Silicon Laboratories SI5344	SI5344D-D-GM
168	**U2**	MAX8869EUE33+					MAX8869EUE33+	SOP65P640X110	1A, MicroCap, Low-Dropout, Linear Regulator	
169	**U3**	TPS76201DBVR					TPS76201DBVR	DBV5	Texas Instruments TPS76201DBVR	
170	**U4**	TPS76201DBVR					TPS76201DBVR	DBV5	Texas Instruments TPS76201DBVR	
171	**U5**	TPS76201DBVR					TPS76201DBVR	DBV5	Texas Instruments TPS76201DBVR	
172	**U6**	TPS79501DRBR					TPS79501DRBR	DRB8_2P4X1P65	Texas Instruments TPS79501DRBR	
173	**U9**	TXB0101DRLT					TXB0101DRLT	DRL6	Texas Instruments TXB0101DRLT	Bezeichnung gibt es nicht, nicht enthalten
174	**U10**	TXB0101DRLT					TBX0101DRLT	DRL6	Texas Instruments TXB0101DRLT	Bezeichnung gibt es nicht, nicht enthalten
175	**X1**	BU-SMA-G				Solder trough, right angle	BU-SMA-G	BU-SMA-G	FEMALE SMA CONNECTOR	beliebig, z.B. RF2-03E-T-00-50-G
176	**X2**	1751248					1751248	1751248	MKDS 1/ 2-3,5 Printklemme	
177	**X3**	PCI-E-164_SLOT					PCI-E-164_SLOT	PCI-E-164_SLOT	Copy from con-pci_express(pci-e).lbr uploaded Mon Jul 2 10:15:25 2007	kein Bauteil

Figure 15: CTB BOM page 2.

E CTB Power Consumption

During testing of the CTB, the power consumed by the CTB was measured. Tab. 2 shows some typical power values for the operation of the CTB with different signal in- and output configurations.

Power Supply Enabled	Power Consumption @ 5 V [mW]	Commentary
VDD_MCU	10.5	
VDD_MCU, VDDA	21.5	
VDD_MCU, VDD	27.0	
VDD_MCU, VDD, VDDA	134	
VDD_MCU, VDD, VDDA, VDDO1	143	
VDD_MCU, VDD, VDDA, VDDO1, VDDO0	169	
VDD_MCU, VDD, VDDA, VDDO1, VDDO0	223	with optical transceiver

Table 2: The power consumption of the CTB with different power supply netclasses enabled.

F Measurements

No.	DUT	Signal	Frequency	Commentary
1	Si5338	Out: Ch1, Ch2 LVDS 2.5 V	125 MHz	$M1 = Ch1 - Ch2$
2	Si5338	Out: Ch1, Ch2, Ch3, Ch4 LVDS 2.5 V	125 MHz	$M1 = Ch1 - Ch2$, $M2 = Ch3 - Ch4$
3	Si5338	Out: Ch1, Ch2 LVDS 2.5 V	625 MHz	$M1 = Ch1 - Ch2$
4	Si5338	Out: Ch1, Ch2, Ch3, Ch4 LVDS 2.5 V	625 MHz	$M1 = Ch1 - Ch2$, $M2 = Ch3 - Ch4$
5	Si5338	Out: Ch1, Ch2 LVCMOS 1.8 V	625 MHz	
7	Si5338	Out: Ch1, Ch2, Ch3, Ch4 LVCMOS 1.8 V	625 MHz	
8	Si5338	Out: Ch1, Ch2, Ch3, Ch4 LVCMOS 1.8 V	625 MHz	
10	Si5344	In: Ch0 LVDS 2.5 V, Out: Ch3, Ch4 LVDS 2.5 V	125 MHz	$M1 = Ch3 - Ch4$
11	Si5344	In: Ch0 LVDS 2.5 V	125 MHz	
		Out: Ch1, Ch2, Ch3, Ch4 LVDS 2.5 V	125 MHz	$M1 = Ch3 - Ch4$, $M2 = Ch1 - Ch2$
12	Si5344	In: Ch0 LVDS 2.5 V	125 MHz	
		Out: Ch3, Ch4 LVDS 2.5 V	625 MHz	$M1 = Ch3 - Ch4$
13	Si5344	In: Ch0 LVDS 2.5 V	125 MHz	
		Out: Ch1, Ch2, Ch3, Ch4 LVDS 2.5 V	625 MHz	$M1 = Ch3 - Ch4$, $M2 = Ch1 - Ch2$
14	Si5344	In: Ch0 LVDS 3.3 V	625 MHz	
		Out: Ch1, Ch2, Ch3, Ch4 LVDS 3.3 V	625 MHz	$M1 = Ch3 - Ch4$, $M2 = Ch1 - Ch2$
15	Si5344	In: Ch0 LVDS 2.5 V	625 MHz	
		Out: Ch1, Ch2 LVDS 3.3 V	625 MHz	$M2 = Ch1 - Ch2$
16	Si5344	In: Ch0 LVDS 2.5 V	625 MHz	
		Out: Ch1, Ch2 LVDS 3.3 V	125 MHz	$M2 = Ch1 - Ch2$
17	Si5344	In: Ch0 LVDS 2.5 V	625 MHz	
		Out: Ch1, Ch2, Ch3, Ch4 LVDS 2.5 V	625 MHz	$M1 = Ch3 - Ch4$, $M2 = Ch1 - Ch2$
18	Si5344	In: Ch0 LVDS 2.5 V	625 MHz	
		Out: Ch1, Ch2, Ch3, Ch4 LVDS 2.5 V	125 MHz	$M1 = Ch3 - Ch4$, $M2 = Ch1 - Ch2$
19	Si5344	In: Ch0, Ch1 LVDS 2.5 V	125 MHz	
		Out: Ch1, Ch2 LVDS 2.5 V	625 MHz	$M1 = Ch3 - Ch4$
		Out: Ch3, Ch4 LVDS 2.5 V	625 MHz	$M1 = Ch3 - Ch4$
20	Si5344	In: Ch0, Ch1 LVDS 2.5 V	625 MHz	
		Out: Ch1, Ch2 LVDS 2.5 V	125 MHz	$M2 = Ch1 - Ch2$
		Out: Ch3, Ch4 LVDS 2.5 V	625 MHz	$M1 = Ch3 - Ch4$
22	Si5344	In: Ch0, Ch1 LVDS 2.5 V	625 MHz	
		Out: Ch3, Ch4 LVDS 2.5 V	625 MHz	$M1 = Ch3 - Ch4$, bronze SMA cables
23	Si5344	In: Ch0, Ch1 LVDS 2.5 V	625 MHz	
		Out: Ch3, Ch4 LVDS 2.5 V	625 MHz	$M1 = Ch3 - Ch4$, black SMA cables
26	Si5344	In: Ch0 LVCMOS 1.8 V	125 MHz	
		Out: Ch3, Ch4 LVCMOS 1.8 V	125 MHz	$M1 = Ch3 - Ch4$
27	Si5344	In: Ch0 LVCMOS 1.8 V	125 MHz	
		Out: Ch1, Ch2, Ch3, Ch4 LVCMOS 1.8 V	125 MHz	
28	Si5344	In: Ch0 LVCMOS 1.8 V	125 MHz	
		Out: Ch1, Ch2 LVCMOS 1.8 V, Ch3, Ch4 LVDS 2.5 V	125 MHz	$M1 = Ch3 - Ch4$
29	Si5344	In: Ch0 LVCMOS 1.8 V	125 MHz	
		Out: Ch1, Ch2, Ch3, Ch4 LVDS 2.5 V	125 MHz	$M1 = Ch3 - Ch4$, $M2 = Ch1 - Ch2$
30	Si5344	In: Ch0 LVCMOS 1.8 V	125 MHz	
		Out: Ch1, Ch2 LVDS 2.5 V	125 MHz	$M2 = Ch1 - Ch2$

Table 3: List one of measurements made for this thesis. Shown in chronological order are the measurements by the measurement number (no.) characterised by the device under test (DUT), the input and output signal types and frequencies. All channels correspond to those used on the oscilloscope. $M1$ and $M2$ denote the mathematical function shown in the commentary.

No.	DUT	Signal	Frequency	Commentary
31	Si5344	In: Ch0 LVDS 2.5 V	125 MHz	
		Out: Ch1, Ch2 LVCMOS 1.8 V	125 MHz	
32	Si5344	In: Ch0 LVDS 2.5 V	625 MHz	
		Out: Ch1, Ch2 LVCMOS 1.8 V	125 MHz	
33	Si5344	In: Ch0 LVDS 2.5 V	125 MHz	
		Out: Ch1, Ch2, Ch3, Ch4 LVCMOS 1.8 V	125 MHz	
34	Si5344	In: Ch0 LVDS 2.5 V	625 MHz	
		Out: Ch1, Ch2, Ch3, Ch4 LVCMOS 1.8 V	125 MHz	
35	SG	Out: Ch0 LVDS 2.5 V	125 MHz	$M1 = Ch1 - Ch2$
36	CTB	In: Ch0 LVDS 2.5 V	125 MHz	
		In: Ch1 LVCMOS 1.8 V	125 MHz	
		Out: Ch1, Ch2 LVCMOS 1.8 V	125 MHz	
37	CTB	In: Ch0 LVDS 2.5 V	125 MHz	
		In: Ch1 LVCMOS 1.8 V	125 MHz	
		Out: Ch3, Ch4 LVCMOS 2.5 V	125 MHz	
38	CTB	In: Ch0 LVDS 2.5 V	125 MHz	
		In: Ch1 LVCMOS 1.8 V	125 MHz	
		Out: Ch1, Ch2 LVDS 2.5 V	625 MHz	$M1 = Ch1 - Ch2$
39	CTB	In: Ch0 LVDS 2.5 V	625 MHz	
		In: Ch3 LVCMOS 1.8 V	625 MHz	
		Out: Ch1, Ch2 LVPECL 2.5 V	625 MHz	$M1 = Ch1 - Ch2$
40	CTB	In: Ch0 LVDS 2.5 V	625 MHz	
		In: Ch3 LVCMOS 1.8 V	625 MHz	
		Out: Ch1, Ch2 LVCMOS 1.8 V	125 MHz	
41	CTB	In: Ch0 LVDS 2.5 V	625 MHz	
		In: Ch3 LVCMOS 1.8 V	625 MHz	
		Out: Ch1, Ch2 LVCMOS 2.5 V	125 MHz	
42	CTB	In: Ch0 LVDS 1.8 V optical	125 MHz	
		Out: Ch1, Ch2 LVDS 2.5 V	125 MHz	$M1 = Ch1 - Ch2$, $M2$ reference
43	CTB	In: Ch0 LVDS 1.8 V optical	625 MHz	
		Out: Ch1, Ch2 LVDS 2.5 V	625 MHz	$M1 = Ch1 - Ch2$, $M2$ reference
44	CTB	In: Ch0 LVDS 1.8 V optical	125 MHz	
		Out: Ch1, Ch2 LVDS 2.5 V	125 MHz	
45	CTB	In: Ch0 LVDS 1.8 V optical	125 MHz	
		Out: Ch1, Ch2 LVPECL 2.5 V	625 MHz	$M1 = Ch1 - Ch2$, $M2$ reference

Table 4: List one of measurements made for this thesis. Shown in chronological order are the measurements by the measurement number (no.) characterised by the device under test (DUT), the input and output signal types and frequencies. All channels correspond to those used on the oscilloscope. $M1$ and $M2$ denote the mathematical function shown in the commentary. For measurements of optical signals an electrical reference signal was used.

F.1 Rise Time

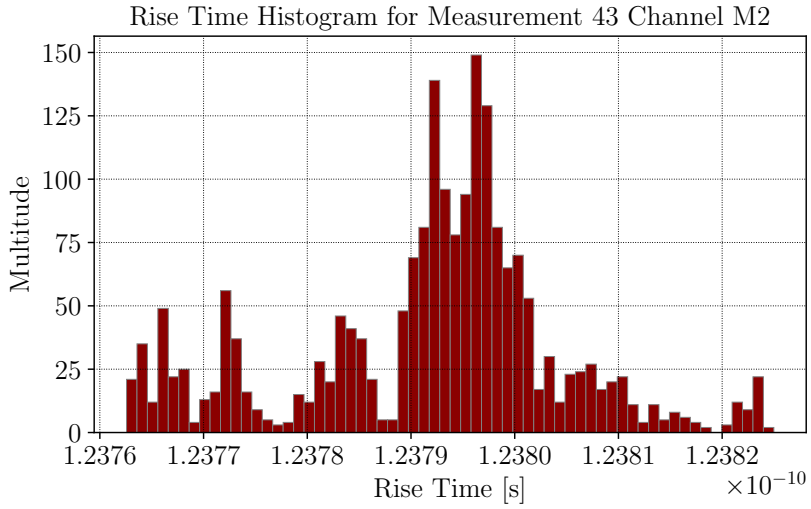

Figure 16: Rise time histogram for measurement 43 channel M2 with the Si5338 as DUT.

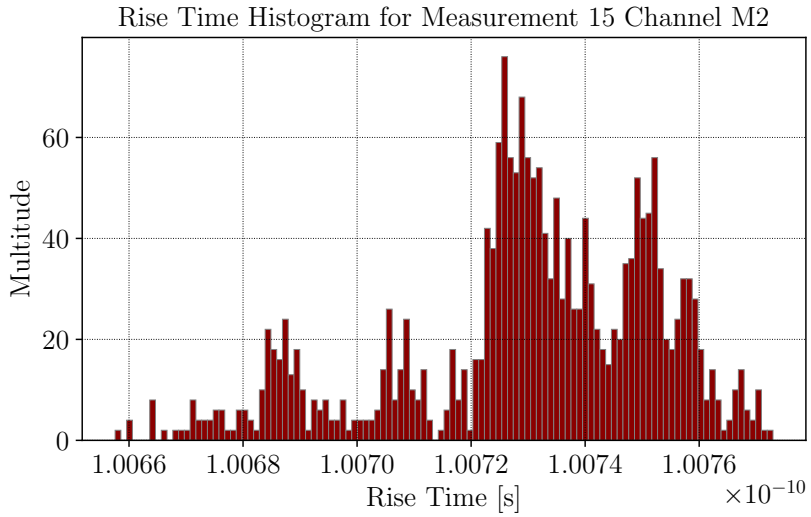

Figure 17: Rise time histogram for measurement 15 channel M2 with the Si5344 as DUT.

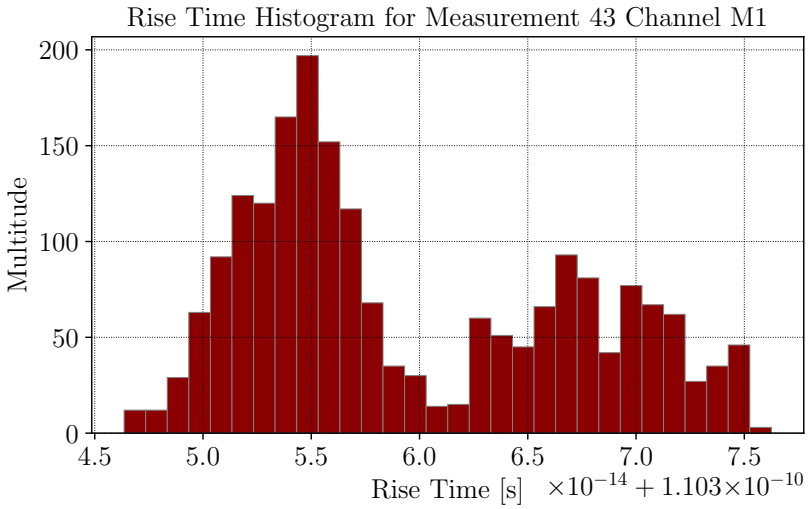

Figure 18: Rise time histogram for measurement 43 channel M1 with the CTB as DUT.

F.2 Phase Stability

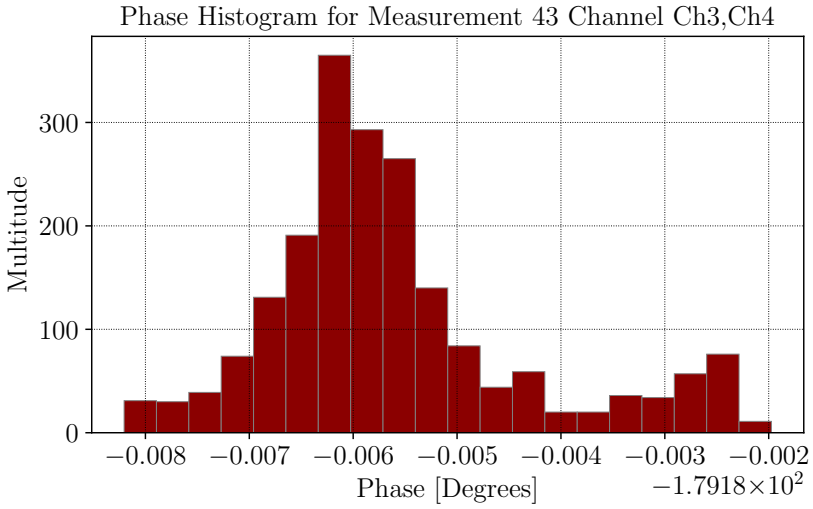

Figure 19: Phase stability histogram for measurement 43 channels Ch3,ch4 with the Si5338 as DUT.

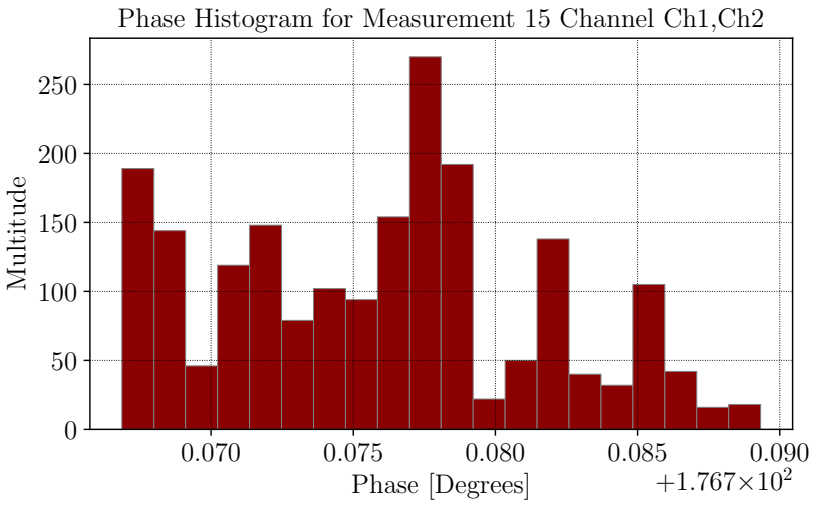

Figure 20: Phase stability histogram for measurement 15 channels Ch1,Ch2 with the Si5344 as DUT.

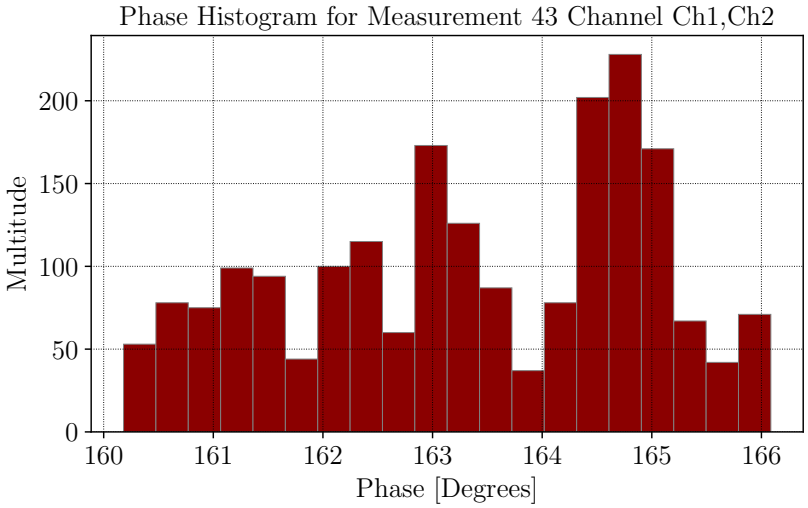

Figure 21: Phase stability histogram for measurement 43 channels Ch1,Ch2 with the CTB as DUT.

List of Figures

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Bibliography

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